8085 Imstructions

1) MOU > MOU Rd RS => 1 Byte, 1 Machino cycle, 4-T state [Mound]

Mou M => 1 Byte 2 machino cycle, 7-T state.

More is every to anche & bit down compart from two registers (sawlo and do stimation) ewhen it in Register specified.

Jon Mov H, M is the memor address whole content is properly by HIL register paint

- 2) Mu Tr. 8 bit deute -> 2 Byte 1 2 machino cylo 1 7 7 stute Entremos modo M]

 H is uned to make 8 bit date into Register. [mode immediate]

 Mu I Register, 8 bit deta -> makes 8 bit data to registe immediaters

 Mu I M, deuta -> 6 local .8 bit data into a memory location pointed by

 HL pain immediately -> 2 Byte, 3 machinoayle, 10 T states

 H is immediate addressing med
 - 3) ADD => ADD R => lined to add combent of Register specified to Accumulators content. 1Byte, 1 machino ayds, 4 T- states.

ADD M -> add constent specified in morroy location painted by HL paint to combent of Accommutation.

1 Byte, 2 machino aydo, 7 T-stales. au plays modified.

- [Add mondrate] 2 byte, 2 machine cycle, 7 T-state.

 Ou plays modyied. Januardvak addressing mode.
- 5) ACI > add evil (along immellate to Accumulator). ACI 8 bit date.

 Otal 8 bit date to comberil of Accumulators along evil acuty.

 It is immediate addressing amode. all fless core modified.

 2 byte, 2 machino cyle, 7 T-Stale.

ADC => add enth catory.

att ADC R -> add one company of Register specified to combin

9 Accumulated along enigh catory.

1841e, 1 machine byolo, 4 Tsteater

ADC M > add the combest present at monogry accution pointed by the pair to content q Rogister along enter cotting.

18 yte, 2 machino cycle, 7 T-Stub.

All flegs are modified.

7) AMA => "AMB Accomulator".

ANT R -> logically perform "And" spercotion contin between contond of Register specified and compent of Accommulation.

1 Byte, 1 machino cylo, 4-Tstate.

ANTA M=> logically perform "AND" of shatism with content located at memory address pointed by 1-12 pain and content of Accommutator.

1846, 2 madrino cycle, 7 T-state.

Auxillas fly is set and contyping is Reset.

ANI = And immediate cuit Acamutation.

ANI & bit duta >> to logically perform Anni operation between & bit cloth specycled and content of Accountation.

A is immediate addressing mode.

2 byte, 2 machine curges, 7 T-state
carollag has is not to 0

Auxillar has is not to 1.

a) CMA => complement Accumuton. A herporm i's comporment on contenty Accumulation, nonwell is Stotact in Accumulator it self. mos flogs moderned. 1 byte, imachine cyclo, 4 T-states 10) CMP => compaire Accumulator CMP R=> und to compare content of Rogister specified and content of Accumulation. His basically [A-R] openation. Hags have water depending on A-P. 18 [A-R] renew is postue [+40] = non signified = 0 Zeroflag = 0 (099) blag = 0 '6[A-R] remult is megation [- no]=> 2290/10920 carryllug=>0 I [A-R] Tresuettis equal in [A=-R] => signflag=>0 30toflag=> carryflag => 0 1 byte, Imachino ayou 4 T-states CMP M=> to compare consent of Accommulator with content of spronet at momory location pointed by the pain. 1 byte, 2 machino cydo, 7 T-states.

11) DAA => Decimal Adjust Accommunator.

The 86H mumber in accumulatis adjusted to John two 4 bit QCD.

Trules 16 value q least signy cont 4 bits of Accommentors is greater than 9 as

y AC flag 15 Set, 6 15 added to Accommendator.

that a mast significant 4 bits of Accumulation is now grades than a, on if CY blag is set, b is added to the most significant 4 bits of the accumulation.

All flags are modified. 10 yte, 1 machinocyte, 4 T- States

12) DCR => Decement.

DCR R > unact to doctreement me content of Register by one.

It is basically subtract I from the negister specified contents

decreement value is stored on Register R specified.

au flag except cooryflag is machines 1 byte, I machine cycle, 4 T-state.

DCR M-> decreemed on content prieset at momory location pointed by HL Registor hair by one.

1 byte, 3 machine oydo, 10 T- states.

13) DCX => DCX Rp => do Orcomed Rogisto, pain 1 De overment Xtended negista pain
This instruction in lineal to document Contend of Rp Hocyard by 1.

and neglect is stoked in Rogisto pain it self
mo bits are affected.

1 byte, imadine cyde, 6 T-stacks-

14) HLT - hout the microphocesson. This is the ICIST statement instruction in any 8085 program of tells the ENDY Execution 9 8085 programs If executes workens Instruction and holds and further execution. Report is moossary to exit from how states 1 byte, 2 or more machino cycle, 50% more Tstader. (5) INR => Inverment INR-R => This instruction industret the value of Register specified by one. It adds 'I' to combent of Rogister, and result is stored in Rogister Hoelf. All plags exopt carryllag is modifieds 1 byte, Imachino cyclo, 4 T-State. INP-M=> it impresents the constant prenent of momory location ported by 1-12 registor hain by ame. 1 Byte, 3 machino cyclo, 10 Tstale.

- 16) INX => INX RP -> Incerement Xendod Register pain.

 This investment is used to increamond the content of Register pain frequent by I and nemed is stoned in Register pain it sets.

 The flag bits are appeted.

 I byte, Imachine cycle, b T-states.
- The suncondito jumps 1 runconditional Jump

 The 16 bit address. The program sequence is throus period to memory address given in the openand.

 3 byte, 4 machine cycle, 10 Tstate.

Those is no condition to jump.

- 18) JC => Jump on carry set. His a conditioned jump.

 JC 16 bit addenses I label. The program beginne is 49 conspensed to particula label of 16 bit addenses i 16 carry flag is sed (1).

 3 byte, 3 machine and 10 T states
- JNC 16 bit address I casel. The program seasonce is transpersed to particular label or 16 bit address 16 carrifley 15 neset (0).

 [mo corry].

 3 byte, 3 machine cycle, 10 T states
- 20) JZ > Jumpon 30900 H 1s a condutored Jump.

 JZ 16 bit address 1 label. The program sequence ist grangested to particular label 1 16 bit address i6 3etropay is Let (1).

 3 byte, 3 machine uyule, 10 T-Stuke.

- 21) JN2 => Jump on Non Zero. This is a conclutional jump.
 The program seasons is thomsperhad to hartranar label at 16 bit address
 if zero play is never [6]. no zero flag net.

 3 byte, 3 machino cydo, 10 T-stale
- 22) LDA > load Accomplets.

 LDA 16 bit address shis implenction is known to load the Accompletes with content from 16 bit memory specified.

 Accompletes will have 8 bit content from 16 bit address.

 Absolute addressing mode.

 Mo flags are modified.

 3 byte: 4 machine yullo: 13 T-states.
- 23) LDAX-1RP > locard accumulated from memory pointed by extended Registed path . His an indirect addressing mode.

 Registed path . His an indirect addressing mode.

 Only BC and DE registes path are unal feet LDAX RP.

 LOAX H is morphished in \$085, because, it is same as

 Mov A, M in its function.

 1 byte, 2 machine oyde, 7 T-Stule.
- 24) LXI => 100d register pair immodiate

 LXI RP, 16 bit data This imstruction loads 10 bit data into one

 Speciel register pair.

 BC, DP, HL are the register hair.

 Immediate addressing mode.

 mo plays are modified.

 3 byte, 3 machine ague, 1 to T-states

25) ORA => OR Accumulatos.

grouped Rogister constant and consons of Register.

The nexuel & stoped in Accommutation

1 byte, imachino ordo, 4 T- states

of memory location pointed by HL negretation with contents prenet

1 byte, 2 mouhim mydo, 7 T- state.

26) ORIS OR immodrate aum Accomunation.

ORI & bildate > it fetyorms of operation on & bit data
Specyledard evil content of Accommendate. The result is stored
in Accumulations

coolighting and AL are herest to 0.

2 bytes, 2 machino cyclo 17 T- States

27) RAL => Rotate Accumulator left mogh courty.

ya motetes the Accumulator content to bit by 1 bit position.

bit I man MSB is copied to CY blog bit, previous Cy bit will be maded to least significant bit of Accumulation.

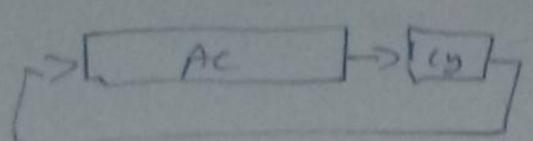
Thus it is abit notation of Accumulation of CY blog.

only carry blag is affected.

1 Byte, Imachine orde, 4 T-State

23) RAR -> Rotate accumulators Right shrough cassing.

28) RAR -> Rotate accumulators combined to Right by 1 bit position.



The least significant bit is coming out and evil he copied on Glay bit and previous Cyplay bit will be maded to the most significant bit postion of accumulation.

There it is a bit restation of Accumulator.

Only copyring is affected.

I Byte, I machine cycle, 4 T- State.

29) RLC => Rotate left A commutation, endnown courses

A grotate the content of Accumulation to left bit by 1 position.

oms B of Accomplated and Como out and left notate will breake an omto space at ISB and shis common bit will be copied at empty bit place and also on the carry bit in flug negister. Thus carry pag gets a copy of pt maded out from his bit position.

A is only 8 bit 90 tector of Accumulator contents only carrying is affected

1 Byte, Imachino ydo, 4 T- States

36) RRC => Rotate Right accumulates. employed casay.

H motate no combin q Accumulates to signed by 16H position.

in play negister and also will be copied to miss position of Accumulation.

This & bit notation of Accumulation content.

Only carry play is affected.

1 byte, Imachino cydo, 4 T- states

31) STA => Store accumulated.

BE STA 16 bit address. This insafuction is und to store

Accumulation 8 bit contend to specified memory location.

This is absolute addressinging mode.

Me plays are modified.

3 Byle, 4 machine ayde, 13 T-States.

32) STAX => Store Accumulates content in moments hainted by
extended regarder RP.

STAX RP. This instruction was register indirect addressing
mode for specifying destination.

Me content of Accumulates will be written to memory location pointed
by 10 bit address or storad in Register pair.

1 Byte, 2 machine or do, 7 T-States.

33) SUB > Subtigad.

SUBRED und to subthact content of Register specified from Content of Accumulaton.

1 machin oyd, 1 Byte, 4-7 states all play modified.

SUB M=> unod to sub1910ct content prosent in momory 10 cotion pointed by HL pain brom content of Accumulators. 1 Byte, 2 machino eydo, 7 T-studo.

34) SUJ => subilitated Immodiates

SUJ 8 bit dota >> subtract a 8 bit data brom Accumulator condent and Store result in Accumulator. all plays madified. Immodiate addressing modo.

2 Byte, 2 machino Mydo, 7 T-state.

35) SBD=> subthact evin Borran.

SBBR = Subtlact contet of specified Registers from Accommutators Content along with Bothow. The nessed is stored in Accumulator. 1 Byte, Imachin odo 147 stata

SBB M-> Subthact content specyted at morroy location pointed by ht pain olong with borrow-

1 Byte, 2 machino ogolo, 7 T- stato. au flags are modified.

XPA R=> porform logical Exclusion OR operation on Registor.

Content and Accumulation Condon.

Rosaud is storad in Accumulation.

1 Byte, I machine cycle, 4 T- State.

XPA M=> perform logical Exclusion OR operation on content

Spooned at mornoly location pointed by ht pain.

1 Byte, 2 machine cycle, 7 T- State.

27) XRJ => Exclusive GR Immoduate ewill Accumulator.

XRI 8 bit data => This instruction is Used to herform

FX-OR between 8 bit data and Accumulator contendo

The result is storad in Accumulator.

2 Byte, 2 machino cycle, 7-Tstates