FUNCTIONALITY OF 8259 [PROGRAMMABLE INTERRUPT CONTROLLER]

→ 8259 microprocessor is defined as Programmable Interrupt Controller (PIC) microprocessor. There are 5 hardware interrupts and 2 hardware interrupts in 8085 and 8086 respectively. But by connecting 8259 with CPU, we can increase the interrupt handling capability. 8259 combines the multi Interrupt output, Interfacing of single PIC provides 8 interrupt inputs from IR0-IR7.

Features of 8259 Programmable Interrupt Controller:

The features of 8259 programmable Interrupt Controller are

- Intel 8259 is designed for Intel 8085 and Intel 8086 microprocessor.
- It can be programmed either in level triggered or in edg. triggered interrupt level.
- We can masked individual bits of interrupt request register.
- We can increase interrupt handling capability upto 64 Interrupt level by cascading further 8259 PIC.
- Clock cycle is not required.

1] It can manage eight priority interrupts. This is equivalent to providing eight interrupt pins on the processor in place of INTR pin.

2]. It is possible to locate vector table for these additional interrupts any where in the memory map. However, all eight interrupts are spaced at the interval of either four or eight locations.

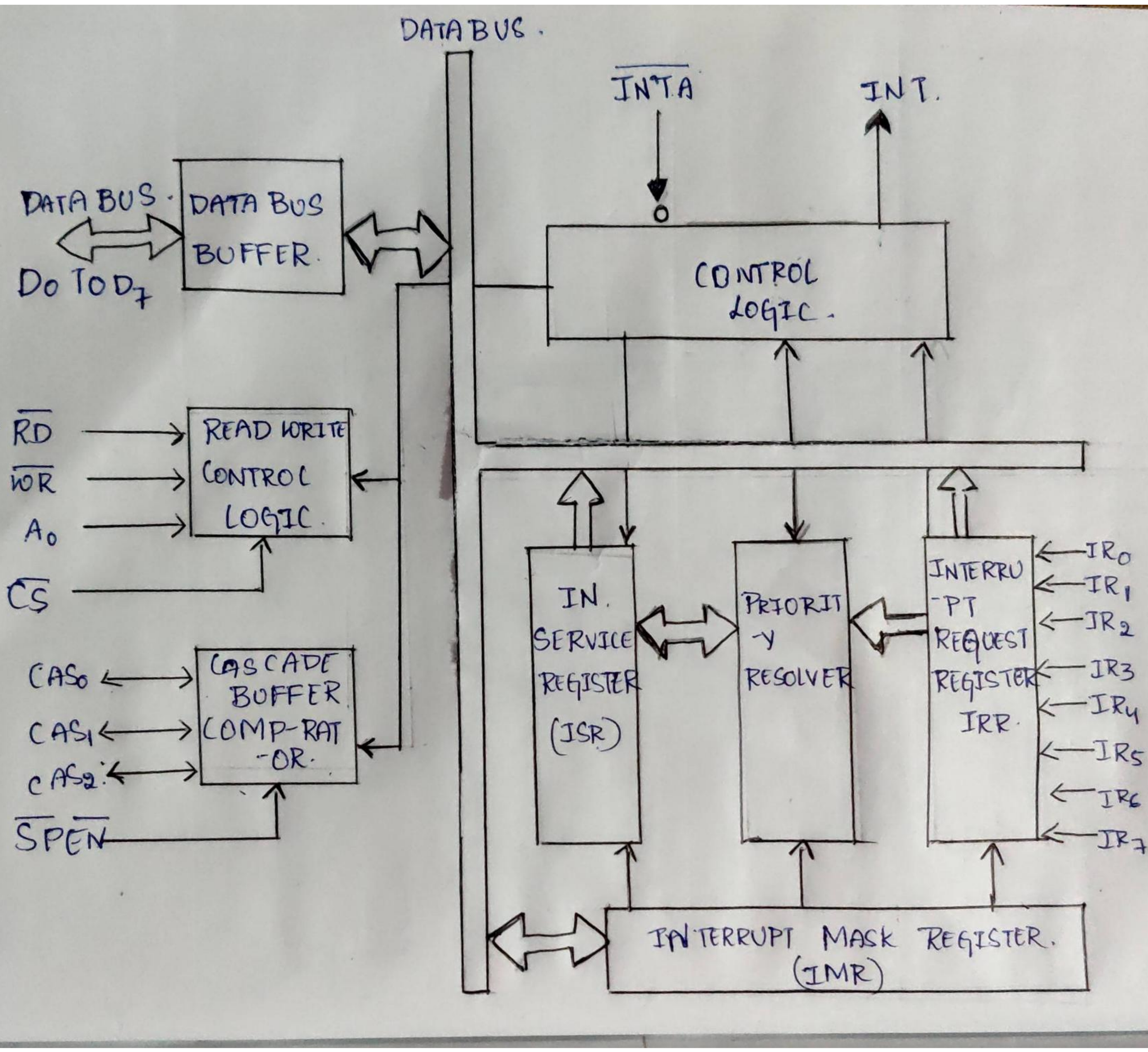
3] By cascading nine 8259s it is possible to get 64 priority interrupts.

4]. Interrupt mask register makes it possible to mask individual interrupt request.

5]. The feature of 8259 A can be programmed to accept either the level triggered or the edge triggered interrupt request.

6]. With the help of 8259 A user can get informations of pending interrupts, in-service interrupts and masked interrupts.

7]. The Features of 8259A is designed to minimize the software and Realtime overhead in handling multi-level priority interrupts.



BLOCK.	DESCRIPTION.
*Data Bus Buffer.	This block is used to communicate between 8259 and 8085/8086 by acting as buffer. It takes the control word from 8085/8086 and send it to the 8259. It transfers the opcode of the selected Interrupts and address of ISR to the other connected microprocessor. It can send maximum 8-bit at a time.
* R/W Control Logic.	This block works when the value of pin CS is 0. This block is used to flow the data depending upon the Inputs of RD and WR. These are active low pins for read and write.
Control Logic.	It controls the functionality of each block. It has pin called INTR. This is connected to other microprocessors for taking the interrupt request. The INT pin is used to give the output. if 8259 is enabled, and also the Interrupt flags of other microprocessors are high. then this causes the value of the output INT pin high, and in this way this chip can responds requests made by other microprocessors.
Interrupt Request Register.	It stores all interrupt level that are requesting for Interrupt service
Interrupt Service Register.	It stores interrupt level that ~~will be~~ are ~~masked to~~ currently being execute.

Interrupt Mask Register.	It stores interrupt level that will be masked, by storing the masking bits of interrupt level.
Priority Resolver	It checks all three registers, and set the priority of the interrupts. ~~It~~ Interrupt with the highest priority is set in the ISR register. It also reset the interrupt level which is already been serviced in the IRR.
Cascade Buffer.	To increase number of Interrupt pin, we can cascade more number of pins, by using cascade buffer, when we are going to increase the Interrupt capability, CSA lines are used to control multiple interrupts.