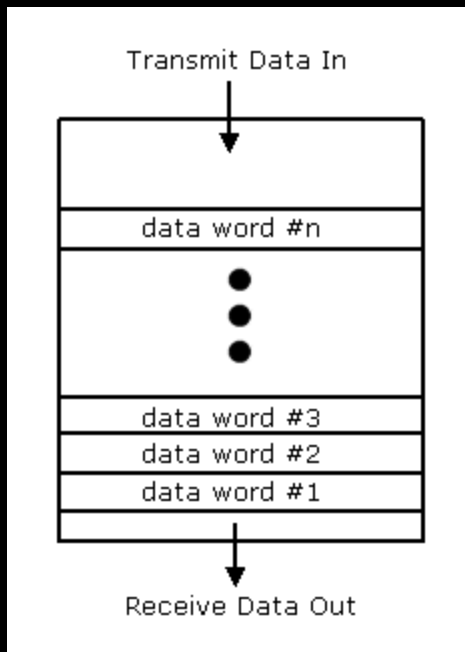


FIFO RAM

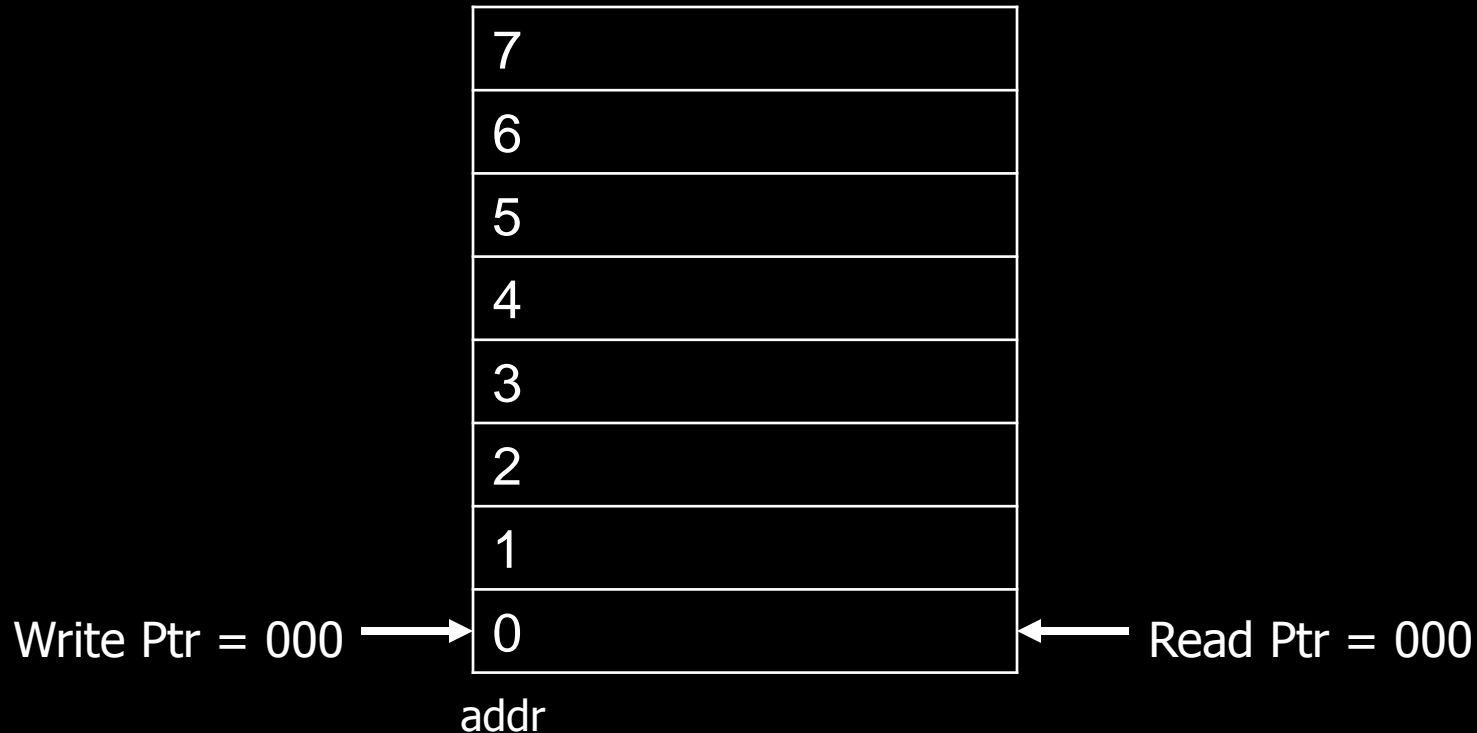
FIFO Design (provided)



Why can't this be done with a simple shift register?

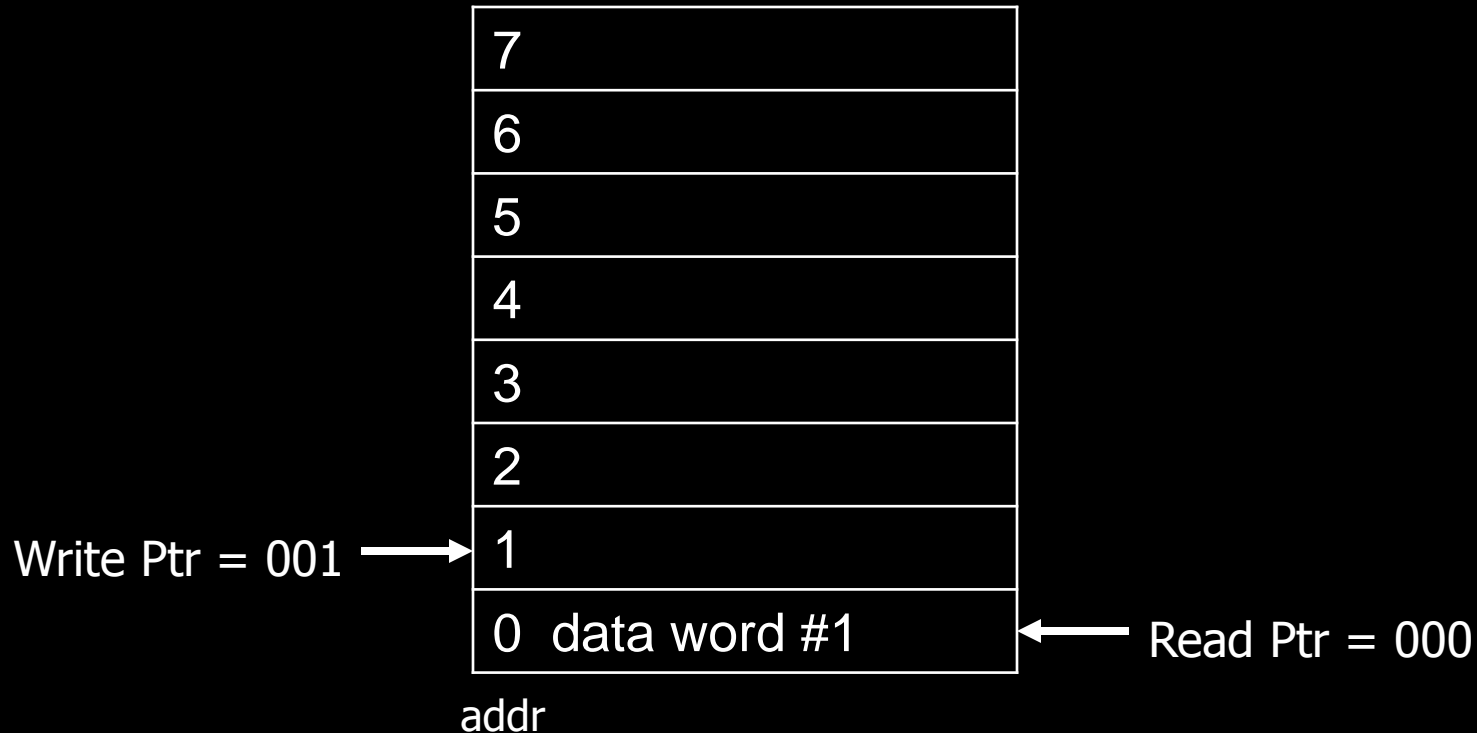
- Purpose:
 - Efficiently handle data transfer between two systems
 - Allows source & receiver of data to operate at different speeds (& clock rates)
- Some Requirements:
 - Data must be read out in same order as written in
 - Can't assume synchronization between input and output
 - Next word in FIFO must be immediately available to read.

FIFO Operation



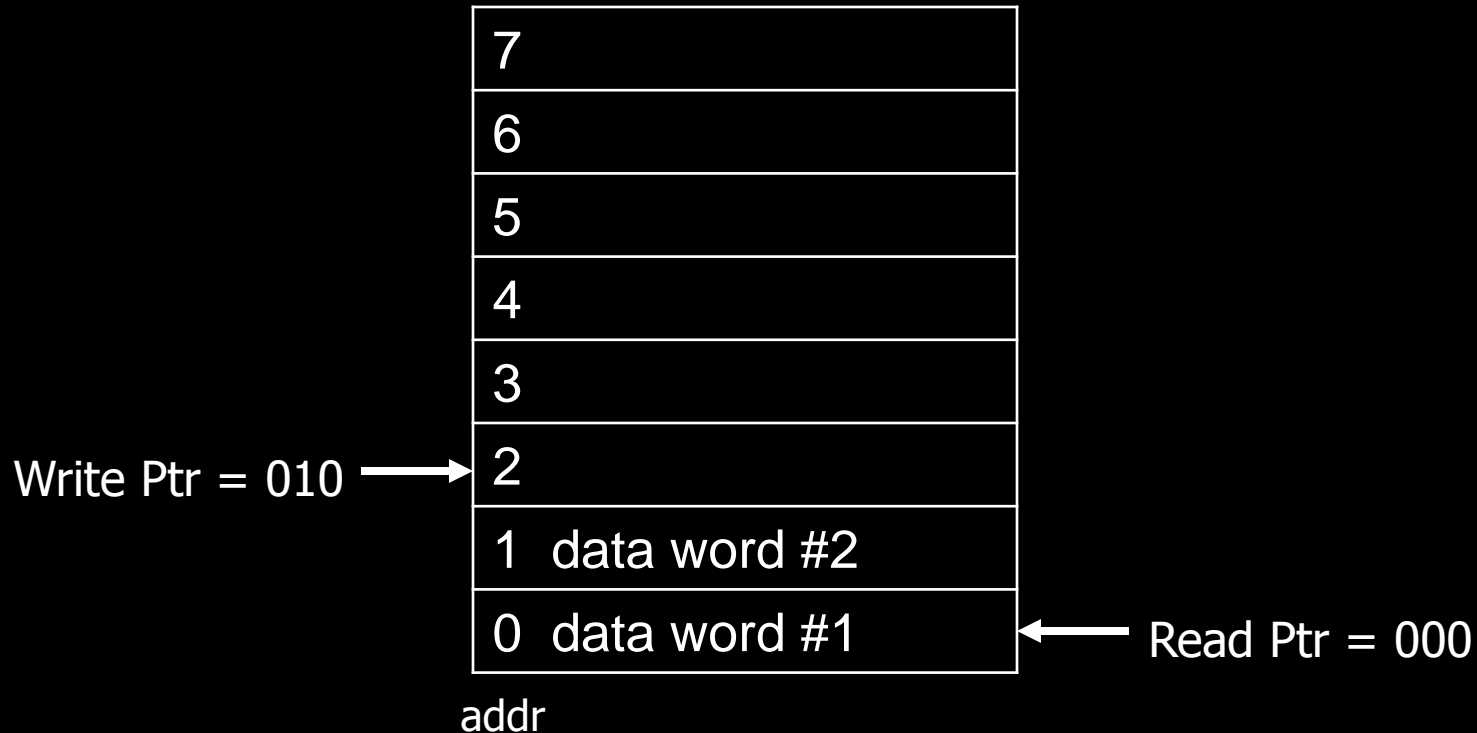
Prior to writing anything
FIFO is empty, Write Ptr = Read Ptr

FIFO Operation



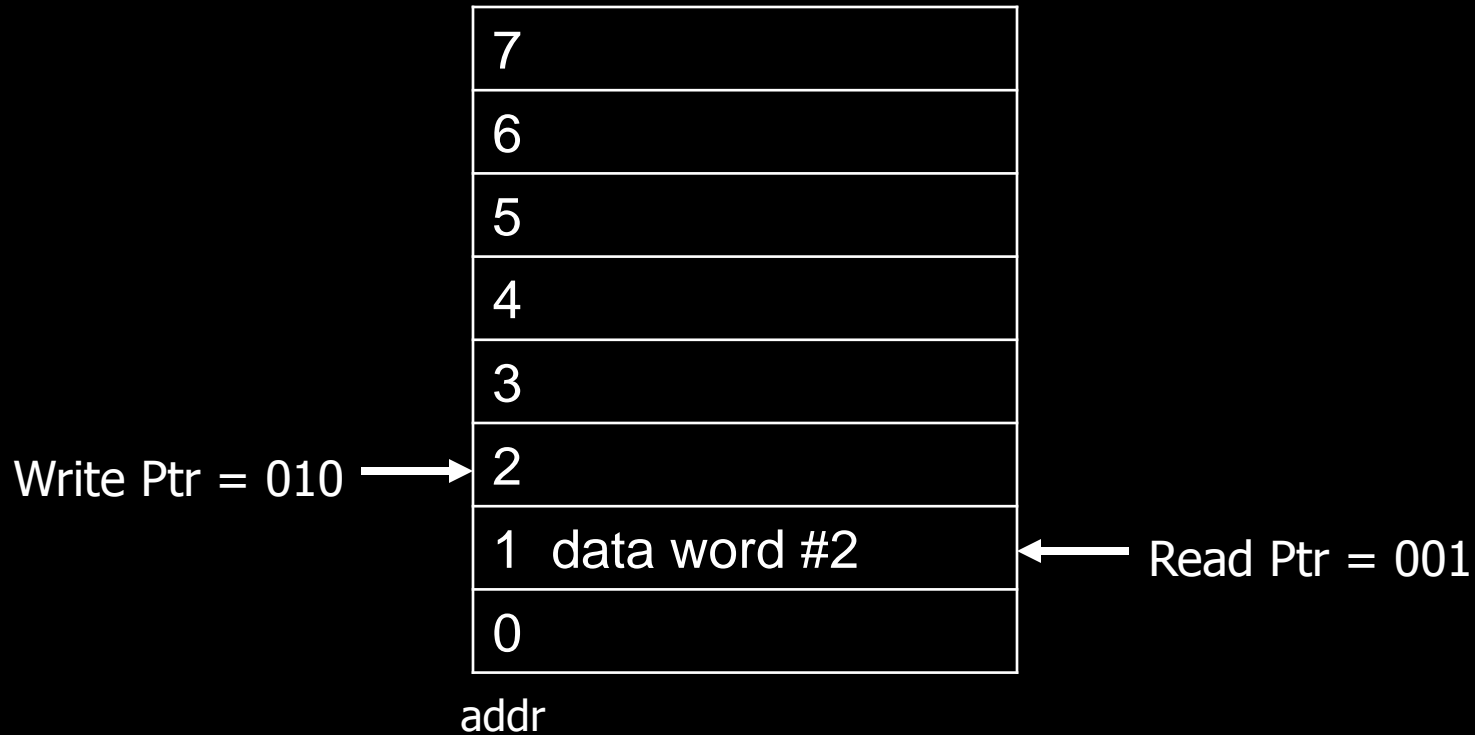
After 1st word written

FIFO Operation



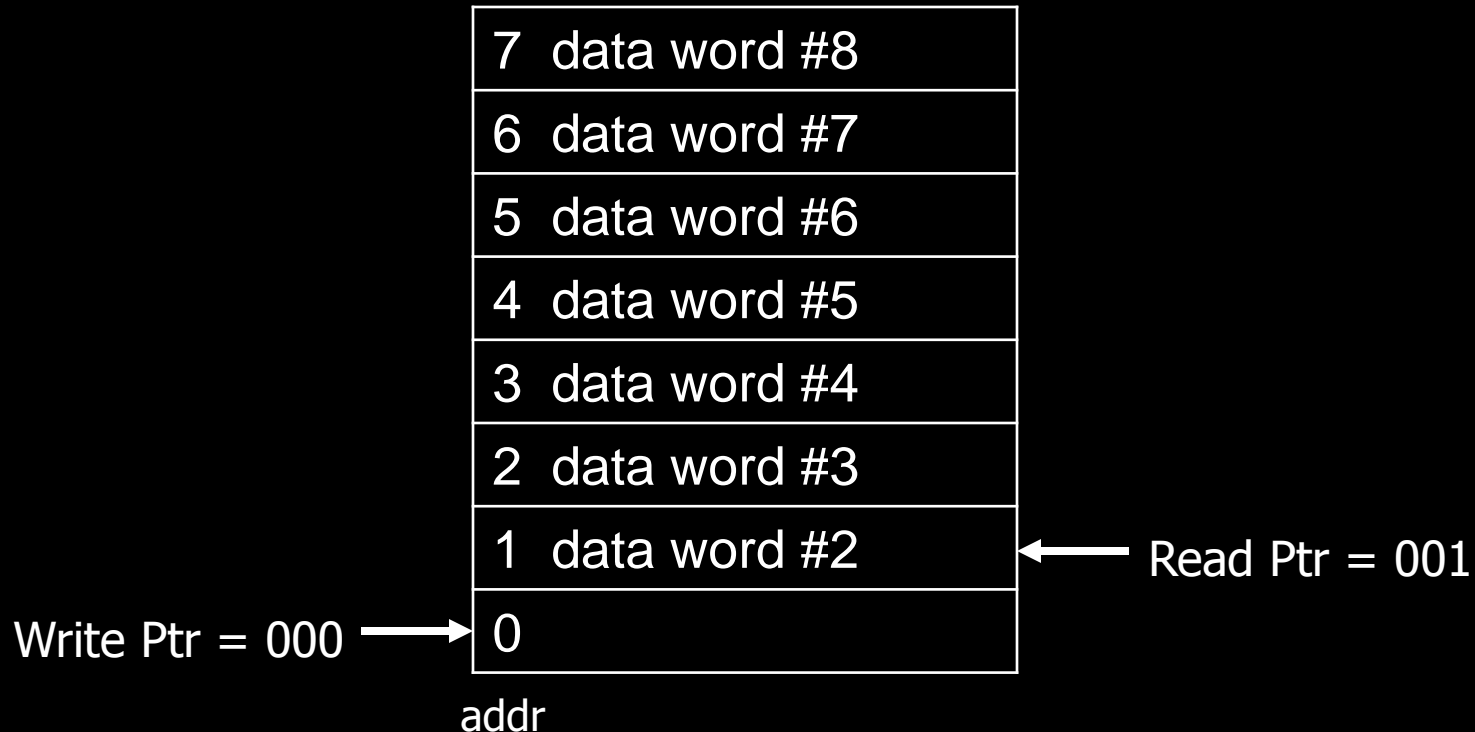
After 2nd word written

FIFO Operation



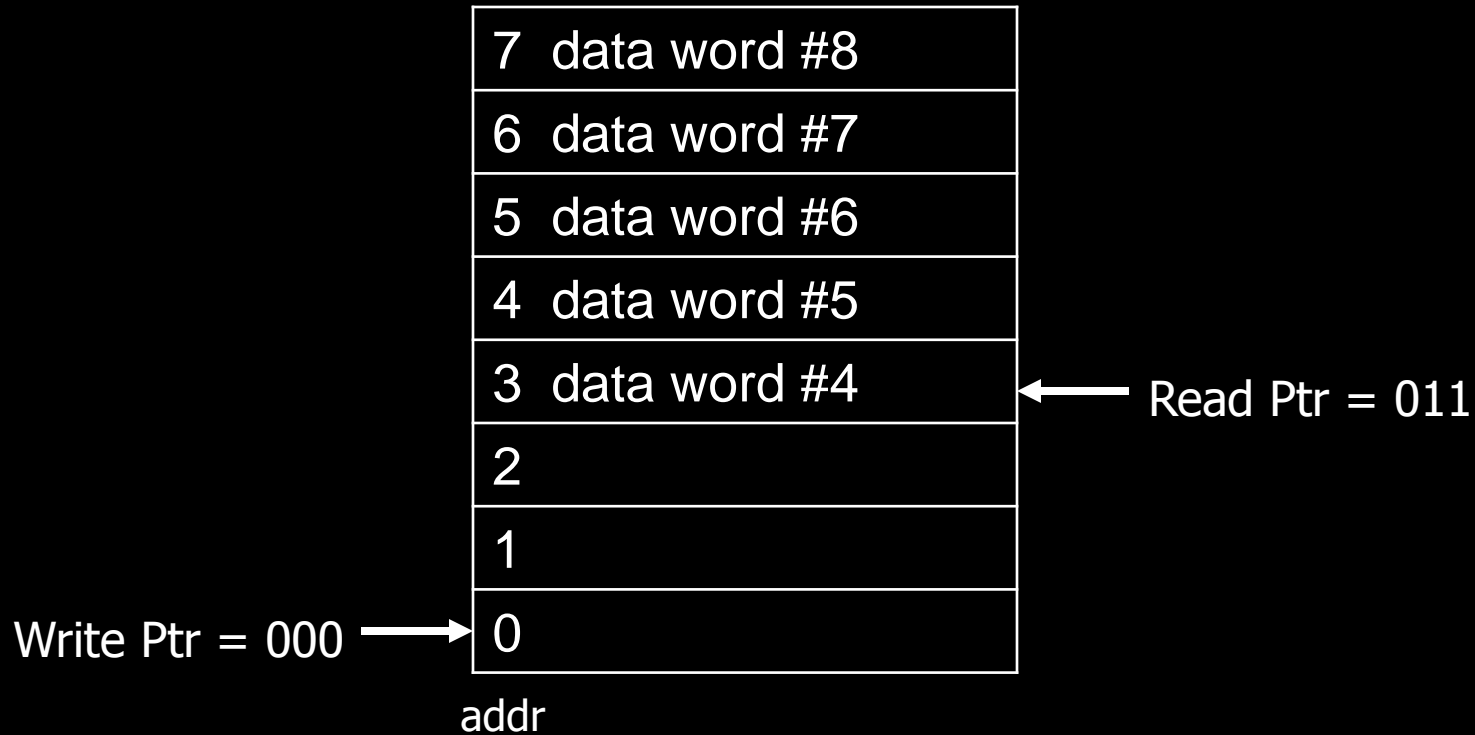
After 1st word read

FIFO Operation



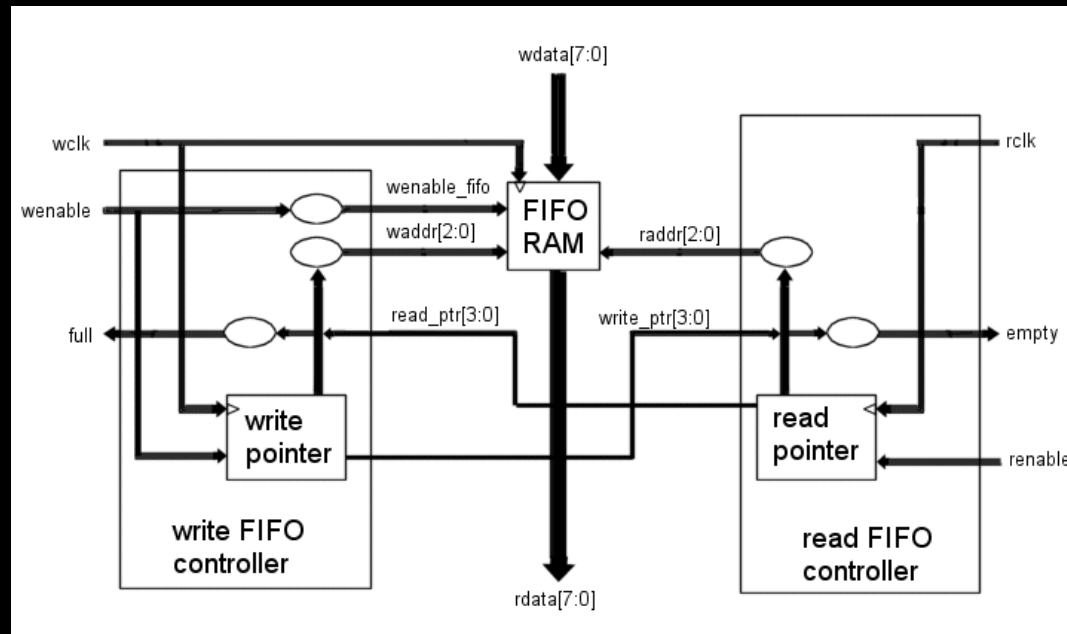
After 7 more words written
Notice write pointer wrapped around

FIFO Operation



After 2 more words read

FIFO Implementation



Write controller:
Checks for full condition.
If not full, writes data &
increments write pointer.

FIFO RAM:
A set of 8 registers,
8 bits each, with
addressing logic

Read controller:
Checks for empty
condition. If not full,
increments the read
pointer.