ilps

Flip-Flop

s

* sequential

logic

A

combinational

cft.

olps

7 Memory

elements

*

& Memory elements

store binary

information which defines the

shate

f

the sequential

circuit

at any given

time.

* byn chronous sequential cket--when olp change states in time with a clock

A clock signal must be present inorder for the alps to change `state.`

synchronous sequential circuits

*

that use clock pulses in the ips of memory elements are called clocked sequential circuits & Ampschronus - independent of clocking. The op can change thate without having to wait for a clock pulse.

* Flip flops are memory elements used in requention circuits.

★ A

FF ū a bistable electronic

تر

circuit that has 2 stable states.

it's opp is either ov (0) or +5v (1).

since it opp

will remain as set untill somethi

A FF has memory

ид

is done to

change

device.

it

memory

*

Binary information can enter a FF is a variety of ways, giving rise to different types of FFA

4 Easiest to

to way

to construct a FF is to connect 2 inverters in series.

V2 B

V3

A

B

X3=0V

V1 = V3=OV. If a fl6 line is connected, removing the and at V1, V1 = √3 = 0V

راله

+Vcc V1=5V

V2
=OV

Do

V2 = 5V

(v, xvg

remai -n *at*

5V with feed

back)

*

SR/as flip

flop

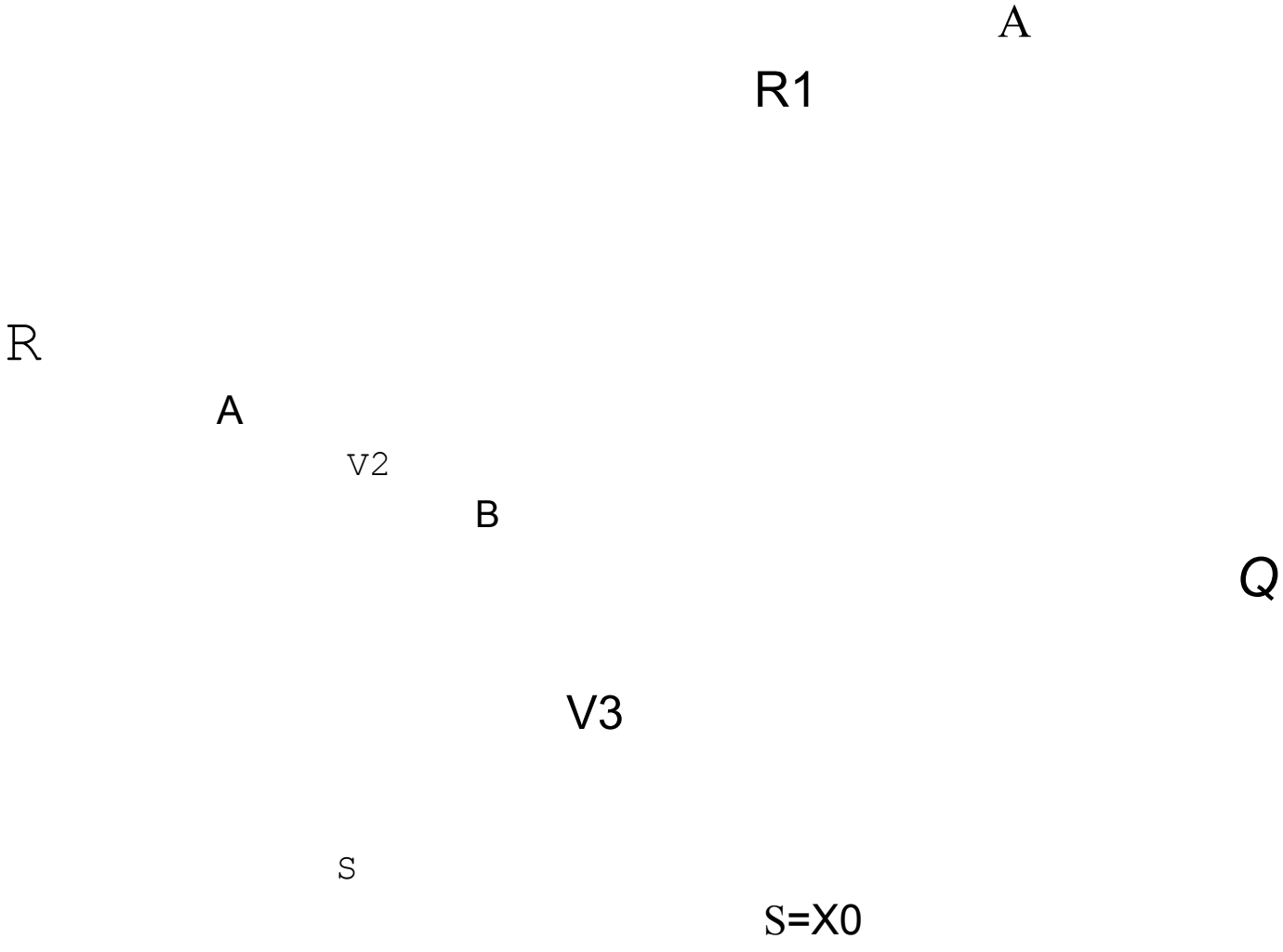
The additional ilps on NOR and

NAND galés provide a

convinient

means for application of i/p signals

to switch the FF from one state to the other.



か

او

Reset

B

set

RS

Q

a

faction

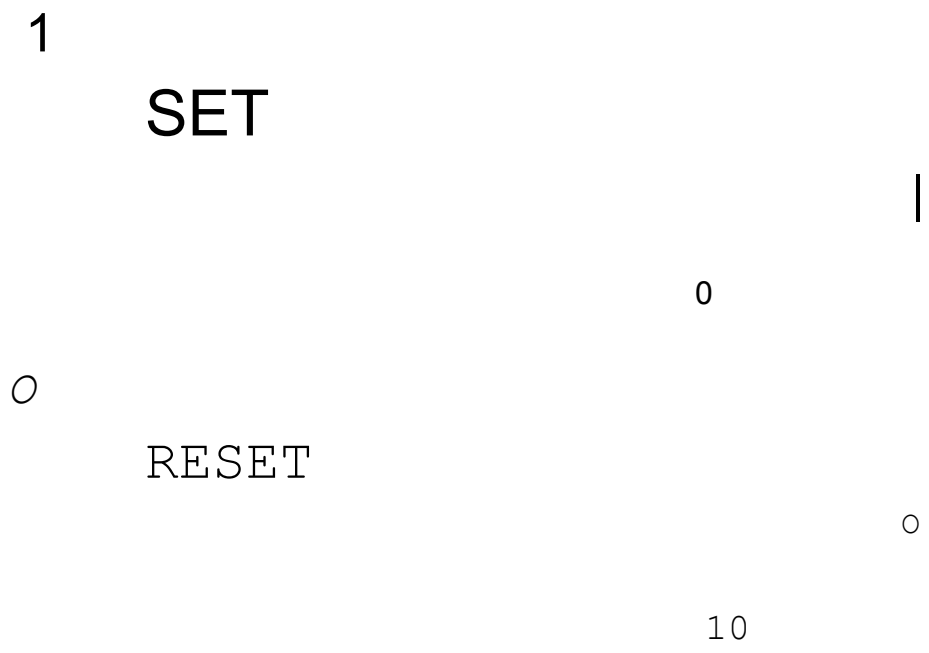
Nor

деят

до

last state No change

x



Forbidd
en

* for a NOR gate if any ipps is 10/piso.

* R=S=0 : since a o *elp* of NOR gate has no

effect in its o/p,

the FF remains in last state.

* R=0, S=1 : Ŕ=0, both

i)ps of

gate A are o, so Q=1. Thus I at,

Silp is said to SET the FF and it switches to stable state where

Q=1

* R=1 S=0 : Q=0, Q=1:.RESET the

FF and *it* switches to a stable

state Q=0.

* R=S=1: Both ax Q

= 0

o at the

same time. Hence this state is

forbidden

R

Q

100

NAND gate latch (Rs FF)

In

5

A

ارکا

A

·R

ol

R =X,

B

NAND

RS

R S

a

x

00

1

1

Last state

y

อ |

10

1

(SET)

o

10

0 1

o

10

0

ง

0

(RESET)

02

(Forbidden)

& A low on any i/p of

forces it's o/p to 1.

110

NAND gate

R S

Q

s

Do

Do

甲

oo last the

01

Do

Rad

اھ

1.

○

?

S

R

اتھ

Q

yo Both these FFA (NAND A NOR gates) are haid to be transparent as any change in ip information at hands is housmitted immed -iately to the olp at a and Q according the T.T.

clocked Rs *FFS*

Enable=

0

R

Q

S

Q

Ltı

Q

R

EN RSF

Qntl

Ч

D

xx

Qn

1

до

Q

01

1

?

* Addition

of

2 AND

gates at the RAS

дей

ülps will result in a FF that can be enabled or disabled.

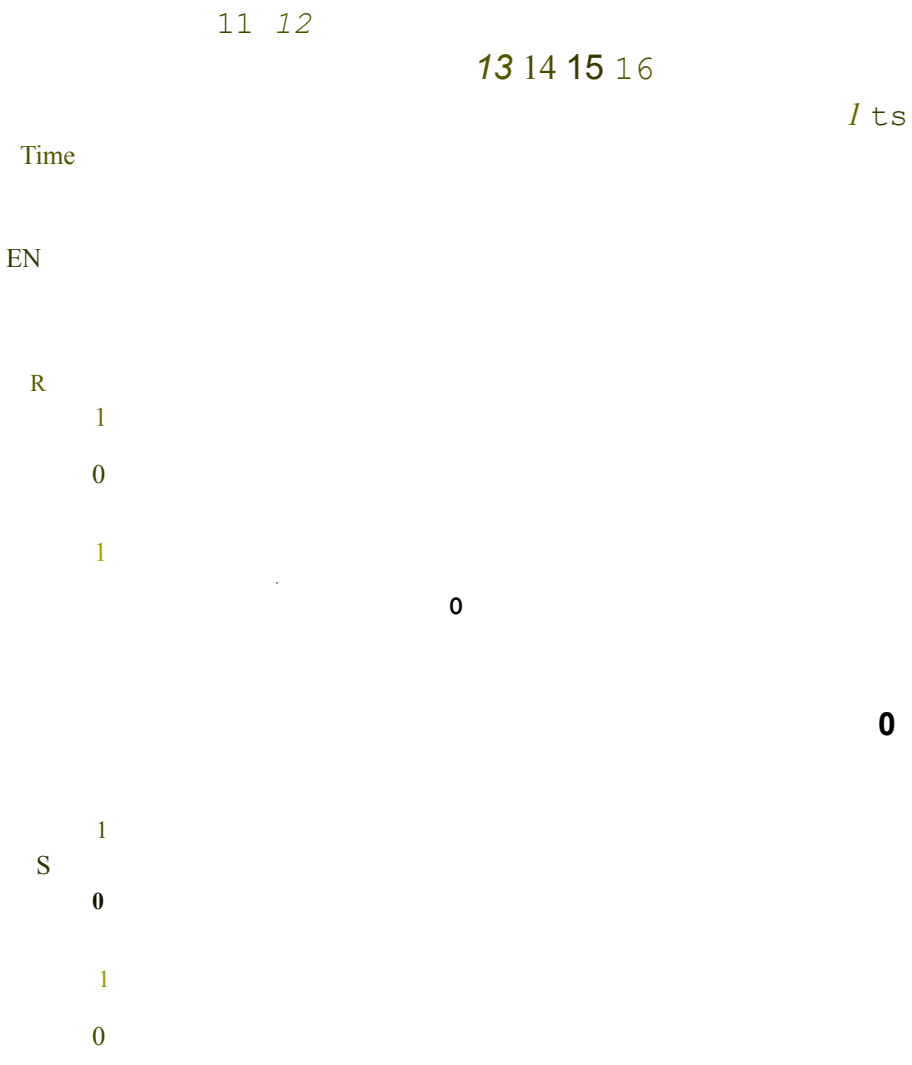
* when Enable ipp is now, the AND gates *are* both low and the latch is disabled.

to when Enabla elp is high, the latch ф

is enabled and the information at R and s ipps will be transmitted directly to the o/ps.

*

The o/p in the table is Qn+1 as two instants of time have to be considered.



Limitations

g

0

1

RS *FF*

* RS FF has 2 data ips. Creviation of 2 signals to drive FF is a disadvantage in many applications.

Yo The forbidden state of both SAR

high may occur in advestantly. to These have led to D-FF (Delay) Data) a eket. That needs only a single dalá

i/p.

A

EN

xo

EN D

o

ابركها

xo

S= |

R =O Q

Qntl

Qn

子

EN

1

when

xo

1

0

1

EN is low, irrespective

of D,

Q will remain latched in lait state.

* when EN is high, l lakes in the

бо

last value

A 4–bit Register using 1 Flip-flops

23=0

D2=1

DFO DO

F

clock

D

EN

D

Q

Q

lo

Q

EN

100

Q Q

D

EN

6

10

T

Q=0

Q=1

A3

R

* Four D flip flops are driven by a single clock signal.

* when clock is high, ilp data is loaded into the FFS and appears at the o/p.

* when clock goes low, the o/p retains the data

83

)

The waveforms in Fig. 8.51 drive a *D* latch as shown in Fig. 8.15. What is the value of *D* stored in the flip-flop after the clock pulse is over? D= Q=1

ооллол

CLK

Q

a

Edge triggered latches (FFA):

Ton

Toff

clk

tve edge

1

-ve edge

саде

A positive pulse

ə

Frive edge

-ve edge négative pulse

CIK

(2508)

|PT/NT

Pulse

forming

cft:

PTS

NTA

* In the latches with enable i/p *(RSND)* the latches respred to the data w/ps only when the enable i/p is activated.

4 In many digital

applications, howe

*

-

vel it is desirable to limit the

responsiveness of the ckt.

to a very short period of

time instead.

of

the

A

entire duration

that the

J enabling i/p is

activated .

A This meltrod of enabling the cht is called as "edge triggering where the circuit's data *ilp*s have control only during the time that the enable i/p is transitioning from one state one state to another.

Positive edge triggered Rs FFS

s.

s

62

s

Q

clk

PTS

R

Q

Q

R

Clk

PT

سی

tve edge
triggered

FF

Q

сти

IR

Q

-ve edge triggered

FF

CSR

SR) Qutl

On (hast thate)

1 0 1

?

(illegal)

0 (RESET)

10 | (SET)

* The AND galés are active only while the *PT(*postive traclition) is high (narrow, around 2500) and thus & change state only during this short time period i..., FF is transparent only during PTS

C

PT

13

R

Q

ঙ৲ন৮

D

[お]

01

1

0

-ve colge triggered

RS FF

乚

C

PT

S

R

Q

to

0 !

$3

D

Edge triggered

FEA

D

S

Q

TO

D ANTI

C D

O x Qn

ox

0

PT

个

T

1

CIK

R

* when clock is low Q is latched in *its* last state.

PRESETA CLEAR

signals.

D

PRESET = X,
0

o

S=XO Q

PT

CH
K

R=X1 Q

CLEAR
=X".

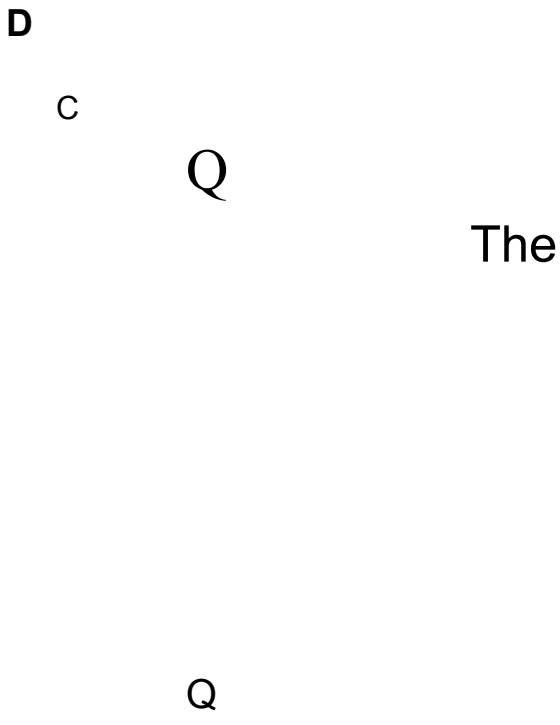
* when power is applied, FFX come up

in random states

It is necessary

in some digital systems to clear or preset certain FFS.

* PRESET and CLEAR are called asynchrous ipps because they activate the FF indepent of clock.



The

Q

D

C

Q

Q

the edge

triggered

Edge higgered Jk FPA

agdiv

e

low

re edge

CLEAR =

x

R=S=1

in

ou edge triggered RS

FF

frees both & and a to the same

logre

level

1

which is

an

illegal condition.

it is not possible to predict the

final state

of Q for this ilp

condition.

Yo The Jk Ff accounts for this illegal ilp.

Y

The JK FFA are ideal elements to

build counters.

c

tve edge triggered. Jk *FF*

Jol

PT

S=1 Q

Q-0

%

反

Q =

X

R=D Q

o

k = 1

(s)

(R)

c

J K

κ

Qutl

れ

0

。

Qn (last state)

。

0

(RESET

)

个

"

10

I

(SET)

en

(Toggle)

* The cross coupling from opps to ilps

*

changed the RS FF into a Jk FF.

when J=K=0, both AND gates are disabled & clock pultes have no Q retains its old value.

effect

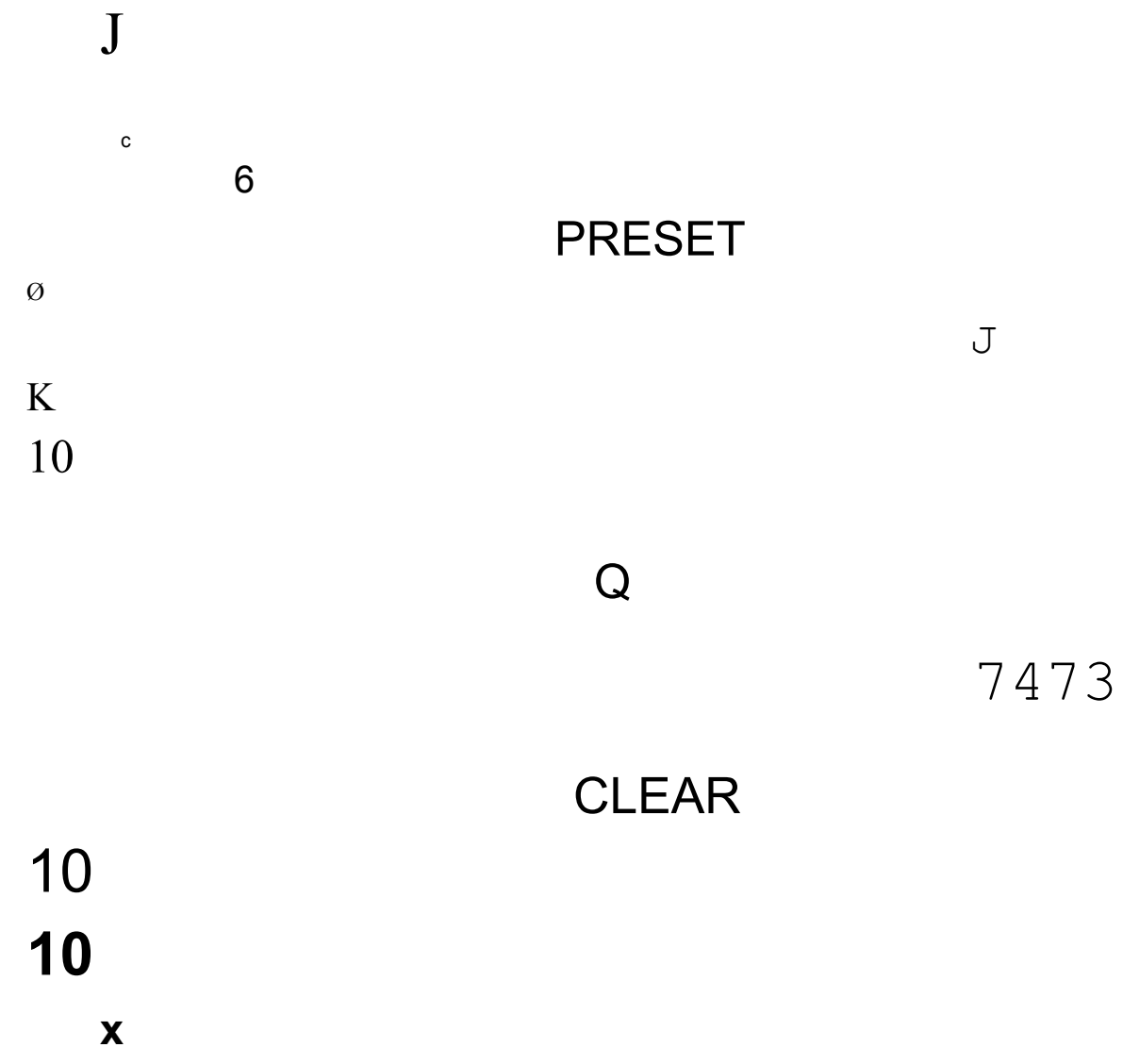
when J=op

J=op k=1, the upper gate is way to set the FF. 'If Qué high, the R ilp is enabled

disabled, so

there's no

in the +ve edge of clock, hence & becomes how .



Q

7476

* Characteristic equations

– These are useful in analysing the circuits made *of*

FFX.

1

2

(s) (R)

Qn J

○

д

○

(Qn)

ə

1

1 (an)

S

7

3

4

ə

'I (en)

5

0 1

0

6

T

(ăn)

J tant!

oo

Ди

01

ə

1

111 Qn

(toggle)

Qn

o

Quts = {m

(3,3,4,6)

JK

00

อา

TO

อ

Qnt) =

+

D-FT

Qn

D Qn+L

0

Qn+

\

Qn Dt QnD

n

Qn+1 =

D(+R!)

Qutí

Qn41 =D

RS FF

Qn S R

oo

ooo

Qutl

o

SRI Qutl

Qn

υ D

10

?(x

)

Qutí

{(2,4,6)

+dc (3,7)

00 01 **11**

TO

0

2

4

d my w

o

10

1

e

l

oo

1

SR

0 1

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Qn

6

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0

X

71

Qnxl

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St &

nŔ

X