

Unit 2

Multiplexers Data selector

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(n:201

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3:1

MUX

olp

Y

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M

control signals/
selection line's

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no.oj

2

* 2 selection lines $\rightarrow \rightarrow$ no.
of ifps = 2 = 4 [4:)

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only one

o/p .

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many

ilps but

*** By applying control
signals/selection
signals**

,

the *o/p*

we can steer any

input line

m selection lines can select the m .
of 2^m input signals.

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To design and
implement

4 : 1

multiplexer

signals, so you

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olp y

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4:1

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5, So => 22 = 4

ilps

case 1: if (5,52

=00 case 2: xf 5,

5, = 01

case 3;

Case 4 ;

$Y =$

$$1 = 10)$$

$$y = 10$$

$$Y =$$

$$y = ig_{яд}$$

$$= 11, \quad Y = dz$$

s, so iots, solits, solz
+5,52%3

*ckt. using NAND only

$$y = s_1 s_2 s_3 + s_1 s_2 s_3 + s_1 s_2 s_3 + s_1 s_2 s_3$$

=

$$(s_1 s_2 s_3 + s_1 s_2 s_3 + s_1 s_2 s_3 + s_1 s_2 s_3) \cdot (s_1 s_2 s_3 + s_1 s_2 s_3 + s_1 s_2 s_3 + s_1 s_2 s_3)$$

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2 : 1 **Мих**

21

So

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So

Y = soest Soli
y

60

y

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**Design 8 : 1 Mux using
4:1 × 2:1 Mux. Use block
diagrams.**

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8;1

Y

$$5, 5, 50 \overset{3}{\Rightarrow} 22 = 8;\text{ps}$$

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Y2

$$2 : 1$$

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3) Construct a

16x1 Mux with two

8x1 and one

2X1 Multiplexers

Use block diagrams.

- Assignment

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4) Full adder implementation using dual 4:1 Mux (74153 IC)

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4:

74153

selection

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$5 = \{(1, 2, 4, 7)\}$

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$\{ (3, 5, 6, 7) \}$

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