Regist as

* Registers and counters are important applications of clocked FFS.
* The FFS used to construct registers are usually edge- triggered JK, SR & D types

y

* A collection of FFA in cascade a register.

is called

* shift registers are capable of moving or shifting the data stored in their flip flops in either direction.

* shift regiaders that can shift data in both directions are called bi-directional register. *

Based on how the data is *ilp*

or

o/p is retrieved there

are several types of

registers like serial in paralled out (SIPO) serial in serial out (SISO) Parallel in serial out (PISO) and parallel out (PIPO)

Parallel in parallel

4-bit SISO/SIPO/Circular shift

QA

o

QB

=0

o

Serial,

D

Q

D Q

in

(Sin)

A

B

10

Q

D

B

&

Sout

el

clock

Sin=

1/0

0

Л

Л

clockly

sin

Q.

Ав

ac

ə

QC QD

(Sout))

o

o

do

o

1

0-

الد

o-

o

25

Зл

J.

Circular shift

Sin

QA QB

Oc

Q

o

वेददव

O

O

ло

o

Dips of each FF is connected to & o/p of the previous stage

* when clock is applied to FFA,

The data

Д

Serial-in (Sin) line

at

gets stored in FF A + appears

QA

SIPO

* Once the 4-bit data is shifted in after 4 clock cycles) pulses, the data stored in each FF is

&%/

ps available at the
respective & o/ps

Circular streift.

* Connecting the
o/p of

last FF
(ie,

2) to Sin circulates the
data/bib among FFS

connected in cascaded

Sin

manner

PISO/PI

PO

QA

P=1

aB

จ

D=1

D=

Q

B

ع

B

c

1

D= 1 Q

D

shift/

lood

* The liel ilps are PA,

PB, PC X PD and

o/ps are

are

QAI

QA, Q B, Qc

X Qo.

3,

* The Q o/Ps of A, B & C are connected

olpo

to D ilps of B,CxD, respectively, through

upper AND

gate.

|=

performs shift

shift / load = 0, pelforms

llel load

Do If shift load i/p =

1

*

*

shift | Lood = 1, all

upper AND galis are

enabled and sin appears at D i/p of FF A.

for PIPO / PISO where ilps have to be loaded in parallel, shift/**Load=0**.

рая

Then lower and gates are enabled

pel ilps (Pa, PB, Pc, Po) now appear at лес the respective 'D' ilps thereby facilito

+ jjel -

ting jel ijp fiel

ojp

هار

ت

* For PISO, shift | load = 1, Sin is loaded

Ri

into FF A, QA →FF B, QB7 C, Q→

Sout

Ring

counter state

table

ɣ

alk (in) Qo Q,

Qy

○

o

B3

○

Initiall

y

shiff

दद

ele

MC=!

gnd

Sin

مرد

=P,

10 =

12

D

2

3

9

5

0

7

8

-OT

مبو

14

10

9

13

I 2

0

た

2

Q2

Q3

cc

et

11 ops

Johnson

Counter

EP, (Serial
(UK)

·ER

(11el

4k)

ак

To design ring counter.

(1000)

Step I

- parallel load

1. set MC=1

connect cl signal

1.0.0.0

to CPs, set Po, P, P2, P3 to 1, 0, 0, respectively

2. Apply clk. 20=1, &=0, 2=0, 8=0

сек

Step2 shift

сли

1. Set MC=0, Cilk to CP,

This

do

transfers sin to Ro, Q

& &,,

Qz x Qz to Qz (right shift)

Twisted ring counter / Johnson

Q1 2

Ring

Cle

بر

Lysin)

as a

Q

Q

1

Q

3

o

7 step I Enifal

load (shift)

Is

stepa

3

4

0

o

Johnson
Counter

Initial

1

2

3

5

Ь

حمله که مه

ɔ

○○○

0

1
O

y (sin)

Qo a

O

O

д

1

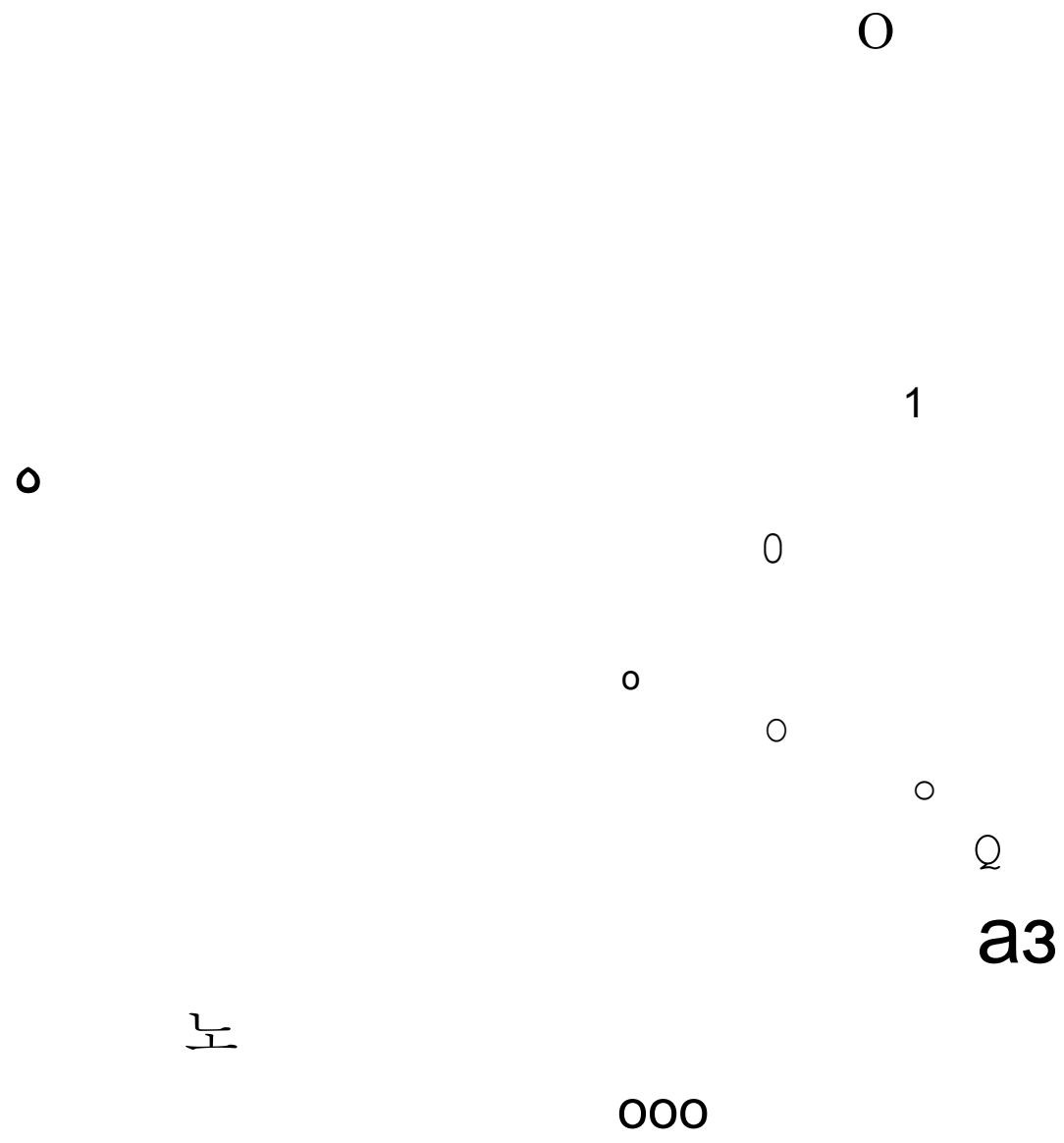
ㅇ

사

ㅇ

ㅇ

2



Universal shift register

QA

QB

oc

clear

сек

DA

A

OA

DB

B

ल

Dc

.

c

Do &

D

a,

BO

Sin

`4:1`

dodidad3

for shift

right

`4:1` `ilpa,` do

action

do

di

4:1

a

4 : 1

4:1 ao **do**

didz dz

leo

dodidads

Gogod,
dads

'P3

P

'Po

sin

HOLD

for shift
teft

ɔ

0

1

Shift Right

de

10

shift left

d3

1

yee

load

shift right: Sin -> QA > Qq

→ QcQD

QA & QBT QT Qot Sin

शुर

*

* A universal shift register is me
which is bidirectional and has
capabilities to accept both serial

and parallel ilps as well as capaki lities to serial and parallel olp.

do

of MUX is

selected. * when a, 90=00, The Q 0/0 of the FFA get connected to their respective D ilps and on application of clock pulse, these D ips appear at the respective ofps i..,

there is

д

no change in register content

when Q, 90=01, d, of Mux is selected. Sin of shift reg. gets connected do DA of

FFA Да з

Further QA, QB, Q get

connected to Df, Dc X DD, respectively

DB

through d, of MUX.

shift reg. ready for shift

right upon application of

clock pulses.

is

thre

to when

a12 = 10,

10,

da

of

MUX is

selected where in shift left

operation happens. QD, QC, QB get connected to

اد

QcQB

Dc, DB, & DA,

respectively

selected. Po, P,,P2 * when Q, Q0=11, dz is selected.

d3

+ P3 appear at DA, DB, PC ADD, resp ectively, constituting parallel ips

and parallel o/ps.

Applications

7

Shift registers

Ring counter

1000

0100

*

0010

Johnson Counter

* sequence generator

useful in generating pattern.

a sequence

Sin

ito

1

-1011 1011 1011

Sout

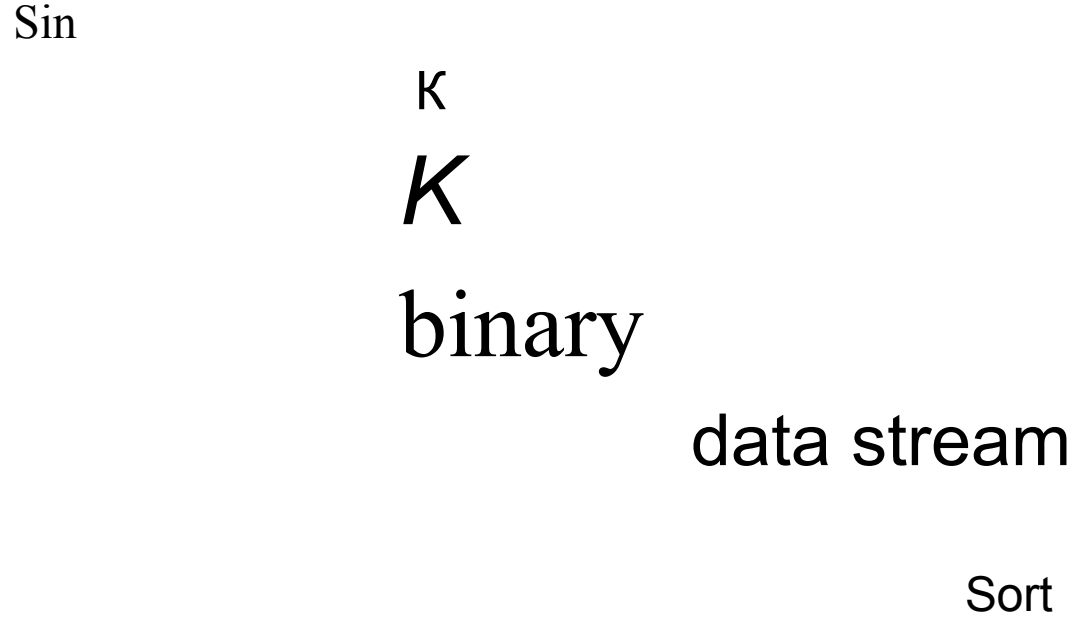
* The left mott bit of the shift register is connected to Sin and right most

provides serial data out.

* when clock is applied, data transfer takes place. Like ring counter data is not after every shift as *it* is fed back as Sin.

* Sequence defect

or




1
0
0
no
match
1 0 1
I sequence to be
detected
x
千
0

मैं
ا
1
o
O
○
ר

* Sequence defector checks kinary date Dream and generates a signal

when

detected.

a

a

particular

sequence is

* The above ckt. can detect a 4-kit

binary

sequence.

word

One register stores the kinary to be detected from the kinary olata stream.

* At every clock, bitwise comparisons

these 2 registers are done through

of

1

only

when both

EX-NOR whose *op* is ilps are same v..., 00 m 11. The

final o/p is taken from 4-*ilp* AND gate

ак

which becomes 1 only when all its ilps are 1 i.e., *all* one bits are matched.

Counters を up-counter Z down counter

Fandor

Synchronous

Asynchronous

* Design a (3-bit)

counter

43

-73 FFA

Synchronous lounters.

Asynchrono

us

Counters

500 711

* Clock applied to all FFS simultaneously

* No propagation delay

ch

* Clock is applied to the first FF,

사.

'FF

olp of porff will be

The

ud

clock lo être 2

FF

and so on.

There is propagation delay

* O/p will be

pastel

оне

*/% will be slow because of

рбора

the

gation delay

between

successive flip flops.

4 Design is difficult & Design is simple.

* Errors can be located & locating errors

earit

y

is difficult.

* Any type of counters & 2, 3, 4 kit,

com be built

Synchronous

counters

decade counters

can be built

Egl: Design and implement synchronous

mod-8 up-counter wing Jk

FFS.

8 finité states

Procedure : i) identify

the no.

✓(ii) Construct state

table

по

o

to (7)!!!

FFA:

3FFA

or 8 states

=

3

2

(ii) get the logical expressions for ips (iv) minimize

(v) implement the ckt.

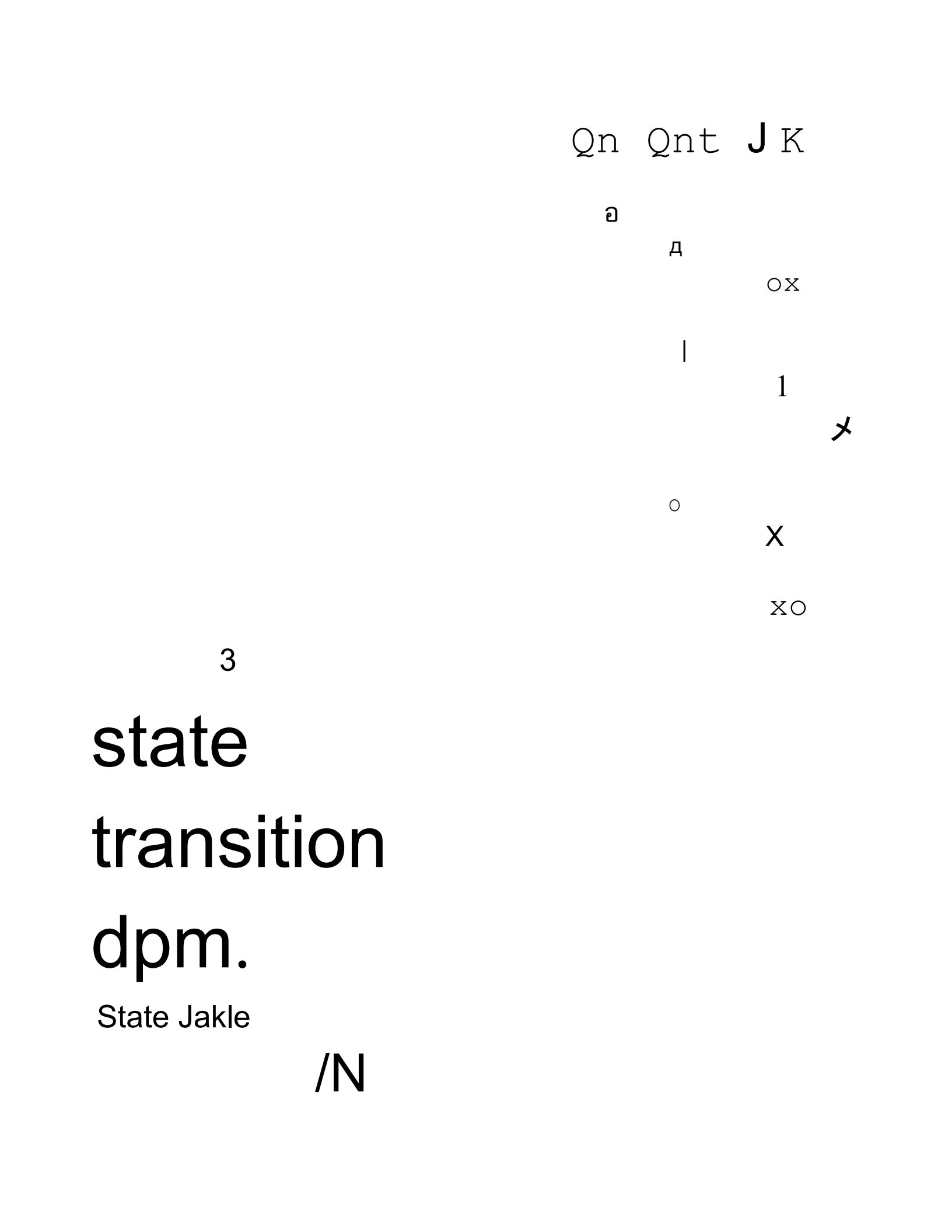
Qn

mod-8 upcounter (0–7) using Ik

Ontl

On

ɣ


Qn Qnt J K
ɔ
д
ox
|
1
メ
○
X
xo
3
state
transition
dpm.
State Jakle
/N

e

+

Present state Next state

at

Excitation table

E/PS

QA QA QTc JA KA JB

KR Jc Ke

oo

c

QA QB Qc

Iв Kв текс

9 o

x

ox

1 x

1

0

|

1

9 x

1 x ***ox***

X 1

3

न ल

2

1

1

|

1~10

ox

xo

1

x

৭

1

10

○○

Ovl 1 x

X 1

or

0 *1* X *0*

ox

1 *x*

6

7

1

1

5

0

0v
ル

1 X

x 1

(III xoxo

1 x

oo

A

RA

ac

QBQc

O

00 0|

1

10

010

1

XX

ac

JA =

Roαc

Влавас

○

5

X

0001

11 10

XЫX

2

5

XxX

J2 =

20

JB

Q &

Q C

1

B

00 01

11

To X, X3

JC=1

X

5

10

6

Ke

QB QC

IJ

0001 11

10

0 XXX2 X2

4

KA =

QBQ C

KB

QgQc

X

Xdx,

Xy

XyX1

KB =

Qc

K1 =

1

kc=

x

2

6

2

6

ak

QB

Q

СЛИ

Jo
A

KA
50

A
шма

Q
A

Iв

SD

113

ø
H

339

5

Q

KB RD

Kc RD

1

Egz: Design and implement synchronous counter using Jk FFs to count

down from

7111

do 2.

111- 3 FFA

6- finite states

3

6

Excitatio Jable

Qn Qn H J k

4

o

o

Ox

o

ما

10

X

X 1

ا ١

xo

1

QA QB

QC

Present orate Next state

+

Ja

ilps

咕

Qut at Qt JA KA JB KB

Jc kc

7

1

o

X

o

X D X 1

6

10

1

xo

x

1x

5

100

xo OXXI

4

ID 0

0 1

x 1

1x IX

3

011

010

0 x

Xo XI

xo *1x*

2

010

JB

A

DA

A

dc = {(0,

1)

00 **01**

031

хых

X 03

e

Xu X5 X 7 X6

Oc

Ja =

&c QB

QC

ac

o o 0|

11 10

2

XX, X3X2

JB = Q

c

X+X

7

DA

QB

QC

○○

X X X3 X2

X1

14 05

0=*10*

1

KA

Qa Qc

QA

квас

ƨƆ

7

6

11 10

X, TO

0.10

3

X2 07 (1

01 X5 Dy6

кв KB = QA

QC

сли

ろし

4

xox

XoX1X31

Xxx

2

J1 = K1 =

1

кс

}

6

JA =

Q

Гв

JB =

Qc

Jc="

Ka =

QB Qc

KB =

Q120

QA

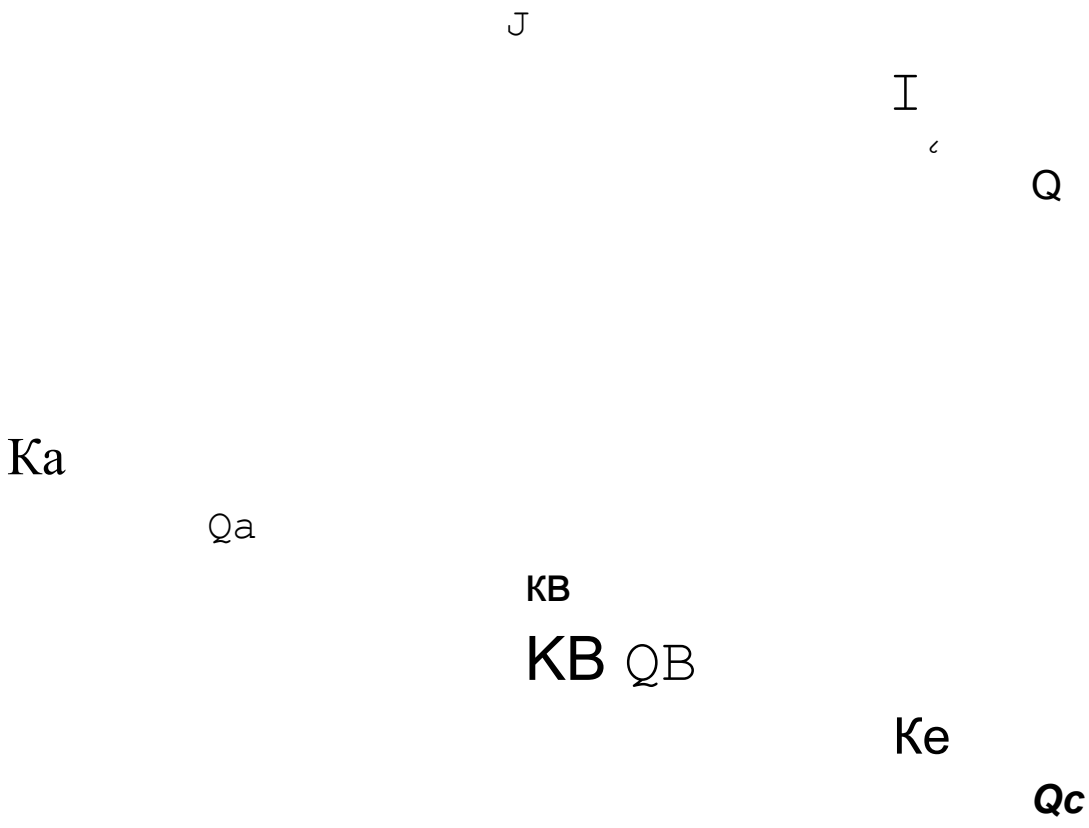
QC

кс

ѳр

ав

Q



Eg3 :- Design a synchronous

counter using JK-FF that generates the sequence 0,3, *1, 2,* 6,0

D

Use _DFF

OTB

A

Q

+

Q

P.S

N.S

QA QB QC QA

Q a te

JA KA JB PB Jc

kc

pB

e

D

оД

01

1

ox

1

x

1

メ

3

011

001

ox

X I

x

D

1

001

ого

ox

1

X

X

x 1

2

010

1 10

1 X

xo

ox

Ь

110

OOO

X I XI

ox

dc = {(4,5,

7)

JA

Q

JB =

1

да

QB

QC

00 01 *11*

00

3

е

10

2

7X6

X4 X5 X 1

JA z Qq

Q c

QBQ
C

o

JA= {(2),

'KA

Ja={(=)

$$kg = \{(3,6)$$

KB

X

01.11

xox

Kz=QA f

Qc

ка

xx

xxx

Xxx I

KA

=1

={(6)

Jc =Q

R

Kc

c

J8 = 1,

Kg =

Q12+ &c

KB

JA=QqQc,

KA=1

write the ckt. dgm. with 3 FFS

Qn Qnt D

O อ

Uring

D FE

อ

ว

+ t

DA

DB

D

1

O

P.S

N.S

QA QA Q x

QB QC Q Q

QA QB Q

C

D

OД

011

3

0 1 1

001

P

J

001

ого

○

2

010

110

6

110

oo

OOO

dc =

{(4,9,7)

○

ฮ

+Vcc

Aspichronous counters

* using clocked JK FFA

up counter :-

(0-7}, "11

B

J=1

B

J="

c

TA

©

слы

k=1

A

·K=1

B

la

K=1

* 3 -ve edge triggered Jk FiFA are connected in

cascade.

d

B

c

O

D

S

R

T.T, JK FF

ㄴ

OO

0 1

ما لا

Qn+

Q

0

колко

c

ρ

1

Initially

ABC=000

Qn

간의

Прог сук в

→

1

— СЯК С

U

○

○

С В А

до

р

ʊ

2

3

4

5

6

Д

0

до

10

7

1 11

0 to 7 counter

P

0 0 0

* System clock drives FF A, the o/p of A

olp

of

drives FFB,

B drives FF C.

* Hence called

counter.

as

asynchronous / ripple

★ FF A must change before it can trigger

pe

8 FF, and 8 FF must change state

B

B

before it can migger C FF.

* The triggers move through the FFs like

a ripple in

water.

A

X

If A is LSB and

C is MSB then

initially CBA=000

Yo At every -ve transitions

(NTA) A will

change its state

(complement of

state as

J=K=1)

.

previous

* Since & acts as elk for B, each time I waveform goes low FF B will toggle.

* Since B acts as elk for C, each time B goes low, FF C will toggle.

3-bit down counter

Asynchrono

us

A

1(25B)

B

C(MSB
)

C

XVCC

ck

сли

A

B

J

в

J

A

0

ال

کا

k

อ

○

OFT

17

c

ㅁ

ΓΓ

ہوں

c

จ

1 ○○○

7

C BA

1

6

O

5

10

ও

ওদ

s

J

লত

1

ৗ

ওদও

Note:

(i

)

-ve edge triggered → Q as clk -> up counter

(ii)

+ve

11

->Q as

ck->

→ Q as ck → up counter

>

(iii) -ve edge triggered → a as clk → down counter (iv) +ve edge siggered → Q as MK → *clown* counter

Decade counter (10 states).

how many FFS? 4

0-9

41001

mod-10

* The modulus of a counter is the total of states through which the counter

no.

лам progress.

~3-2-0-7

* A counter with 'n' FFA will have 2 olp

A

conditions.

* The largest binary

no

no. with 'n' $FFA = 2\text{-}1$