J JSS MAHAVIDYAPEETHA
JSS SCIENCE AND TECHNOLOGY UNIVERSITY JSS Technical Institutions'
Campus, Mysuru - 570 006

III Semester B.E Degree

DIGITAL SYSTEM DESIGN – CS310L LAB CYCLE

1. a) Study and verify the truth table of logic gates.
   b) Realize Basic Gates using Universal Gates.
   c) Simplify the given expression and realize it using gates.

2. Design and realize
   a) Half Adder / Full Adder.
   b) Half Subtractor / Full Subtractor.

3. Design and set up the following circuit using IC 7483. a) A 4-bit binary parallel adder.
   b) A 4-bit binary parallel subtractor.

4. Design and realize the following using Basic gates & IC 7483. a) BCD to Excess- 3 Code
   b) Excess-3 to BCD Code

5. Design and implement
   a) 4:1 Multiplexer (MUX) using only NAND gates. b) 8:1 Multiplexer (MUX).

6. Half/Full Adder and Half/Full Subtractor using IC 74153. 7. Design and implement One & Two Bit Magnitude Comparator.

8. Design and implement
   a) Decoder circuit using basic gates and to verify using IC 74LS139. b) Half/Full Adder and Half/Full Subtractor using IC 74LS139.

9. Design and implement 3 bit parity generator and verify using Parity Checker. 10. Design JK flip flop with positive edge triggering and realize its working.