Department : Computer Science and Engineering	
Course Title : Digital System Design	Course Code : CS310
Credits(L:T:P) : 3:0:0	Core/Elective : Core
Type of Course : Lecture	Total Contact Hours : 39
CIE Marks : 50	SEE Marks : 100

Course Outcomes: After completing this course, students should be able to:

CO1:	Understand the fundamental concepts of Boolean algebra, Boolean theorems, K-MAP, Quine-McCluskey algorithm and combinational and sequential circuits.
CO2:	Apply the knowledge of theoretical foundations to simplify and solve Boolean functions
CO3:	Using the knowledge of Boolean algebra and behavior, timing aspects, operation of various flip-flops analyze the combinational and sequential circuits.
CO4:	Design and implement combinational circuits, synchronous/asynchronous counters and register circuits.
CO5:	Evaluate the performance of sequential circuits using various models

Unit No.	Course Content	No. of Hours
1	**Digital Logic:** Combinational Logic Circuits, Boolean laws and Theorems , Sum-of-Products Method, Truth Table to Karnaugh Map, Pairs, Quads, and Octets, Karnaugh Simplifications, Don't-care Conditions, Product-of-sums Method, Product-of-sums simplifications, Simplification by Quine-McClusky Method.	07
2	**Data Processing Circuits:** Multiplexers, Demultiplexers, 1-of-16 Decoder, BCD to Decimal Decoders, Seven Segment Decoders, Encoders, Parity Generators and Checkers, Magnitude Comparator.	08

3	**Flip-Flops**: RS Flip-Flops, Gated Flip-Flops, Edge-triggered RS FLIP-FLOP, Edge-triggered D FLIP-FLOPs, Edge-triggered JK FLIP-FLOPs, JK Master slave FLIP-FLOP, Switch Contact Bounce Circuits, Various Representation of FLIP-FLOPs, Analysis of Sequential Circuits, Conversion of Flip-Flops.	08
4	**Registers:** Types of Registers, Serial In - Serial Out, Serial In - Parallel out, Parallel In - Serial Out, Parallel In - Parallel Out, Universal Shift Register, Applications of Shift Registers. Counters: Asynchronous Counters, Decoding Gates, Synchronous Counters, Changing the Counter Modulus. Decade Counters.	08
5	**Design of Synchronous and Asynchronous Sequential Circuits**: Model Selection, State Transition Diagram, State Synthesis table, Design equations and Circuit diagram. **Asynchronous Sequential Circuits:** Analysis of Asynchronous Sequential Circuits, Problems with Asynchronous Sequential Circuits, Design of Asynchronous Sequential Circuits.	08

Text Books:

1. Donald P Leach, Albert Paul Malvino & Goutam Saha: Digital Principles and Applications, 7th Edition, Tata McGraw Hill, 2014.
2. Morris Mano, Kim and Charles: Logic and Computer Design Fundamentals, Prentice Hall, 5th Edition.

Reference Books:

1. Donald D Givone: Digital Principles and Design, Tata McGraw Hill, 2002. 2. John M.Yarbrough: Digital Logic Applications and Design, Thomson Learning. 3. Kohavi: Switching and Finite Automata Theory, TMH.

Web Resources:

1. https://nptel.ac.in/courses/108105113/15.
2. https://nptel.ac.in/courses/117105080/19.