RAKSHIT MISHRA
Course : B.E. (Hons.), Electronics and Instrumentation, 2026
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Technical Proficiency

Coursework	Digital Design, Computer Architecture, Analog and Digital VLSI Design, Microelectronic Circuits, Electronic Devices, Signals and Systems, Microprocessors and Interfacing, Computer Programming
Skills	Python, C Programming, Verilog, Physical Design Tools (Open Source - Yosys, OpenSTA, OpenROAD), Cadence Virtuoso, Sentaurus TCAD

Education

College/School	Degree/ Class	GPA (%)	Year	Hallmarks
BITS Pilani, Goa	B.E.(Hons.) Electronics and Instrumentation	7.7/10	2026	**Top 15 in class of 140 students**
PACE Junior Science College, Andheri	Class XII – Maharashtra Board (HSC)	85.0 %	2022	**JEE Advanced Qualified**
R.N.Podar School, Santacruz	Class X – CBSE	97.4 %	2020	**Maths: 100% Science: 93%**

Work Experience

Energy Systems Analyst, Lighthouse Energy - Canada (Remote)

- Building LightGBM and NSGA-2 based ML algorithms for metric optimization and predictive analysis of key factors.
- Designing and implementing commercial-grade digital twin software and HPC systems for data center performance insights.
- Developing analytical dashboards (Streamlit) for energy modeling, facility sizing, and simulation-based validation.

Summer Intern, Lifespark Technologies- IIT Bombay (Mumbai, India)

- Engineered a 4-DOF Robotic Arm based on Control System Applications and ArduinoUNO to streamline Product Manufacturing.
- Integrated Infrared (IR) and Force Sensors to enhance environmental sensing capabilities, and increase overall system accuracy.
- Developed Control and Filtering Software using Arduino IDE, and designed a Processing Based GUI to optimize user interaction.

Projects

MIPS Processor - Verilog Implementation - Github Link

- Designed a 32-bit MIPS processor core in Verilog with a four-stage pipeline (IF, ID, EXE, WB), enabling parallelism.
- Developed and integrated key CPU Modules, such as Program Counter, ALU, Control Unit, Register File, and Pipeline Registers.
- Implemented pipelining concepts , control signal generation, and hazard detection to ensure correct workability.
- Validated functionality through simulation of assembly programs, using custom test benches for correct instruction execution.

Synchronous and Asynchronous FIFO - Verilog Implementation - Github Link

- Built synchronous and asynchronous FIFO architectures in Verilog with parameterized depth and overflow/underflow protection.
- Implemented safe clock-domain crossing in asynchronous FIFO using Gray-code pointers and double-flop synchronizers.
- Designed exhaustive, self-checking testbenches with random stimulus and formal assertions, achieving 100% functional coverage.

Phase Locked Loop - Cadence Virtuoso Implementation - Analog Mixed Signal Design

- Designed a PLL in Cadence Virtuoso, implementing all key sub-blocks: PFD, CP, LPF, VCO, and Frequency Divider.
- Applied analog/digital circuit design for schematic capture and layout, with emphasis on transistor-level design and integration.
- Gained hands-on experience in VLSI design flow, CMOS circuits, and mixed-signal architectures, preparing for verification.

Research and Publications

Research Work on Single Transistor LIF Neuron Design - Neuromorphic Compute - Computer Architecture

- Developed a single-transistor Leaky Integrate-and-Fire (LIF) neuron in Partially Depleted SOI (PD-SOI) technology, utilizing impact ionization and device-level engineering to emulate biological spiking behavior for neuromorphic computing systems.
- Modeled a PD-SOI MOSFETin Sentaurus TCAD, performing Id-Vg and Id-Vd sweeps across multiple doping concentrations.
- Validated LIF functionality with Fire-Reset Action at V =0.4V, V =1V with Drain/Source Doping = 1e20 and Channel Doping = 1e15.

Project Visio, UbiComp Workshop Paper - Electronics, IOT, PCB Design -In guidance of Professor Sougata Sen

- Research on Explainable VQA (Research Paper Accepted – MemMod4CVQA): Designed a novel model that integrates episodic, semantic, and causal memory for explainable visual question answering on egocentric data.
- Retrieval-Augmented LLM Pipeline (Software Development): Built an optimized language model pipeline with retrieval augmentation, memory-based context handling, and caching mechanisms.
- AI-Powered Smart Glasses (Hardware Project): Developing wearable smart glasses using the ESP32 microcontroller to function as a personal assistant, integrating real-time sensing, processing, and user-interaction.