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DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

A Major Project report on

"Design of Two Stage Operational Amplifier using Cadence EDA Tools"

Submitted in partial fulfillment for the award of degree of Bachelor of Engineering in Electronics and Communication Engineering

Submitted by

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CERTIFICATE

This is Certified that the Major project work entitled **"Design of Two Stage Operational Amplifier using Cadence EDA Tools"** carried out by **Praveen N Pujari, Priya S Adalli, Rakshita R Sankgond, Rakshita S Gadagi,** bonafide students of **VP Dr P.G Halakatti College of Engineering and Technology, Vijayapura** in partial fulfillment for the award of **Bachelor of Engineering** in **Electronics and Communication Engineering** of the **Visvesvaraya Technological University, Belgaum** during the year 2025-2026. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The Major project report has been approved as it satisfies the academic requirement in respect of Major project report prescribed for the said degree.

GUIDE	H.O.D	PRINCIPAL
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DECLARATION

We, students of Seventh semester B.E, at the department of Electronics & Communication Engineering, hereby declare that, the Major Project entitled" Design of Two Stage Operational Amplifier using Cadence EDA Tools", embodies the report of our Major project work, carried out by us under the guidance of **Prof.V.C.Sajjanar,** We also declare that, to the best of our knowledge and belief, the work reported here in does not form part of any other report or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this by any student.

Place:-Vijayapur Date:- 25/10/2025

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ACKNOWLEDGEMENT:

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ABSTRACT

This project presents the design and simulation of a two-stage CMOS operational amplifier optimized for implementation in 45nm CMOS technology. The op-amp comprises a differential amplifier stage followed by a gain stage, with Miller compensation employed to ensure stability and enhance phase margin. The 45nm technology node enables high integration density and improved speed, allowing for low-power operation while maintaining high gain and wide bandwidth. The design achieves a high open-loop gain, adequate slew rate, and a large unity gain bandwidth, making it suitable for modern analog and mixed-signal integrated circuits. Simulation results validate the performance, showing effective trade-offs among gain, power consumption, stability, and area. This design is well-suited for advanced low-voltage analog applications in deep submicron environments.

A two-stage operational amplifier (op-amp) is a widely used analog circuit configuration that provides high gain and wide output swing, essential for signal amplification in integrated circuits. The first stage typically consists of a differential amplifier to offer high input impedance and differential gain, while the second stage is a common-source or gain stage that amplifies the signal further and enhances the output drive capability. This topology achieves high open-loop gain, good common-mode rejection ratio (CMRR), and adequate phase margin through compensation techniques like Miller compensation. The two-stage op-amp is integral to analog signal processing, including filters, comparators, and data converters, due to its balance of performance, simplicity, and adaptability in CMOS technologies.

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CHAPTER:1

INTRODUCTION:

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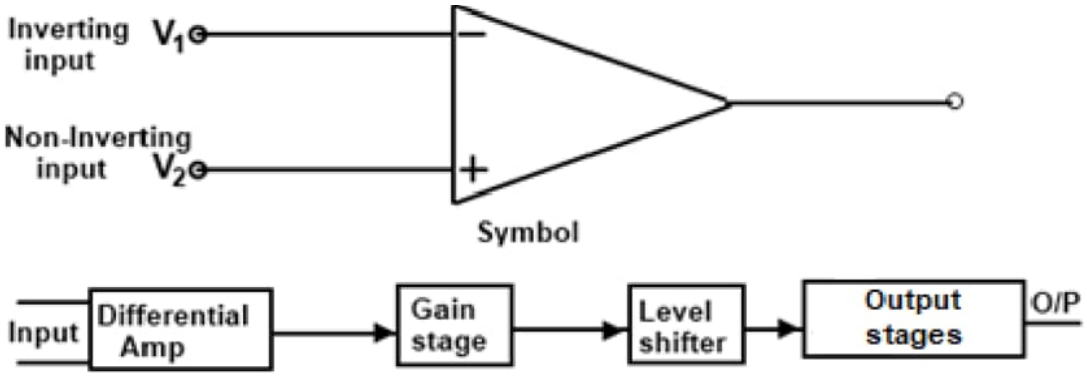
Opamp as abbreviated operational amplifiers are used to perform several operations on input signals. Operational amplifiers are usually used in 2 configurations namely inverting and non-inverting configurations. Opamp are the fundamental block of analog design they are used in circuits such as digital to analog converters (DAC's), analog to digital converters (ADC's), active filters, comparator circuits like Schmitt triggers and zero crossing detectors. The major goal of this study is to design and optimize the size of a two-stage miller compensated Opamp in 45nm node technology. The main challenge remains in the design and implementation of a two-stage Miller compensated op-amp while taking various parameters into consideration that are constraints which are interdependent upon each other. The gain of the circuit is mostly determined by the width to length ratio. The slew rate and bandwidth depend upon Miller capacitance and output load capacitance.



CHAPTER 2:

LITERATURE SURVEY:

2.1 Research studies:

1. karunya Institute of Technology and Sciences, Coimbatore:' **Design and analysis of Two stage op-amp in 180nm CMOS' -** 2024 7th International Conference on Devices, Circuits and Systems (ICDCS) | 979-8-3503- 5047-0/24/$31.00 ©2024 IEEE

This work designs an operational amplifier using adaptive biasing circuit with auxiliary circuit for high slew rate. The proposed op-amp in gives a gain of 40.09 dB, Gain Bandwidth 52.40 MHz, Phase Margin 88.86˚, Slew Rate 31.31 V/μs with Power dissipation 92.2 μW. Fully differential op-amp with high gain bandwidth and low power consumption is designed. The designed op-amp has a gain of 60.8dB, Gain Bandwidth of 2.03 GHz, phase margin 55˚ and power consumption of 2.25 mW for1.8 V.

Performance of an amplifier depends on gain, speed, power dissipation, supply voltage, linearity, noise, voltage swings, topology, optimized aspect ratio and frequency compensation. Simulation results shows that the power dissipation is 1.3mW, Gain60dB and CMRR is 48.7dB in 180 nm CMOS Process. The proposed op-amp can be used in Instrumentation amplifiers for medical applications.

- This gives 40 dB gain, 72 phase margin, 80 dB CMRR,114KHz UGBW and consumes 112nW with 0.8 V power supply.
- Slew Rate and bandwidth are less for the proposed op-amp. This work [3] analyses different current mirror loads.
- It was observed that power consumption is more for Wildar type mirroring with low gain. The Wilson mirroring in op-amp provides better flat output response.
- The Cas code mirroring circuit provides high gain, bandwidth, and CMRR with least power dissipation. It also has greater stability and accuracy and can also drive additional output stages.

2. 2nd world conference on communication and computing:' **Design Analysis of Two Stage OP-AMP and TIQ as a Comparator for Flash ADC'-** 2024 5th IEEE Global Conference for Advancement in Technology (GCAT) | 979-8-3503-7668-5/24/$31.00 ©2024 IEEE.This paper propos2es a two-step four-bit Flash ADC implementation at an operating voltage of 2V. It aims to achieve low power consumption with minimized delay and conversion time. In this design a 2 stage OP-Amp is used as a comparator. This comparator is classified into two parts. One is the biasing circuit and the other is the differential amplifier. It also demands a better gain from the operational amplifier. The W/L ratio is considered for all the transistors using the representation of 180nm technology in Cadence Virtuoso application.

The primary advantage of Threshold Inverter Quantizer(TIQ) as a comparator over Two stage op-amp is the power consumption. The TIQ dissipates power of 1.12nW which is very less as compared to that of a two stage op-amp dissipating a power of 279.2uW. If we check the noise analysis of both the comparators, then it is evident that two stage op-amp produces a noise of 9.300E-17v/sqrt (Hz) which is low a compared to TIQ with a noise of 9.721E-17 v/sqrt. Another advantage of using TIQ in Flash ADC is that it minimizes the need of Resistor Voltage Divider Network thus improve in the overall area of the circuit. Table V shows the comparative analysis of both the comparators.

- Design and Analysis of Robust Two Stage Op-Amp using 90nm CMOS Technology for Biomedical Applications: The paper proposes the study of CMOS based op-amp for achieving moderate gain and low power dissipation for medical applications.
- In the twostage operational amplifier, all the transistors are maintained in saturation region. The main advantage of using this comparator is its low offset voltage.The priority encoder is designed using ratioed logic with smaller number of transistors, which helps in reducing the cost of the circuit and low power dissipation.

3. International Symposium on Electromagnetic Compatibility: '**A Two Stage Miller OpAmp with Low Voltage Cascode Current Source with High EMI Immunity'-** 2023 International Symposium on Electromagnetic Compatibility – EMC Europe | 979-8-3503-2400-6/23/$31.00 ©2023 IEEE |

In this paper, we present intuition-based reasoning behind the EMI-induced output offset at different out-of-band frequencies. Design techniques to reduce the offset at various ranges of frequencies without overhead trade-offs are presented.

An EMI-immune two-stage Miller OTA has been designed, implemented, and validated to have comparable EMI immunity to existing state-of-the-art solutions for the two-stage OTA; without extra overheads of circuit components, power, and area. Our EMI-aware design approach reduces the asymmetry of positive and negative slew rates and mitigates the offset. Circuit implementation and layout is done using standard 0.18 μm CMOS technology. Monte Carlo simulations are done to consider process variations and mismatches. EMI induced offset is simulated in voltage-follower configuration with a range of amplitude and frequency of EMI.

- Two-stage Miller OTA, designed and optimized for certain specifications may have asymmetric slew rates, which causes the output offset voltage in the presence of large-amplitude EMI. Circuit implementation and layout is done using standard 0.18 μm CMOS technology

4. IEEE International Conference on Interdisciplinary Approaches in Technology and Management for Social Innovation (IATMSI):' **Flexible and High Throughput Designs of Operational Amplifiers'-** 2024 IEEE International Conference on Interdisciplinary Approaches in Technology and Management for Social Innovation (IATMSI) | 979-8-3503-6052-3/24/$31.00 ©2024 IEEE

This project presents flexible and high throughput op-amps that can perform multiple parallel operations using the same circuit. The operation mode is adjusted using a control line of an analog switch. With the proposed design, the throughput of the threestage op-amp with extra CS amplifiers is 50% greater than the conventional three stage op-amp design.

The throughput of the proposed three stage op-amp only with analog switches and the proposed telescopic op-amp remains the same, as they only perform one operation at a time. However, the flexibility to change the number of stages and the number outputs of these proposed op-amps is high. All the conventional existing and proposed op-amps are designed with 180nm CMOS technology using Cadence Virtuoso

5. 5th IEEE Global Conference for Advancement in Technology (GCAT):' **Two-Stage Op Amp Design and Flash ADC Implementation'**- 2024 5th IEEE Global Conference for Advancement in Technology (GCAT) | 979-8- 3503-7668-5/24/$31.00 ©2024 IEEE

This paper describes how to build a flash ADC with a ladder network reference voltage of 1.8V and L T spice tools, utilizing 90nm technology. Examined, demonstrating that the Wallace tree encoder design uses less power (910pW).

The Flash ADC is known for its top speed performance due to its parallel structure, making it ideal for applications that require broad bandwidth.

The first objective was to optimize the encoder circuit to lower the 3-bit flash ADC's power consumption. Encoders are made using a variety of design techniques, including 2:1 multiplexer-based encoders and Wallace tree encoders. It has been demonstrated that encoders for 3-bit flash ADCs constructed with Wallace trees use less power than encoders based on 3:1multiplexers. We also used a variety of design logics, such as switching logic and pass transistors.

6.Department of ECE, Sri Venkateswara College of Engineering, Tirupati, Andhra Pradesh, India: '**Analysis of Two Stage CMOS Operational Amplifier in 90nm CMOS Technology'**- 2024 Feb Volume 12 Issue II International Journal for Research in Applied Science & Engineering Technology (IJRASET)

In this design, we have satisfied all the parameters in the requirement and specially we achieved high gain values, slew rate and wide unity gain phase margin. By comparison we found that the simulation result is a little different from out theoretical design due to some omitting during our calculation. but after all, our calculation has represent t the real situation and offered great help in the design of the device. All the simulations have been carried out using cadence in 90nm CMOS process.

The complete rail-to-rail output voltage swing is achieved by operating the current sourcing transistors in deep triode region. The important parameters related to CMOS two-stage operational amplifier such as direct current gain, phase margin, settling time, power dissipation, CMRR, unity gain-bandwidth and slew rate have been calculated in 90nm CMOS technology using cadence virtuoso tool and it is verified with the theoretical values. The unity gain bandwidth of the proposed two stage CMOS operational amplifier is enhanced by varying
the widths of the operating transistors.

7.Department of Electronics & Communication Engineering Dayananda Sagar College of Engineering Bangalore: '**Design of Two Stage Miller Compensated CMOS Opamp with Nulling Resistor in 90nm Technology'**:- 2024 Third International Conference on Intelligent Techniques in Control, Optimization and Signal Processing (INCOS)

The simulation was performed in cadence virtuoso in 90nm node technology, and the system's gain and phase margin were improved by modifying the parameters (W/L) and using a nulling resistor in series with the miller capacitance. The Opamp Design has a gain of 68 dB with a phase margin of 80 degrees under unity gain configuration with a slew rate of 9 V/μSec for a voltage supply range of 0 to 1.2V, a CMRR of 84 dB, a gain bandwidth of 23 MHz, and a power dissipation of 33μW.Hence we have successfully designed a two stage Miller Compensated Opamp with high gain with relatively good bandwidth and phase margin with low bias current in 90nm technology.

CHAPTER 3:

SOFTWARE AND TOOL REQUIREMENT

Cadence Virtuoso

Cadence is an Electronic Design Automation (EDA) environment that allows integrating in a single framework different applications and tools (both proprietary and from other vendors), allowing to support all the stages of IC design and verification from a single environment. These tools are completely general, supporting different fabrication technologies. When a particular technology is selected, a set of configuration and technology-related files are employed for customizing the Cadence environment. This set of files is commonly referred as a design kit. The Cadence tool kit consist of several programs for different applications such as schematic drawing, layout, verification, and simulation. These applications can be used on various computer platforms. The open architecture also allows for integration of tools from other vendors or of own design. The integration of all this tools is done by a program called Design Framework II (DFW). The DFW application is the cornerstone in the Cadence environment. It provides a common user interface and a common data base to the tools used. This makes it possible to switch between different applications without having to convert the data base.

Cadence Schematic editor

To create the schematic the tool Virtuoso Schematic Editor is used. This editor is an interactive system for building schematics by instantiating some basic components (transistors, capacitances, etc.) and to connect them to each other. The values (properties) of the components can be edited to suit the specifications. Likewise, text and comments can also be included. In order to create a circuit in the schematic editor instances or circuit components like transistors, supply nets and wires should be added. To add an instance "T" should be pressed from the keyboard. This will open up a Component Browser. This will list all the components housed within the NCSU Analog Parts library and gives the ability to search for a specific component from the Filter. The required components can be searched and placed in the window. Wires can be added among the chosen components by pressing 'W from the keyboard and make appropriate connections across all transistor elements. This will come in very handy during simulation, especially when dealing with circuits with several components. It is often advisable to add Pin names to each of the I/O terminals in a circuit. Thus, the pins can be added to the schematic by clicking on the pin symbol and make appropriate connections across all I/O ports. The VDD and VSS pins should be chosen to be Input Output when selecting the Direction during pin creation. The final schematic editor of a sample circuit will look as

shown in fig 3.1. Further, the 'Check and Save' option will check for errors in the schematic and save the current design if no errors are found.

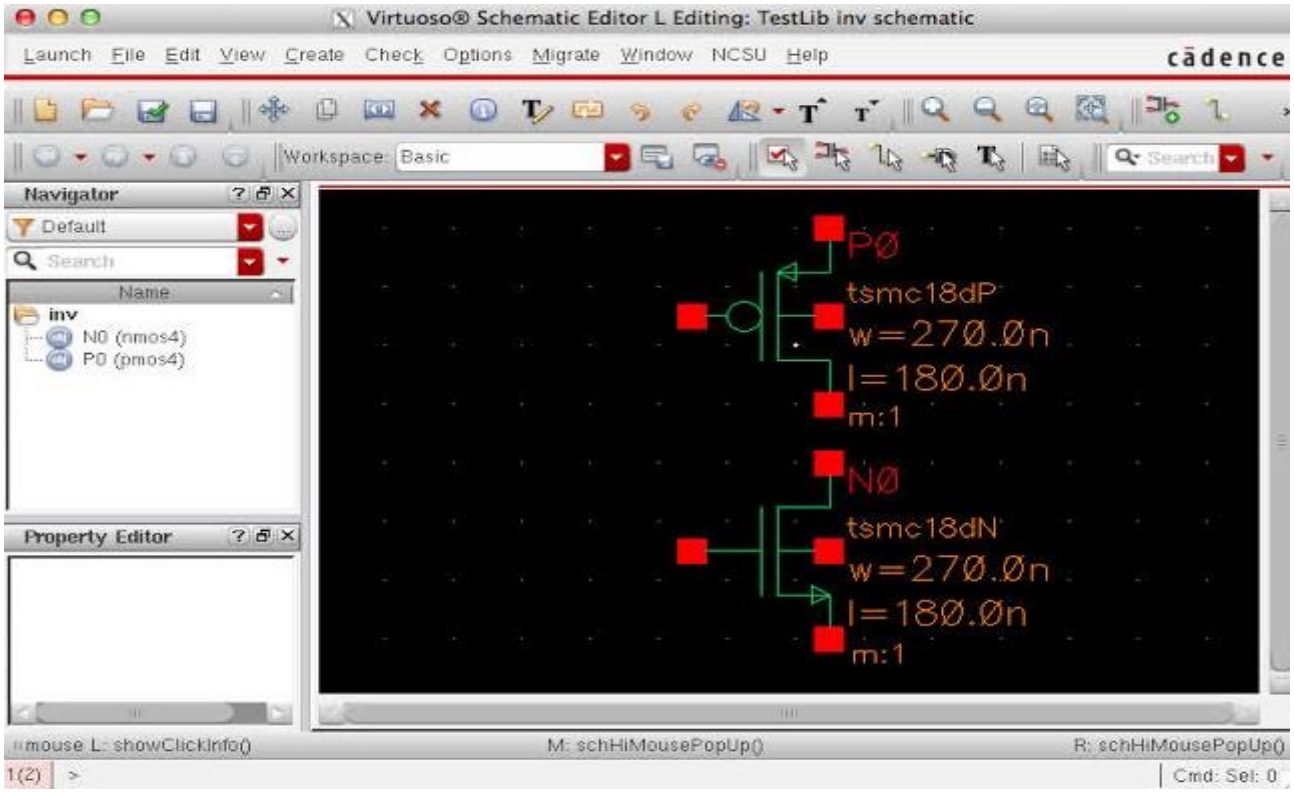


Figure 3.1: Schematic editor

Schematic Symbol Creation

The editor will also create symbols of the cells so that they can be used in other parts of the construction. When dealing with large circuits its often advisable to generate symbols for each sub-circuit in the design and perform all simulations by placing the corresponding symbols in a testbench. The symbol can be generated by creating a cell view from schematic cell view. The input and output pins in the symbol can be rearranged as per the design needs. Once the symbol is created it will popup. By default, Cadence will generate a rectangular symbol, however the generated symbol can be edited as per the user needs. After the symbols have been created the various symbols can be combined to form a Test Circuit. The test circuit can be fed with a suitable input in the form of transient pulse or any analog signal along with a required DC supply. These test circuits can be checked for its functionality by performing various simulation analysis like Transient, DC and AC analysis. The symbol editor window.

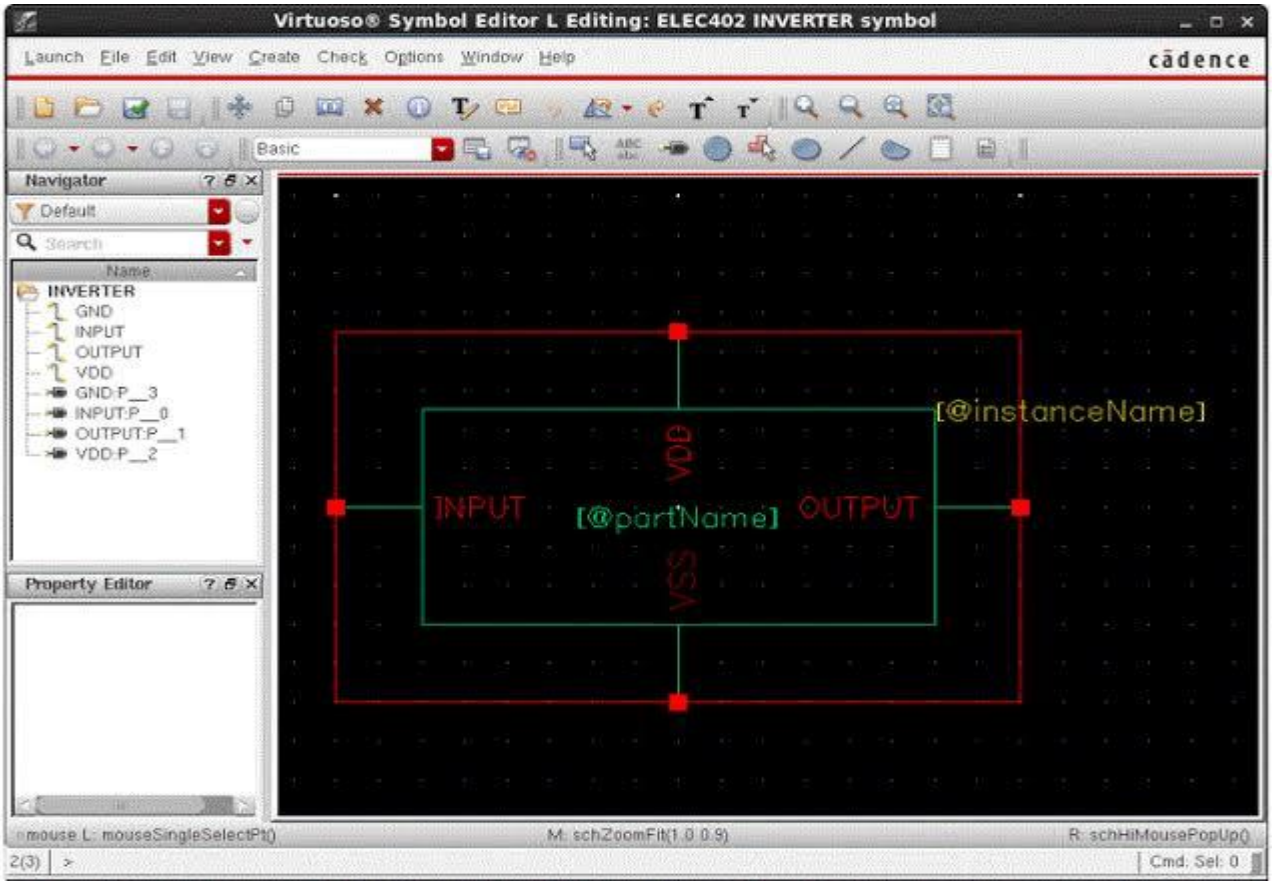


Figure 3.2: Symbol editor

Virtuoso Analog Design Environment

Virtuoso Analog Design Environment L is the entry-level analog design and simulation environment for the Virtuoso custom design platform. Analog Design Environment L is the industry's leading task-based environment for simulating and analyzing full custom, analog, and RF-IC designs. It features a graphical user interface, an integrated waveform display, distributed processing, and interfaces to popular third-party simulators.

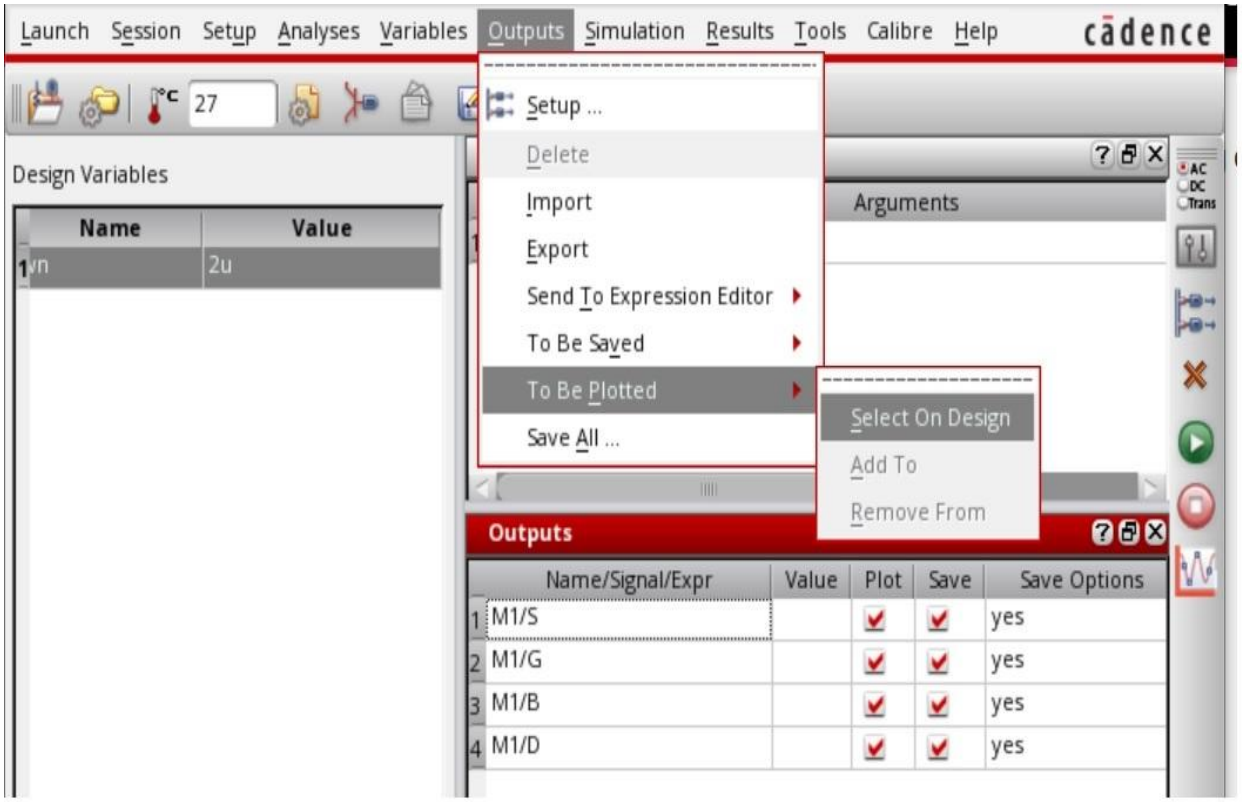


Figure 3.3: ADEL Window

1.Introduction to ADEL: ADE L (Analog Design Environment – L) is the basic simulation environment inside Cadence Virtuoso used for analyzing analog and mixed-signal circuits. It provides a graphical interface that helps designers perform simulations without manually writing SPICE code. ADE L is mainly used during schematic-level design to verify circuit functionality and performance.

2.Setting Up Variables and Inputs: In ADE L, designers can define variables such as supply voltage, bias currents, device dimensions, or input amplitudes. These variables make the simulation flexible because you can change values quickly or sweep them across a range. ADE L also allows you to assign input sources to your circuit so that different test conditions can be applied easily.

3.Selecting Simulation Analyses: ADE L offers several types of simulation analyses that help designers understand circuit behavior. Common analyses include DC operating point, DC sweep, AC analysis, Transient analysis, and Noise analysis. Each analysis provides specific insights—for example, AC analysis gives frequency response, while transient analysis shows time-domain waveforms. All these analyses are selected using a simple menu.

4.Running Simulations with Spectre: Once the setup is complete, ADE L uses the Spectre simulator to run the required simulations. Spectre calculates voltages, currents, and device operating regions based on the circuit schemtic. ADE manages the simulation process and ensures that results are stored properly for viewing and measurement.

5.Viewing Results and Waveforms: After simulation, ADE L provides tools to view outputs like node voltages, currents, waveforms, and frequency responses. You can also check transistor operating points to verify whether devices are in saturation, cutoff, or linear region. The results can be displayed in graphs or tables, making analysis easier.

6.Performance Measurements and Expressions: ADE L allows the user to create expressions to measure circuit performance automatically. Examples include gain, bandwidth, power consumption, phase margin, or delay. These expressions help designers validate the circuit against specifications without manually calculating values every time.

7.Corner and Parametric Analysis: ADE L supports sweeping variables and running design corners such as TT, FF, SS, FS, or SF. This helps designers understand how the circuit behaves under different process, voltage, and temperature (PVT) conditions. Parametric sweeps allow the user to analyze the effect of changing one or more design variables.

Layout:

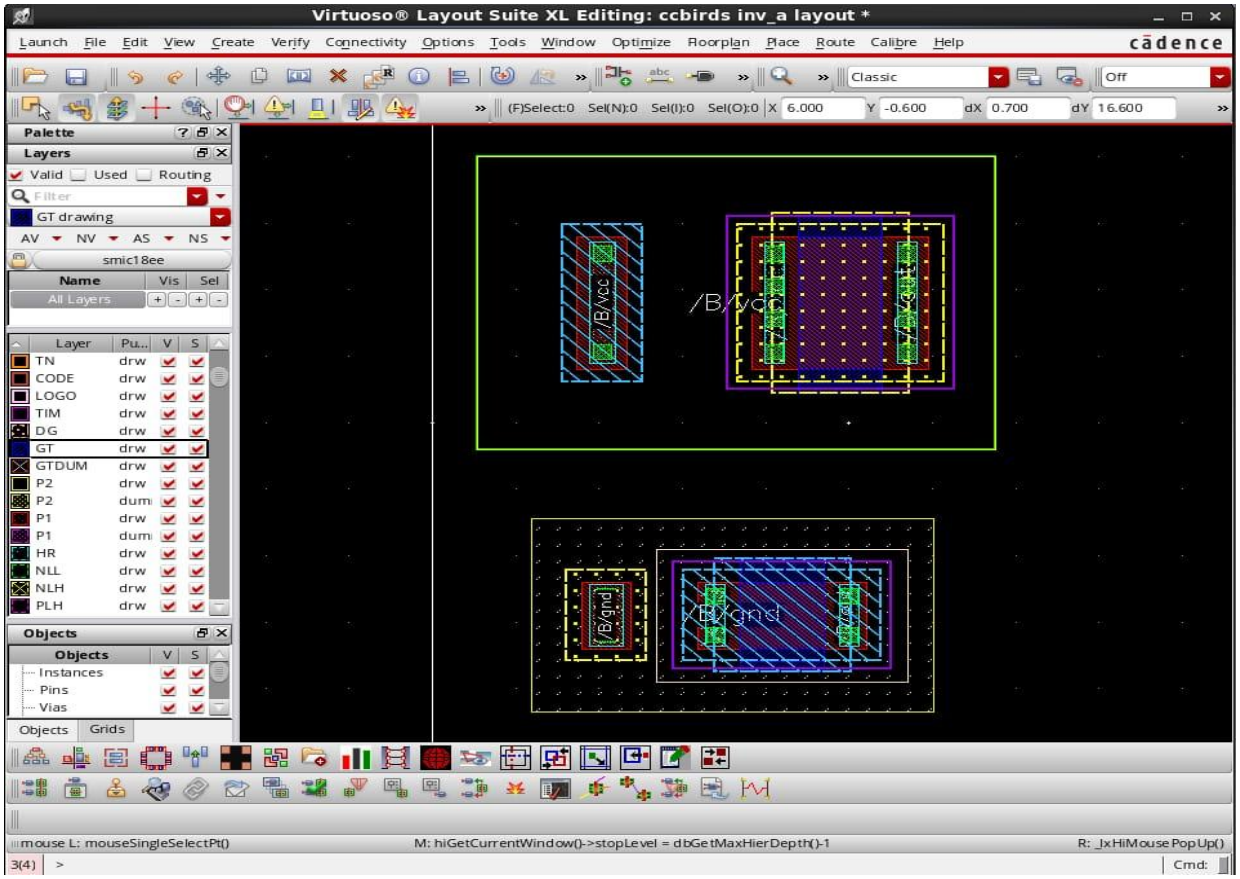


Figure 3.4: Layout XL

1. Introduction to Layout XL: Layout XL is an advanced layout environment in Cadence Virtuoso that helps designers create physical layouts linked directly to the schematic. It is mainly used for custom IC layout, where accuracy, matching, and design rule compliance are critical. Layout XL provides intelligent features that make layout creation faster and more error-free compared to the basic layout editor.

2. Schematic-Driven Layout (SDL): The most important feature of Layout XL is Schematic-Driven Layout. This means the layout is directly connected to the schematic. When you open a cell in Layout XL, it automatically reads all schematic devices, pins, and connections. You can use the "Generate All From Source" option to place devices and create connections based on the schematic, reducing manual effort and mistakes.

3. Assisted Device Placement: In Layout XL, devices such as transistors, resistors, and capacitors can be placed easily because the tool recognizes their parameters from the schematic. It shows you which components are placed and which are pending. This makes it easier to maintain matching, symmetry, and proper orientation—important in analog layouts.

4. Connectivity and Routing Support: Layout XL automatically highlights nets and connections from the schematic. When you select a net, the tool shows the required connections in the layout using flightlines. It also supports interactive routing, auto-routing suggestions, and features like stretch-wire and via generation, which simplify metal routing.

5. Design Rule Checking (DRC) Assistance: The environment continuously checks for layout violations such as spacing, width, enclosure, and overlap errors. Layout XL gives real-time DRC feedback while drawing shapes or routing. This ensures the layout is always DRC-clean or close to clean, reducing time spent fixing errors later.

6. Layout Versus Schematic (LVS) Preparation: Since Layout XL is schematic-driven, it ensures layout connectivity matches the schematic. The connections and device parameters are easy to compare before running LVS. The "Check Against Source (CAS)" feature helps you verify missing connections, wrong device placements, or mismatched pins before final LVS checking.

7. Parameter and Property Synchronization: If the designer changes a device parameter in the schematic (e.g., transistor W/L), Layout XL shows a mismatch notification. You can then update the layout device parameters to maintain consistency. This reduces human error and keeps both schematic and layout synchronized.

CHAPTER 4:

METHODOLOGY:

The methodology of a two-stage operational amplifier (op-amp) involves the design and analysis of an analog amplifier that provides high gain, large output swing, and good frequency compensation.

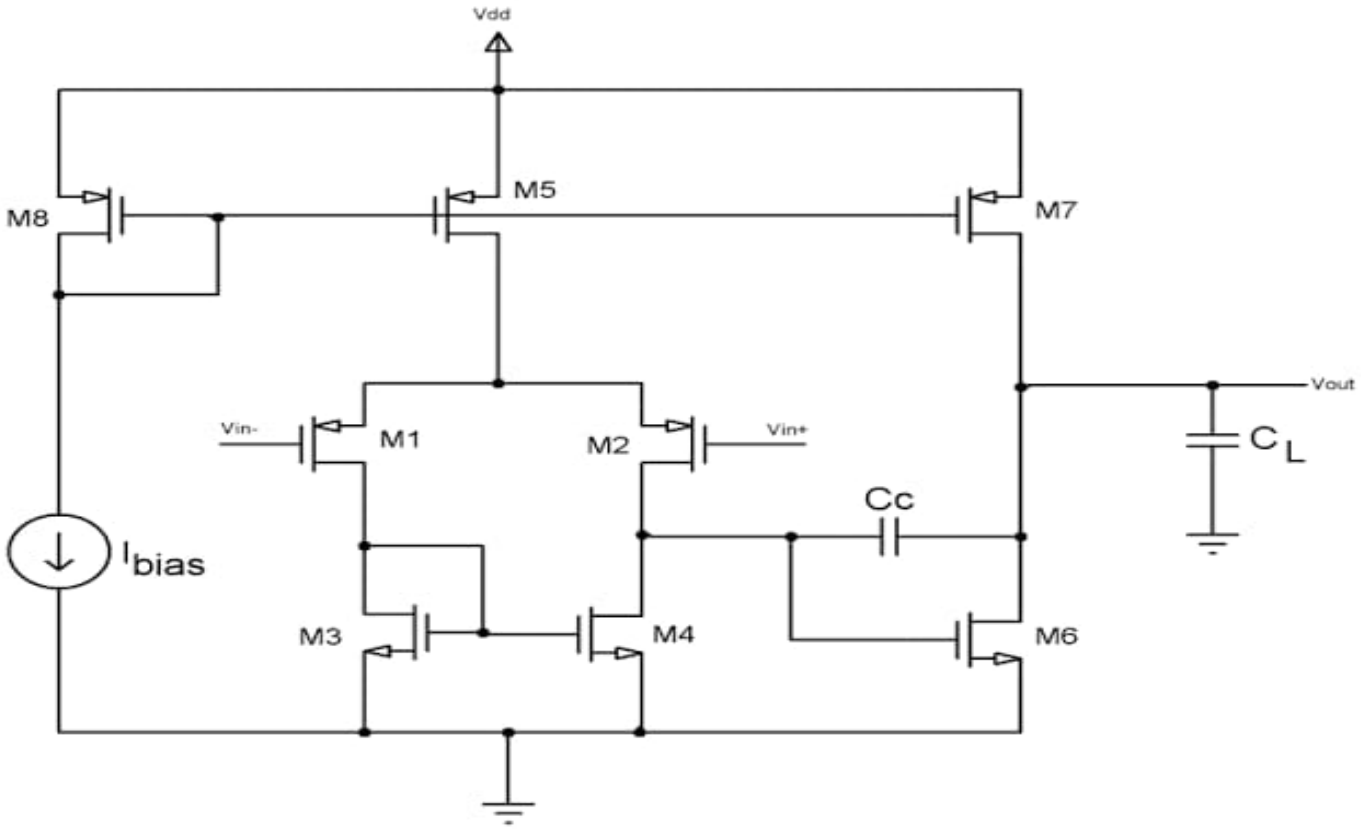


Fig 4.1: Diagram of two stage operational Amplifier

The two-stage op-amp architecture consists of two cascaded amplifier stages: the differential amplifier (input and the gain stage. The differential amplifier performs the crucial task of amplifying the voltage difference between the input terminals, while the gain stage provides additional voltage gain. This configuration offers several advantage over single-stage op-amps, such as higher gain, improved bandwidth, and increased output voltage swing.

Design Considerations: To design an efficient and high-performance two-stage op-amp, certain key consideration must be taken into account:

a. Differential Amplifier: The differential amplifier is responsible for amplifying the voltage difference between input terminals. It is typically implemented using transistors, such as MOSFETs or BJTs, configured in a different pair arrangement. Design parameters such as biasing, transistor sizing, and load configuration need to be careful optimized to achieve high gain, low offset voltage, and improved linearity.

b. Gain Stage: The gain stage provides additional voltage gain to the signal amplified by the differential amplifier. designed to have a high gain and wide bandwidth while maintaining stability. Common configurations for the gain stage include common-source (for MOSFETs) or common-emitter (for BJTs) amplifiers. The choice of active device and load configuration influences the overall performance of the gain stage.

c. Compensation: Two-stage op-amps require compensation to ensure stability and prevent oscillations. Techniques such as pole splitting, Miller compensation, and frequency compensation capacitors are employed to achieve stability without sacrificing bandwidth. The selection and placement of compensation components play a crucial role determining the overall stability and phase margin of the op-amp.

d. Performance Characteristics: Two-stage op-amps exhibit several performance characteristics that determine their suitability for specific

Applications:

a. Gain and Bandwidth: The gain of a two-stage op-amp is primarily determined by the gain of the gain stage, which can be significant higher compared to single-stage op-amps. The bandwidth of the op-amp is influenced by the individual bandwidths the differential and gain stages. Careful design considerations can yield two-stage op-amps with high gain and with bandwidth, enabling them to handle a broad range of signals.

b. Slew Rate: The slew rate of an op-amp defines its ability to respond to rapid changes in the input voltage. Two-stage op-amp with appropriate sizing and biasing of transistors can achieve high slew rates, enabling them to handle high-frequency

c. Power Consumption: Two-stage op-amps typically consume more power compared to single-stage op-amps due to the presence of multiple amplification stages. Power efficiency is an important consideration, especially in portable devices and low-applications, where trade-offs between gain, bandwidth, and power consumption need to be carefully evaluate

The steps for the to two stage Operational Amplifier are:

1.Simulation: Simulating a two-stage op-amp involves using Cadence tool and analyze the behavior of the amplifier circuit. This process allows to predict the performance characteristics of the op-amp, such as gain, bandwidth, and stability, before fabricating the device.

2.

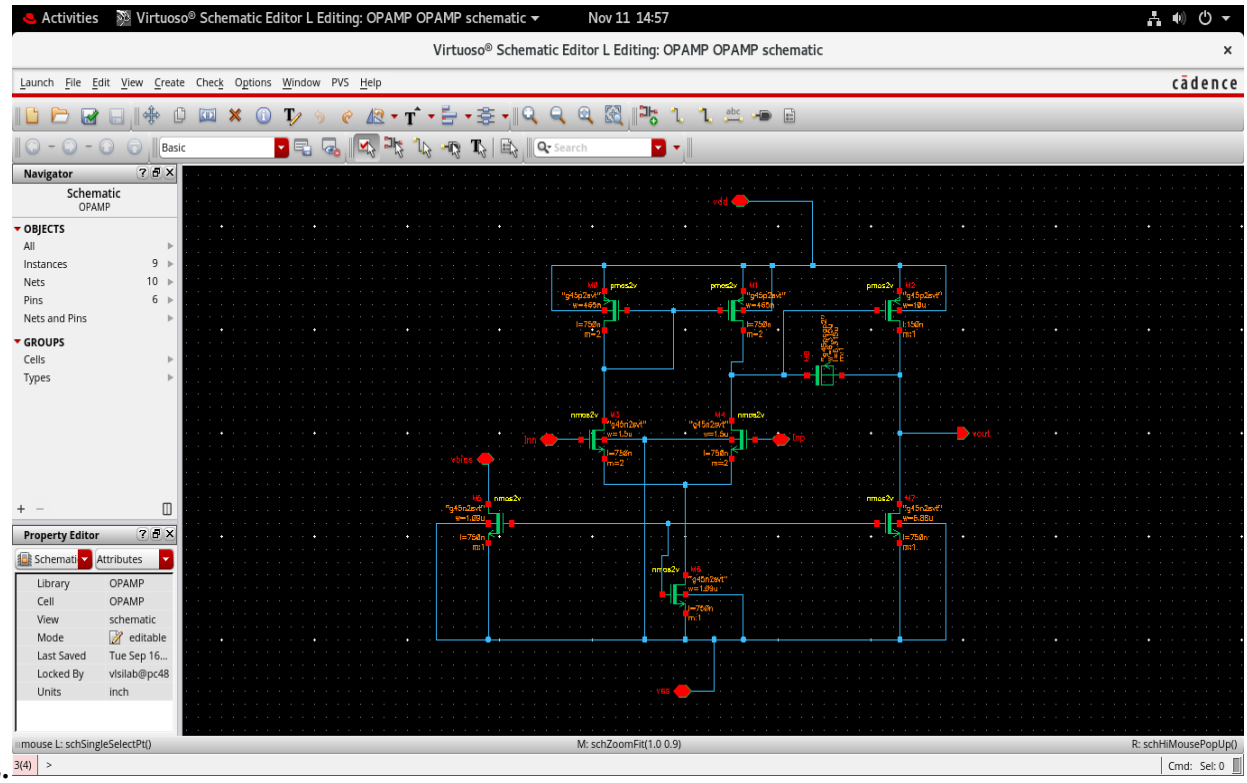


Fig 4.2: Simulation diagram of two stage op-amp using cadence tool

The schematic shown in the Cadence Virtuoso environment represents a two-stage CMOS operational amplifier (Op-Amp) designed using a 45nm technology node. The circuit consists of two main amplification stages. The first stage is a differential amplifier formed by a pair of NMOS transistors connected to the inputs Vin1 and Vin2. These transistors share a common current source controlled by a bias voltage Vbias, which sets the tail current and ensures stable operation. The outputs of the differential pair are connected to a PMOS current mirror that serves as an active load, enhancing the gain of the stage.

The second stage is formed by an NMOS transistor that receives the amplified differential signal and further drives the output. This stage includes a PMOS load and provides additional gain. To ensure frequency stability and to avoid oscillations when negative feedback is applied, a Miller compensation capacitor is used between the intermediate node and the second stage input.

3. Creation of the symbol:

The creation of an op-amp symbol using a two-stage op-amp involves designing a schematic representation that includes the two input terminals, the output terminal, and the voltage supply terminals.

This symbol visually represents the core components and connections of a two-stage op-amp, aiding in circuit diagrams and analysis.

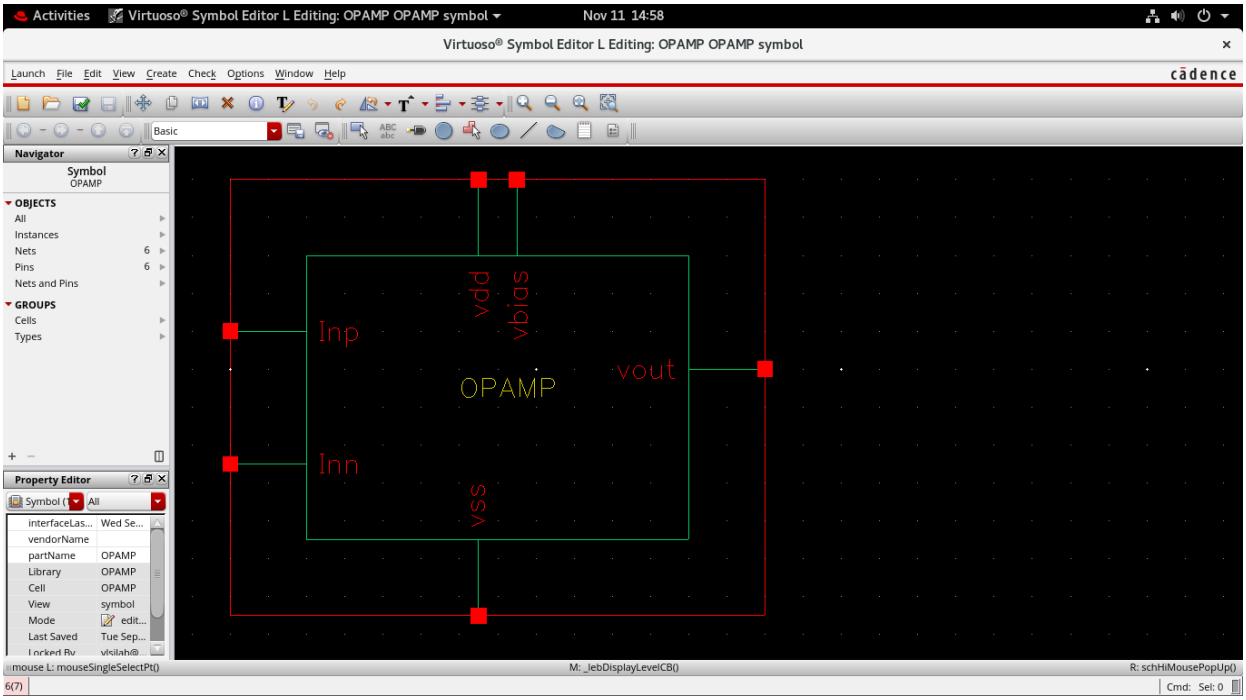


Fig 4.3: Creation of symbol of two stage op-amp using cadence tool

In the above shown diagram is a symbol of the two stage of operational Amplifier using the Cadence Tool of 45nm

1. Symbol Outline: The green rectangle in the center is the symbol boundary representing the opamp. Pins are attached to this boundary and labeled accordingly.

2. Pins: Each red square represents a pin for electrical connections

Inn: Inverting input, Inp: Non-inverting input, out: Output, Vdd: Positive supply, Vss: Negative supply / ground, Vbias: Bias voltage. These pins are standard for a differential opamp with biasing.

3.Test circuit:

The op-amp has two DC voltage sources representing VDD and VSS, and is biased using a current source labeled as I1 with a specified bias current (Ibias). Additionally, an AC voltage source is connected to the non- inverting input to provide a test signal, which is likely used for transient or frequency response analysis. A capacitor is connected to the output to simulate loading or to help analyze the output behavior.

The schematic includes various ground connections for a common reference point. Overall, the testbench is designed to verify the performance characteristics of the opamp, such as gain, frequency response, and stability under specific power and biasing conditions.

4.Test circuit-1:

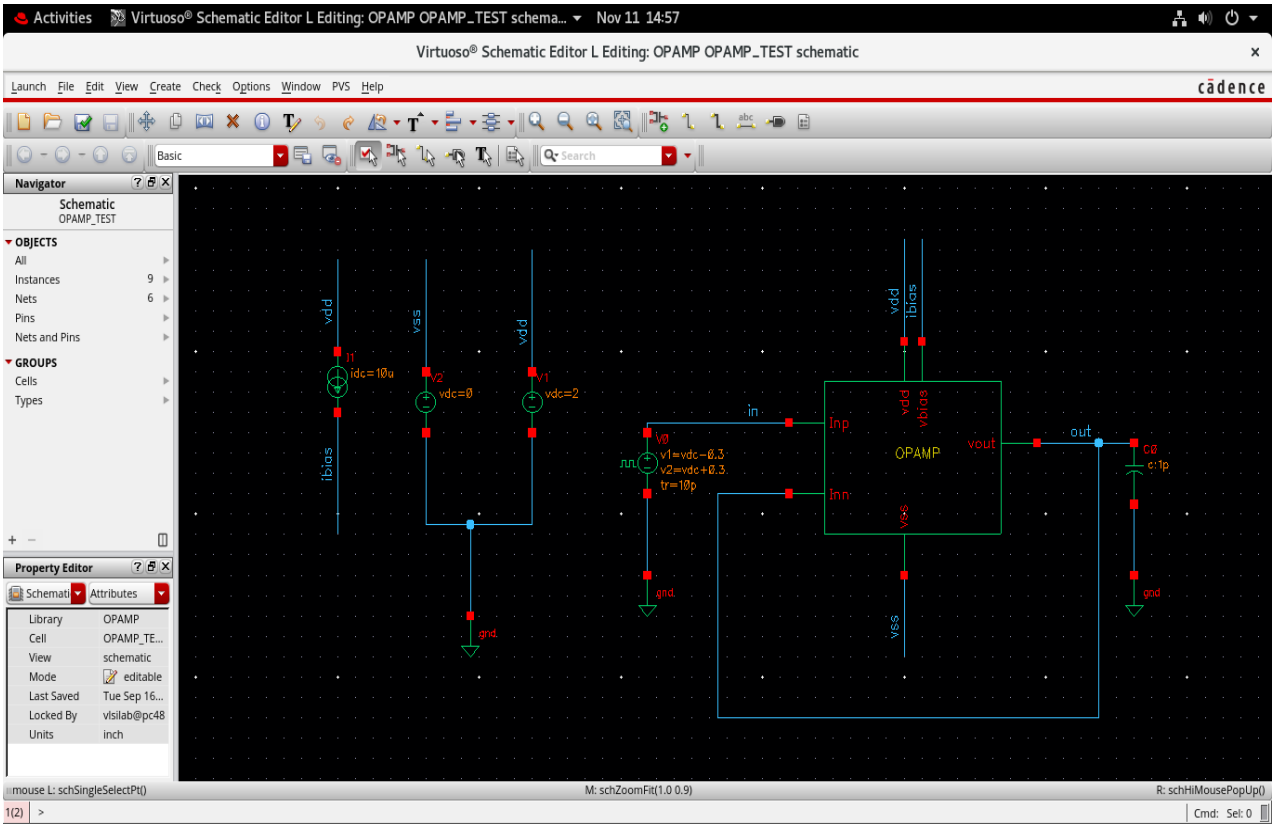


Fig 4.4: Test circuit diagram of the twostage op-amp using Cadence tool.

Transient analysis simulates the circuit's behavior over time when time-varying (dynamic) signals are applied. It helps observe the time-domain response like rise time, fall time, delay, and signal shape. DC (Direct Current) analysis finds the steady-state operating point (bias point) of the circuit—this includes node voltages and currents through elements when no time-varying signals are present.

Transient analysis evaluates how the opamp reacts to input signal changes over time, which is critical for understanding its dynamic performance. DC analysis helps confirm if the opamp is correctly biased and functioning in the intended region

5.Test circuit-2:

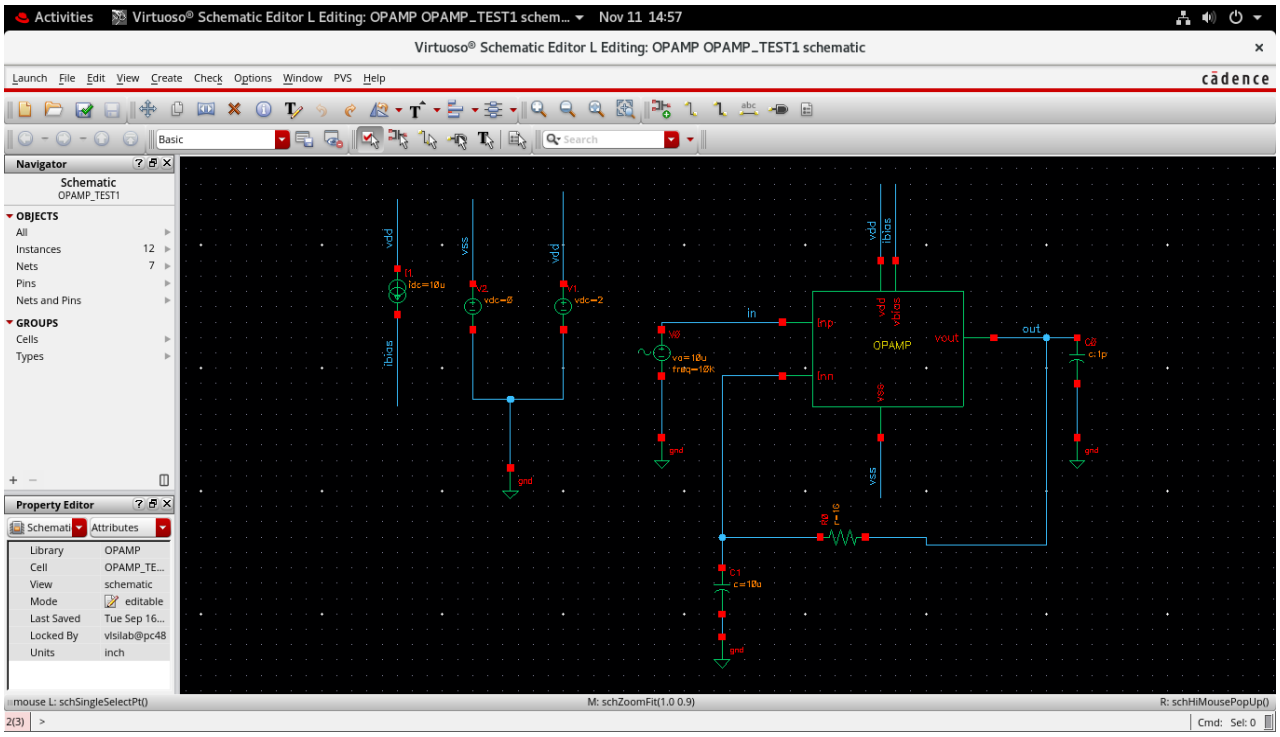


Fig 4.5: Test circuit diagram of the twostage op-amp using Cadence tool.

1. Power Supply Section (VDD and VSS): The schematic uses two independent DC voltage sources to power the operational amplifier. The positive supply (V1) provides +2 V, while the negative supply (V2) provides –2 V. Together, these form a dual ±2 V power rail, which is commonly used in analog circuits to allow the op-amp to process both positive and negative input signals. Both sources are connected directly to the corresponding vdd and vss pins of the OPAMP symbol. Proper dual-supply configuration ensures that the amplifier operates correctly with adequate headroom for linear amplification.

2. Bias Current Source (I1 – 10 µA): A constant current source labeled I1 supplies a 10 µA DC bias current to the OPAMP through the pin marked vbias. Many custom-designed analog circuits, especially differential amplifiers and op-amps, require an external bias current to set the operating point of internal transistors. This bias current determines important parameters such as transconductance, slew rate, and power consumption. By connecting a stable 10 µA current, the designer ensures that the op-amp operates in its intended region.

3. Input Signal Source (AC Source V6): The input signal for testing the OPAMP is generated by the AC source labeled V6. It is configured with a small AC amplitude (vo = 10 μV) and a test frequency of 10 kHz. This source is connected to the non-inverting input (inp) of the OPAMP. The purpose of this signal is to evaluate the amplifier′s small-signal behavior, such as AC gain, frequency response, or transient behavior, depending on the chosen simulation mode. By applying a small sinusoidal signal, the testbench ensures linear operation and accurate measurement of amplifier characteristics

4. OPAMP Symbol Block: At the center of the schematic is the OPAMP symbol, which represents the internal amplifier circuit designed in another cell. It includes input pins (inp and inn), supply pins (vdd and vss), a bias input (vbias), and an output pin (vout). The OPAMP is placed inside a test environment to validate its DC, AC, and transient performance. The connections ensure that the amplifier receives correct biasing, proper power supply, and an input signal to amplify, allowing complete functional verification.

5. Feedback Network : A resistor R0 and capacitor C1 form a frequency-dependent feedback network connected around the OPAMP. R0 is connected from the output node to the inverting input (inn), while C1 connects the same inverting input to ground. Together, they create an integrator or a compensated feedback configuration, depending on the chosen values. This network is essential for stabilizing the OPAMP and controlling its closed-loop gain. The feedback ensures that the amplifier operates in a predictable manner and allows the designer to study stability, bandwidth, and phase margin during simulation.

6. Output Load Capacitor (CL = 1 pF): The output of the OPAMP drives a small load capacitor of 1 pF, which represents the load that the amplifier might experience in real-world applications. This capacitor helps evaluate the OPAMP′s ability to drive capacitive loads without oscillation. It also affects transient response, settling time, and overall stability. Including a load in the testbench is crucial for verifying the practical performance of the amplifier under realistic operating conditions.

7. Ground References: All ground terminals in the schematic are connected to the global ground node.This provides a common reference point for the entire circuit, ensuring correct operation of the DC sources, bias networks, and signal paths. The global ground connection is required for proper simulation convergence and accurate measurement of voltages and currents in the testbench.

3. Layout:

The layout shown in your screenshot represents a complete OPAMP (Operational Amplifier) layout designed using Cadence Virtuoso. The entire circuit is placed inside a yellow PR Boundary, which defines the physical size and area of the layout block. Inside this boundary, different regions correspond to different functional parts of the OPAMP such as the input differential pair, current mirrors, biasing section, output stage, and power distribution network. The layout carefully follows analog design principles such as symmetry, matching, short routing paths, and clean separation of sensitive analog nodes.

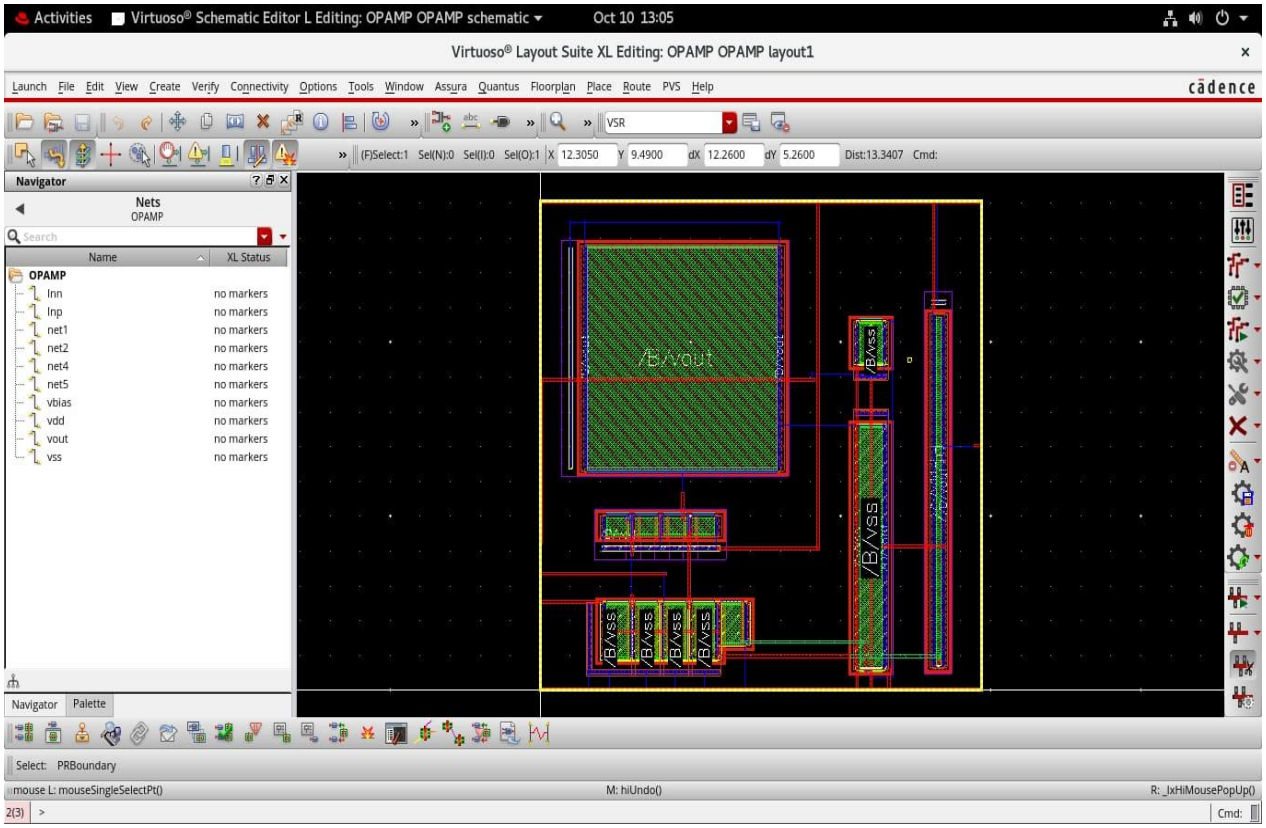


Fig 4.6: Layout diagram of the two stage op-amp using Cadence tool

At the top-left region, the large green-filled block labeled Vout is the Output Stage of the OPAMP. This region consists of large PMOS/NMOS transistors that form the second stage or the output buffer. These devices are sized larger because they need to drive the output node with higher current. The dense metal routing above them ensures low resistance and good performance. This area typically handles the highest current in the OPAMP.

On the right side of the layout, you see long vertical matched structures labeled VBias and VSS. This is the Bias Circuit and Current Mirror Section. It generates the constant bias currents for the differential pair and other internal nodes. The transistors in this section are placed in matched pairs and often use common-centroid or interdigitated patterns to minimize mismatch and ensure stability.

At the bottom-center, there are small horizontal blocks that form the Input Differential Pair. These are the transistors connected to the two input signals (In+ and In−). Their placement is symmetric so that both input paths have identical electrical characteristics. This is extremely important for minimizing offset voltage and improving CMRR. The differential pair sits near the bottom to minimize noise coupling from other sections.

In the bottom-left corner, multiple cells labeled VSS represent the ground/substrate contacts, which help stabilize the substrate and prevent latch-up. These taps ensure a solid connection to ground and reduce noise coupling from neighboring transistors. They also form a continuous grounding network across the layout.

Different metal layers (red, blue, green, etc.) represent routing of signals and power. Lower metal layers are used for local device connections, while higher layers carry global signals such as VDD, VSS, VBias, and Vout. The routing is kept short, clean, and orthogonal to reduce parasitic resistance and capacitance — very important for analog circuits.

1.PR Boundary and Overall Layout Structure: The entire operational amplifier layout is enclosed inside a yellow PR Boundary, which defines the physical size and placement region of the block. This boundary ensures that the OPAMP can be integrated smoothly into a larger chip design while maintaining spacing, routing limits, and guard ring constraints. Inside this boundary, all devices, interconnects, bias networks, and power rails are organized in a structured manner to achieve proper functionality and meet analog design layout guidelines

2.Output Stage Region: In the upper-left portion of the layout, the large green-filled block labeled “Vout” represents the output stage of the OPAMP. This region contains the large transistors used to drive the output node, typically forming either the second stage or the output buffer. These transistors are usually sized larger to provide high gain and sufficient load-driving capability. The metal routing over this block combines multiple parallel fingers to reduce resistance, ensure strong current drive, and maintain matching between PMOS and NMOS output devices.

3. Bias Circuit and Current Mirror Section: On the right side of the layout, vertically arranged blocks represent the bias circuitry and current mirror transistors. This section generates the stable bias currents required for the differential input pair and gain stages. The devices in this area are placed using matched and symmetric layout techniques such as common-centroid and interdigitated patterns. The vertical structure helps reduce gradients and mismatch errors, while the labeled node "VBias" indicates the distribution of bias voltage throughout the OPAMP. Proper routing ensures low-noise and stable biasing for the entire amplifier.

4. Input Differential Pair Section: At the bottom-center of the layout, the small horizontally arranged blocks form the input differential pair. These represent the two input transistors that receive the positive and negative input signals (Inp and Inn). The layout ensures symmetry so that both input devices experience identical parasitic and geometric conditions, which is essential for minimizing input offset voltage and improving the common-mode rejection ratio (CMRR). The routing around this section is carefully balanced to provide equal signal paths and maintain precise matching between the two input branches.

5. Power Rails, Substrate Contacts, and Grounding: In the lower-left region, several cells labeled "VSS" represent substrate contacts and ground connections. These contacts ensure proper biasing of the substrate and prevent latch-up, noise coupling, and unwanted parasitic effects. They form a stable reference ground plane for the OPAMP. Additional connections to VDD and other supply lines are routed in upper metal layers to reduce resistance and improve reliability. The distribution of power rails across the layout ensures uniform supply delivery to all transistors and improves overall performance.

6. Interconnect Routing and Metal Layers: Different metal layers (red, blue, green, etc.) are used to route signals efficiently and avoid parasitic coupling. Metal1 is used mainly for local connections, while upper layers carry important nodes such as Vout, VDD, and VBias. The routing strategy keeps critical analog nodes short and isolated to maintain high gain and low noise. Via stacks are placed carefully to provide reliable vertical connections between layers, and the metal fill patterns maintain uniform density for DRC compliance and to avoid stress-induced mismatch.

sCHAPTER 5:

ADVANTAGES:

1.High Gain: The cascade of two gain stages in a two-stage operational amplifier design provides a much higher overall voltage gain compared to a single-stage amplifier. In this configuration, the first stage amplifies small input signals, and the second stage further boosts the signal amplitude. This multiplication of gains from both stages results in a very high total gain, which is crucial for applications requiring precise amplification of weak analog signals, such as in sensor interfaces or analog computation circuits.

2.Improved Output Swing: The second stage of the amplifier, typically implemented as a common-source stage, plays a key role in achieving a large output voltage swing. This means the output can vary over a wide voltage range without distortion or clipping, allowing the amplifier to effectively drive various loads. The improved output swing makes the circuit suitable for applications that demand a strong and undistorted signal, ensuring better linearity and performance across different operating conditions.

3.Good Common-Mode Rejection Ratio (CMRR): The differential input stage in a two-stage op-amp significantly enhances the Common-Mode Rejection Ratio (CMRR). This feature enables the amplifier to reject unwanted noise or interference that appears simultaneously on both input lines, allowing only the difference between the two signals to be amplified. A high CMRR is vital for analog signal processing applications, such as instrumentation amplifiers, where precision and noise immunity are essential.

4.Better Frequency Compensation Control: In Cadence, frequency compensation—particularly Miller compensation—can be simulated and optimized accurately. This helps control the phase margin of the amplifier and prevents oscillations or instability. Through proper compensation techniques, designers can ensure that the amplifier maintains stable operation across varying frequencies and load conditions, improving both dynamic performance and reliability.

5.Design Flexibility: Cadence provides powerful design flexibility by allowing precise adjustments of transistor dimensions, bias currents, and compensation networks. These parameters can be fine-tuned to achieve the desired balance between power consumption, speed, and gain. This flexibility helps designers optimize performance according to the specific requirements of the application, whether the priority is high speed, low power, or high accuracy.

6.Accurate Simulation and Analysis: Cadence tools such as Spectre and Analog Design Environment (ADE) enable highly accurate simulation and analysis of circuits. Engineers can perform AC, DC, and transient analyses to study the amplifier's behavior under different operating conditions. Additionally, Monte Carlo and corner simulations help evaluate performance variations due to process and temperature changes, while noise and distortion analyses ensure the circuit meets quality and performance specifications before fabrication.

7.Layout and Parasitic Extraction: Using Virtuoso for layout design and Parasitic Extraction (PEX) allows verification of the amplifier's real-world behavior after fabrication. Parasitic resistances and capacitances introduced during the layout process can affect circuit performance, so extracting and simulating these effects ensures accuracy. This step bridges the gap between ideal circuit simulations and actual silicon behavior, confirming that the designed amplifier will perform as intended in practical applications.

8.Better Linearity and Reduced Distortion: A two-stage operational amplifier provides improved linearity and reduced signal distortion compared to single-stage designs. By dividing the total gain across two separate stages, each stage operates within its most linear region, minimizing the chances of signal clipping or harmonic distortion. This ensures that the amplified output closely follows the input signal without unwanted alterations. Such enhanced linearity is especially important in precision applications like instrumentation amplifiers, audio systems, and analog computation circuits, where signal accuracy and fidelity are critical.

CHAPTER 6:

APPLICATIONS:

1. Analog Signal Processing: Operational amplifiers (op-amps) play a key role in analog signal processing, where they are used to amplify weak sensor signals or analog waveforms. These circuits ensure that the small signals from transducers or sensors are strengthened to levels suitable for further processing or measurement. Applications include audio processing, instrumentation, and communication systems, where precise amplification and filtering of analog data are essential.

2. Data Converters: In data converter circuits such as Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs), op-amps are used as buffers or gain stages. They help maintain signal integrity by providing high input impedance and low output impedance, ensuring accurate signal conversion. This makes them essential in digital signal processing systems, where analog signals are interfaced with digital circuits.

3. Control Systems: Op-amps are used as error amplifiers in feedback control systems. They compare a reference input with the actual output and amplify the difference (error signal) to correct the system's performance. For example, in power management and automatic control systems, op-amps help regulate voltage, speed, or temperature by maintaining stable and accurate operation through feedback loops.

4. Active Filters: Active filters use op-amps along with resistors and capacitors to implement low-pass, high-pass, band-pass, and band-stop filtering. These filters allow desired frequency components to pass while blocking unwanted noise or interference. They are widely used in audio systems, communication circuits, and instrumentation to condition and purify signals for further use.

5. Voltage References and Regulators: Op-amps are essential in voltage reference and regulator circuits. They maintain a stable output voltage regardless of variations in input voltage or load conditions. This is particularly important in analog front-end circuits, where precise voltage levels are necessary for proper operation. Op-amps ensure stability and accuracy in linear voltage regulators and reference generators used in power supplies.

6. Audio Amplifiers: In audio systems, op-amps are used in preamplifiers, tone control circuits, and power amplifiers to ensure high-fidelity sound reproduction. They amplify low-level audio signals from microphones or musical instruments with minimal distortion and noise. This application is vital in sound systems, hearing aids, and broadcasting equipment for clear and quality audio output.

7. Medical Electronics: In medical applications, op-amps are used for low-noise amplification of bio-signals such as ECG (Electrocardiogram) and EEG (Electroencephalogram). These biological signals are typically very weak, so op-amps amplify them accurately without introducing noise or distortion. This enables precise monitoring and diagnosis of physiological conditions, making op-amps indispensable in biomedical instrumentation.

8. Instrumentation Amplifiers: Instrumentation amplifiers are precise amplifier circuits built using op-amps. They amplify small differential signals while rejecting common-mode noise or interference. These are widely used in measurement systems, strain gauge sensors, temperature sensors, and biomedical instruments where accuracy and noise immunity are critical. Their high input impedance and excellent gain stability make them ideal for sensor signal conditioning.

9. Oscillators: Op-amps are used to build oscillators that generate continuous waveforms like sine, square, or triangular waves. Circuits such as Wien-bridge and phase-shift oscillators use op-amps to provide the required feedback and gain for sustained oscillations. These are commonly used in signal generators, function generators, and waveform synthesis in electronic testing and communication equipment.

CHAPTER 7:

RESULTS:

Fig 7.1: Transient Analysis waveform

Input Waveform: The input waveform is represented square-wave signal applied to the two-stage operational amplifier during transient analysis in Cadence Virtuoso. This input signal alternates between a high level of approximately 1.2 V and a low level of around 0.8 V, repeating with a steady periodicity. The purpose of applying such a square wave is to test how the op-amp behaves under rapid voltage transitions, allowing the designer to observe large-signal performance parameters such as propagation delay, slew rate, and settling behavior. Because square waves force the op-amp to respond quickly to sudden changes, they serve as an effective stimulus for evaluating the transient response of the entire system.

Output Waveform: The waveform represents the output voltage of the two-stage op-amp when subjected to the square-wave input. The output closely follows the shape and timing of the input signal, indicating that the op-amp is functioning properly and responding to the stimulus as expected. Although the output tracks the input, it shows a slightly slower rising and falling edge, which is characteristic of a two-stage op-amp due to internal compensation and limited drive current. The output voltage swings between approximately 0.8 V and 1.15 V, demonstrating that the design achieves a reasonable output swing for the given biasing conditions.

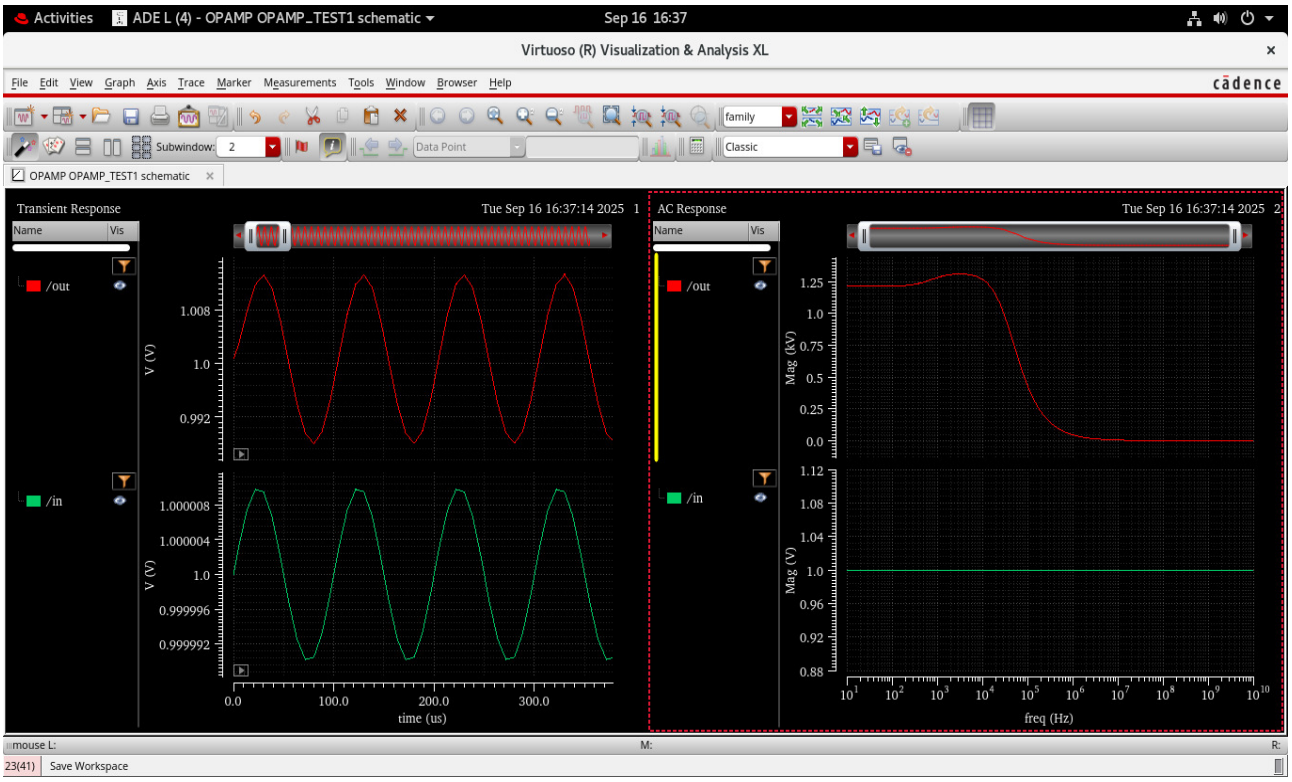


Fig 7.2: Transient and AC Analysis

Transient Response: The transient response displayed on the left side of the diagram shows how the op-amp's input and output signals behave over time when a sinusoidal signal is applied. The green waveform represents the input signal, which is a small-amplitude sine wave centered near 1 V. The red waveform represents the amplified output signal, which maintains the same shape as the input but has a higher amplitude, indicating the gain provided by the two-stage op-amp. The smoothness of the output waveform shows that the amplifier operates in its linear region without distortion, clipping, or slew rate limitations. This plot confirms that the op-amp can correctly amplify AC signals in the time domain while maintaining waveform integrity.

AC Frequency Response: The AC response shown on the right side of the diagram illustrates how the gain of the op-amp changes with frequency, which is essential for evaluating stability and bandwidth. The red curve shows the output magnitude across a wide range of frequencies. At low frequencies, the gain remains high and stable, representing the DC gain of the amplifier. As the frequency increases, the gain starts to roll off, indicating the presence of dominant and non-dominant poles in the amplifier. This roll-off helps identify key performance parameters such as the −3 dB bandwidth and unity-gain bandwidth (UGB). The green curve, representing the input AC amplitude, stays flat, confirming that the input reference

remains unchanged across frequency. This frequency-domain analysis verifies that the amplifier has proper compensation and stable high-frequency behavior.

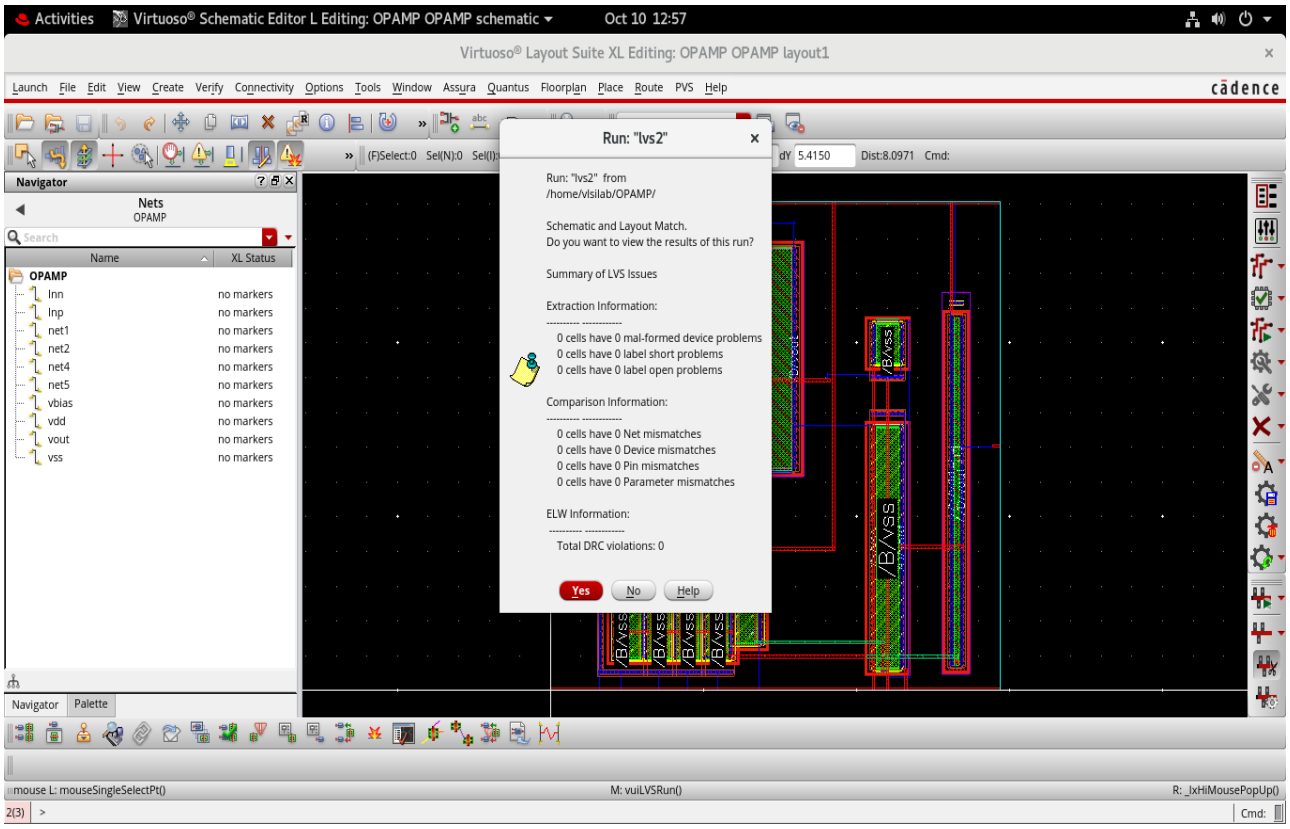


Fig 7.3: DRC and LVS check

1. Introduction to LVS: Layout Versus Schematic (LVS) is an essential verification process in VLSI design that compares the physical layout of a circuit with its original schematic. The main goal of LVS is to ensure that the electrical connectivity and device structures implemented in the layout exactly match the circuit described in the schematic. LVS validates the correctness of the design from a functional and connectivity point of view, ensuring that the layout truly represents the intended electrical behavior.

2. Purpose of Performing LVS: The purpose of LVS is to detect any inconsistencies or mismatches between the schematic and layout, which could otherwise cause the fabricated circuit to fail. LVS checks whether all components used in the schematic, such as transistors, resistors, capacitors, and connections, are properly implemented in the layout. It also verifies that there are no missing or extra devices, no incorrect connections, and no mismatched parameters like transistor width and length. This ensures that the final circuit will behave exactly as simulated.

3.How LVS Works in Cadence Virtuoso: In Cadence Virtuoso, the LVS tool works by first extracting a netlist from the layout using a process called layout extraction. This extracted netlist includes device information, node connections, and parasitic details inferred from the layout geometry. The tool then compares this extracted netlist with the schematic netlist on a device-by-device and net-by-net basis. If any mismatches are found, LVS highlights the errors and reports them for correction.

4. Types of Errors Detected by LVS: LVS can detect various types of mismatches that may occur during layout creation. These include device mismatches, where a transistor or component may be missing or extra; net mismatches, where connections do not match the schematic; pin mismatches, where labels like VDD, VSS, or input/output pins differ; and parameter mismatches, where device sizes such as W/L ratios do not match the schematic. LVS also identifies shorts, where unintended connections are formed, and opens, where expected connections are missing.

1. Introduction to DRC: Design Rule Check (DRC) is a crucial verification process in VLSI layout design that ensures the drawn layout follows all the manufacturing rules defined by the semiconductor foundry. These rules specify the minimum dimensions and spacing required between different layers so that the fabricated chip works reliably. DRC checks the physical correctness of the layout and helps ensure that the circuit will be manufacturable without defects.

2.Purpose of Performing DRC: The main purpose of running DRC is to identify any layout errors that could lead to fabrication issues such as short circuits, opens, or electrical leakage. DRC verifies important parameters like metal width, spacing between conducting layers, via enclosure, and proper overlapping of layers. By catching these errors early, designers can correct the layout before moving toward fabrication, ensuring reliability and yield of the IC.

3. How DRC Works in Cadence Virtuoso: In Cadence Virtuoso, when the DRC tool is executed, it scans the entire layout and compares each shape with a set of predefined geometric and spacing constraints from the technology file. The tool automatically detects violations and highlights them using markers in the layout window. Each marker indicates an exact location where the layout violates the rules. After scanning, the tool generates a summary showing the total number of DRC errors, allowing designers to quickly identify and fix the issues.

CHAPTER 8:

CONCLUSION:

The two-stage operational amplifier was successfully simulated using the Cadence Virtuoso tool at the 45nm CMOS technology node. The design met the targeted performance parameters, including gain, phase margin, and unity gain bandwidth, which are critical for stability and amplification in analog circuits.

Through the use of Cadence's simulation environment, detailed analysis such as DC operating point, AC analysis, transient response carried out. These simulations confirmed the proper biasing of the amplifier stages, good linearity, and robustness against process variations.

The design process highlighted the importance of careful transistor sizing, bias current optimization, and compensation techniques to ensure stability and desired frequency response. The two-stage architecture proved effective in providing high gain and flexibility in compensation design, making it suitable for low-voltage, high- performance analog applications in modern CMOS technologies.

The major goal of this study is to design and optimize the size of a two-stage miller compensated Opamp with nulling resistor in 90nm node technology [3-5]. The main challenge remains in the design and implementation of a two-stage Miller compensated op-amp while taking various parameters into consideration that are constraints which are interdependent upon each other. The gain of the circuit is mostly determined by the width to length ratio, abbreviatedas (W/L). The slew rate and bandwidth depend upon Miller capacitance and output load capacitance abbreviated as CL. To ensure for the stability of the circuits several compensation techniques are implemented. Mille compensation is used to ensure for the stability of the circuits while it compensates for the slew rate of the circuit, it pushes the dominant pole towards the origin and moves the secondary pole away from the origin also termed pole splitting, this allows the circuit to have a greater bandwidth than merely implementing a two stage Opamp. In practice, the choice of the miller capacitor requires some iteration because it effects the bandwidth, slew rate, phase margin and location of poles in the system.

CHAPTER 9:

FUTURE SCOPE:

1. Scaling to Advanced Nodes:

The design principles used in 45 nm can be further optimized for smaller nodes such as 32 nm, 22 nm, and FinFET-based technologies, enabling higher gain, faster operation, and reduced power consumption.

2. Low-Power IoT Applications:

As IoT devices demand ultra-low-power analog blocks, the two-stage op-amp can be enhanced with bias-optimization techniques, dynamic thresholding, and leakage-reduction methods suited for sub-45 nm nodes.

3. High-Speed Mixed-Signal Systems:

The architecture can be adapted for high-speed ADCs, DACs, PLLs, and sensor interfaces where high gain with moderate bandwidth is required. Technology scaling improves the unity-gain frequency and transient response.

4. Improved Stability Techniques:

Future work can explore advanced frequency compensation methods (Miller with nulling resistor, Ahuja compensation, feed-forward compensation) to achieve higher phase margin while maintaining high gain.

5. Integration in System-on-Chip (SoC):

45 nm CMOS allows compact layout, enabling integration of the op-amp with digital signal processors, RF blocks, and analog front ends in SoC designs for communication and biomedical devices.

6. Process Variation and Reliability Optimization:

Future scope includes designing robust layouts with mismatch-aware optimization, Monte-Carlo analysis, and temperature-variation handling to ensure stable performance in deep-submicron technologies.

7. Low-Noise Biomedical Applications:

The op-amp architecture can be refined to reduce flicker noise and offset, making it suitable for implantable/portable biomedical sensing systems that rely on low-voltage analog front ends.

8. Use in Machine-Learning Hardware Accelerators:

With growing interest in analog compute-in-memory systems, the two-stage op-amp can be optimized as a readout amplifier for SRAM/Flash crossbars used in neuromorphic accelerators.

CHAPTER:10

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