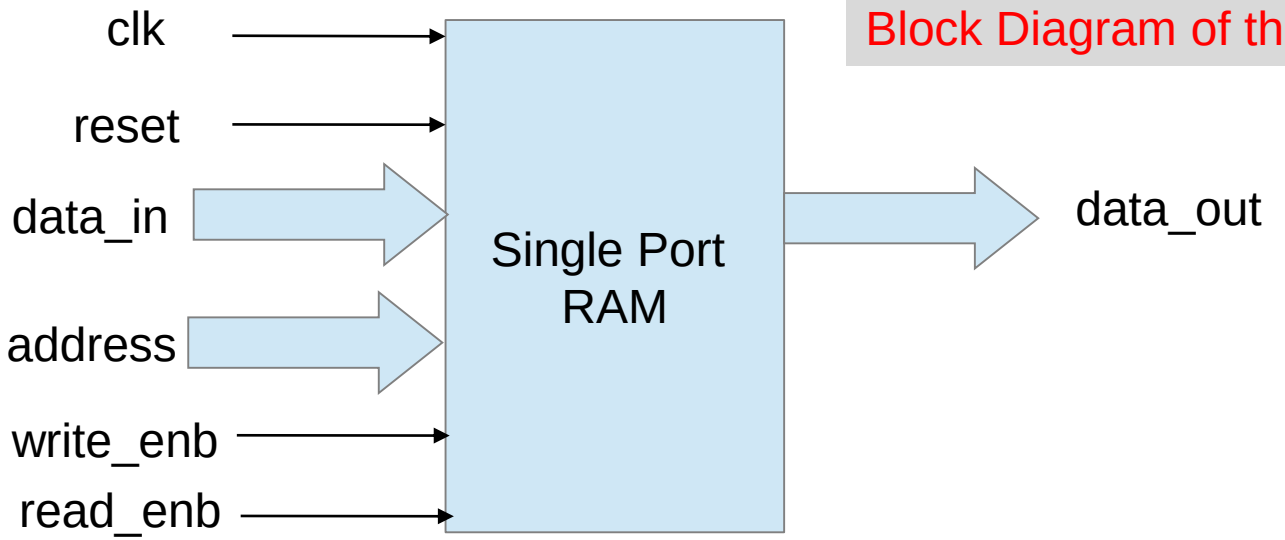
Random Access Memory (RAM) Design Specification Document

1. Design Overview, Functional Description and Block Diagram

- This is a single port RAM
- The operating frequency for the RAM is 50MHz.
- This RAM is 8 bits wide and 32 locations deep.
- When the reset is asserted the RAM is in idle state, i.e., all its inputs will become zero except data input which becomes Z. The data output also becomes Z.
- The RAM supports both read and write operations. If an invalid address is specified for a write operation, the RAM does nothing. However if an invalid address is specified for a read operation the data read from the RAM will be Z..
- It does not support concurrent read and write operations

Block Diagram of the Single Port RAM

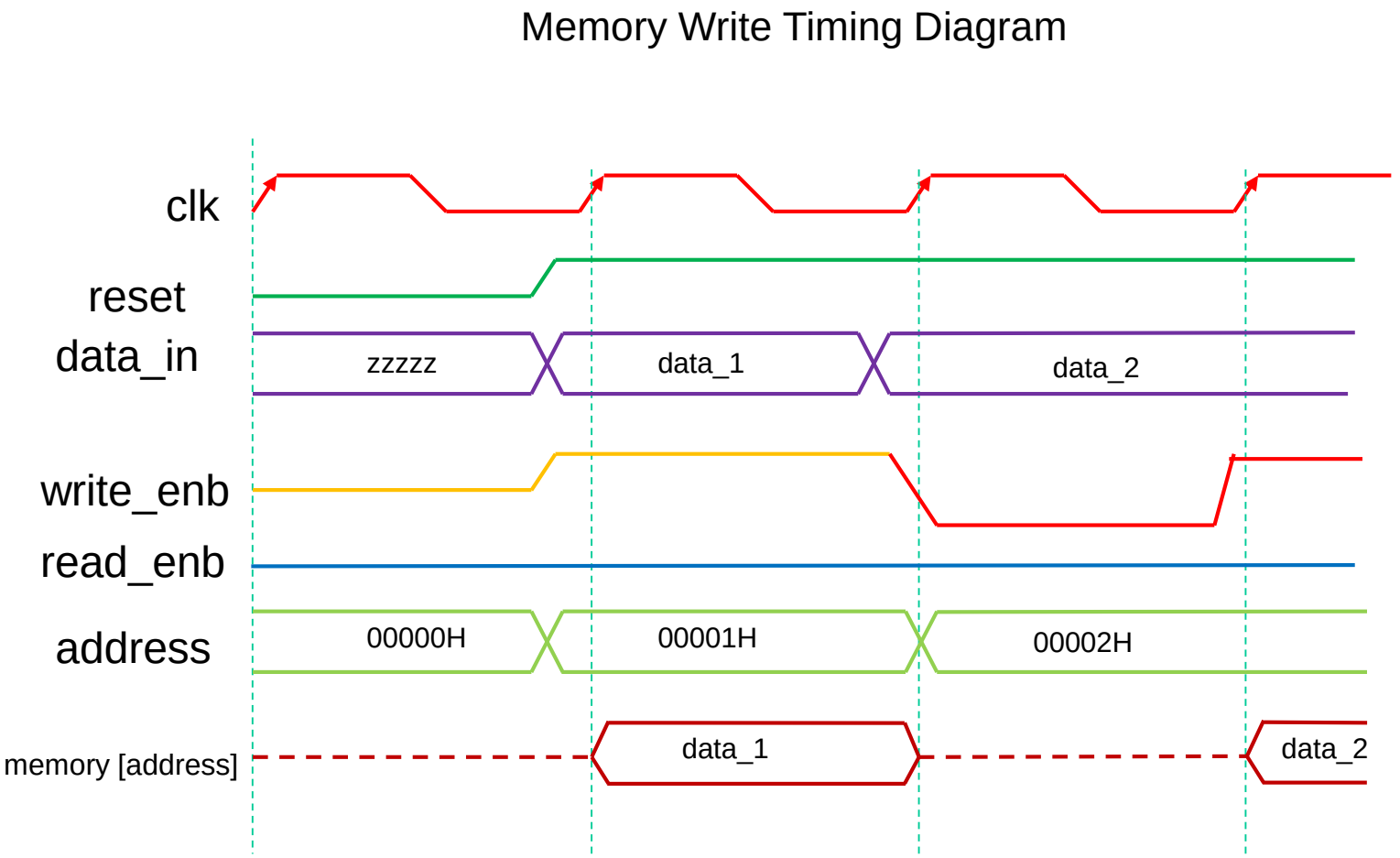


2. Pin Description

Pin-out information of the Single Port RAM:

Pin name	***Direction***	***Width in bits***	***Functionality***
clk	Input	1	Clock signal to the RAM
reset	Input	1	Active low reset signal, to initialize the RAM
write_enb	Input	1	Active high signal to enable write operation
read_enb	Input	1	Active high signal to enable the read operation
data_in	Input	8	Data input to the RAM
address	Input	5	Address to identify the memory location from 0 to 31
data_out	Output	8	Data output from the RAM

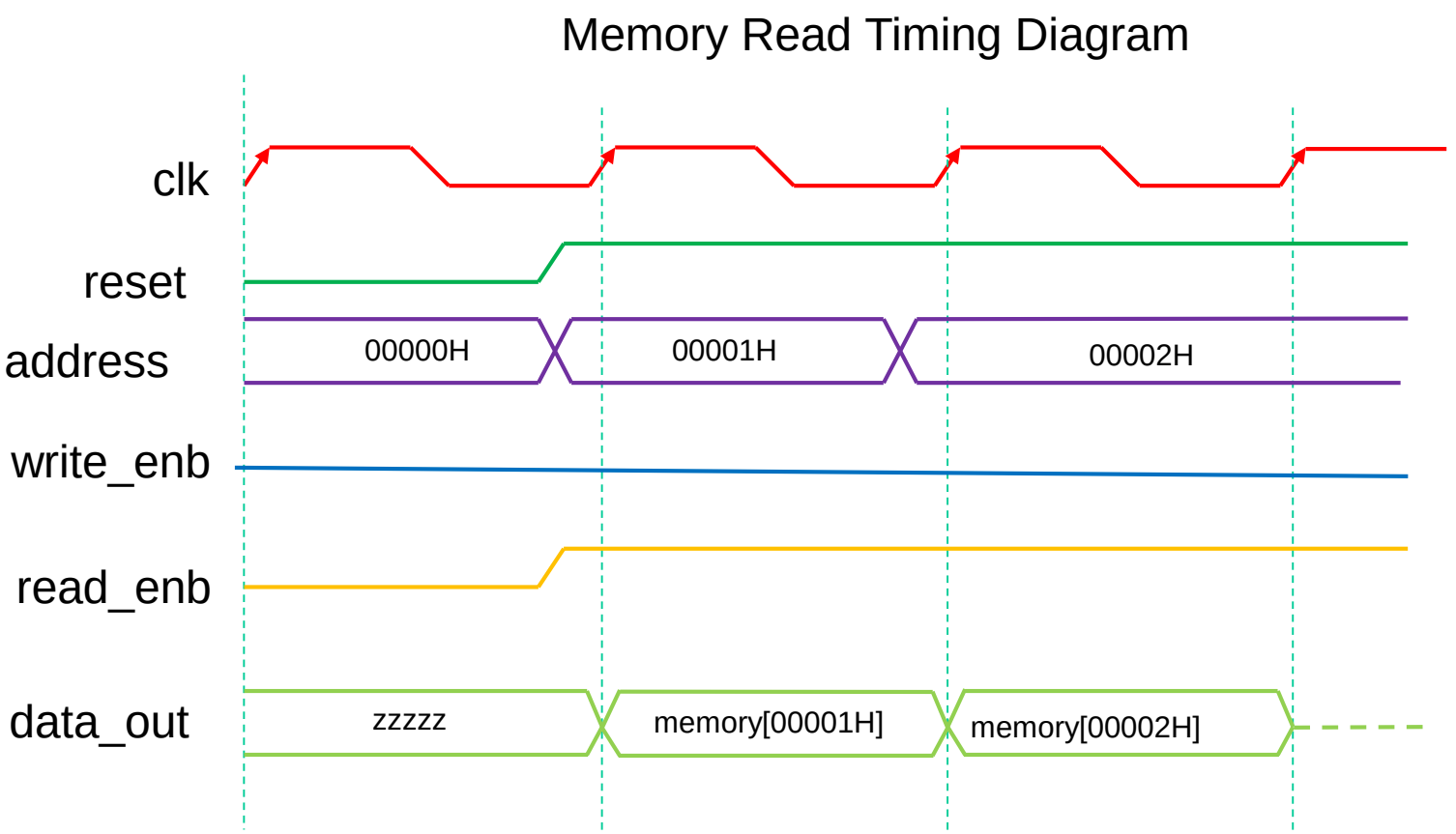
3. Memory Write Operation Description with Timing Diagram



The timing diagram of memory write operation is shown with a positive edge triggered clock ‘clk’ and an active low reset ‘reset’. The following is its description:

1. When reset=‘0’ the input ‘data_in ’ is high impedance and ‘address’ input is zero.
2. When reset=‘1’, ‘write_enb’ =‘1’ and ‘read_enb’=‘0’ then the data_in is written into the corresponding memory address.

4. Memory Read Operation Description with Timing Diagram



The timing diagram of memory read operation is shown with a positive edge triggered clock ‘clk’ and an active low reset ‘reset’. The following is its description:

1. When reset=‘0’ the output ‘data_out’ is high impedance and ‘address’ input is zero.
2. When reset=‘1’, ‘write_enb’ =‘0’ and ‘read_enb’=‘1’ then the data_out is written from the corresponding memory address.