NVRAMcard schematics description

NVRAMcard is based on the SST39SF040 NVRAM chip which is a 512kB non-volatile memory.

The memory is organized in 256 pages of 2 kB. A page is selected by writing a number from 0 to 255 to the parallel register memory 74LS374 by a write cycle (*Device Select synchronous with Φ0) to $C0Nx, where N = Slot# + 8. In this way one of the pages is selected as the 8 outputs of 74LS374 are connected to A12-A19 of NVRAM.

The data bus of the slot is directly linked to the data pins of NVRAM and 74LS374.

The lowest bits of the address bus (A0-A7) are connected directly to NVRAM.

The address bits A8, A9 and A10 are connected to the NVRAM via a multiplexer 74LS257, which upon access of the NVRAM selects inputs “A”, which are linked to A8-A10 of the address bus.

Each selected 2kB page is mapped in the address space $C800-$CFFF and this is selected by *I/O Strobe.

The address bits A8, A9 and A10 are connected to the NVRAM via a multiplexer 74LS257 which is used to zero the bits, in case a $CMxx address is called, where M = Slot#. This is managed by activation of *I/O Select. In that case, the multiplexer selects inputs “B”, which are grounded and effectively A8-A10 are set to 0. At the same time the outputs of 74LS374 are put in high impedance state by grounding its *OE pin and then the 8 pull downs of bits A11-A19 also are set them to 0. Effectively, this selects the lowest 256 bytes of the NVRAM, where the 256-byte firmware is positioned. It is then available at the slot address space $CMxx.

Additional circuitry is added to disable the chip when it is not used. This is necessary as the address space $C800-$CFFF can be used by other hardware and so each such hardware must not keep this space occupied if not in use to avoid conflicts on the address and data buses. Additionally, each program using this address space must turn off the address space, using the circuitry. The circuitry involves a 13-way NAND 74LS133 and a trigger 74LS74, which when on – has the NVRAM enabled and vice versa. The 74LS74 is set to 0 by the *RESET signal and by writing to address $CFFF. It is set to 1 by accessing $C0Nx (usually while selecting a page by writing to it).

When the chip is active, data can be seen in the Slot memory $CMxx and in $C800-$CFFF. When inactive, $C800-$CFFF is off, but the slot memory $CMxx is still active the firmware is always available.

The NVRAM can be written to by activating its *WE pin (synchronous with Φ0) while in the system by writing to the address space *C800-$CFFF following the procedure of the manufacturer. This involved writes to a series of specific addresses prior to writing the actual data.

Finally there are seven 2-way NAND gates and two 2-way NOR gates are used to manage the circuits logic.