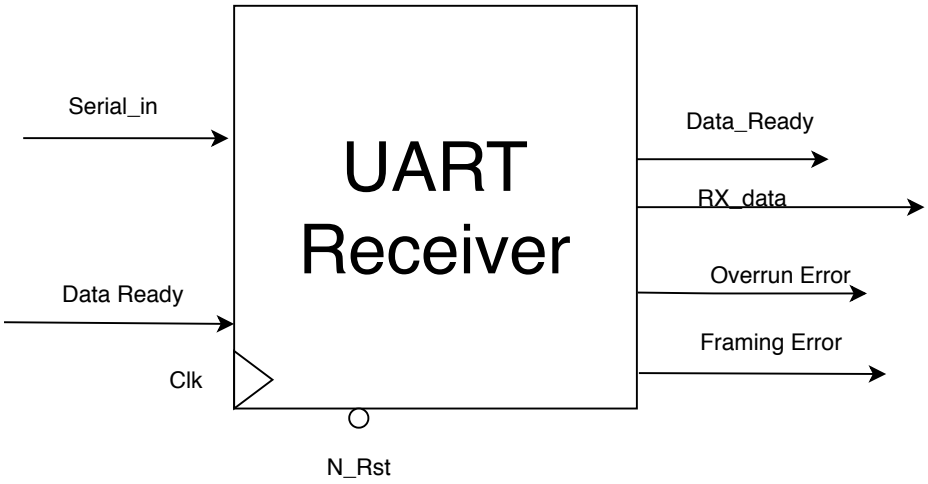
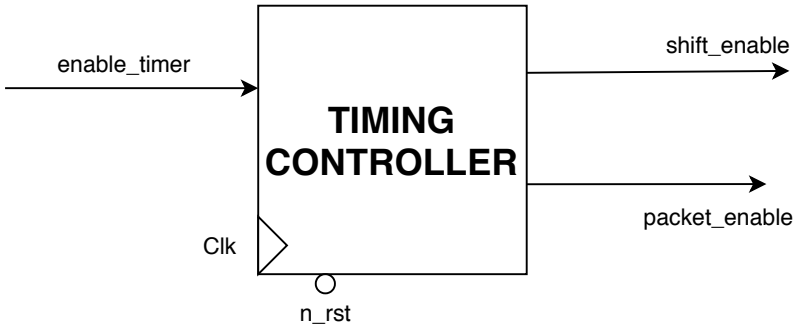
Clk 400 MHz

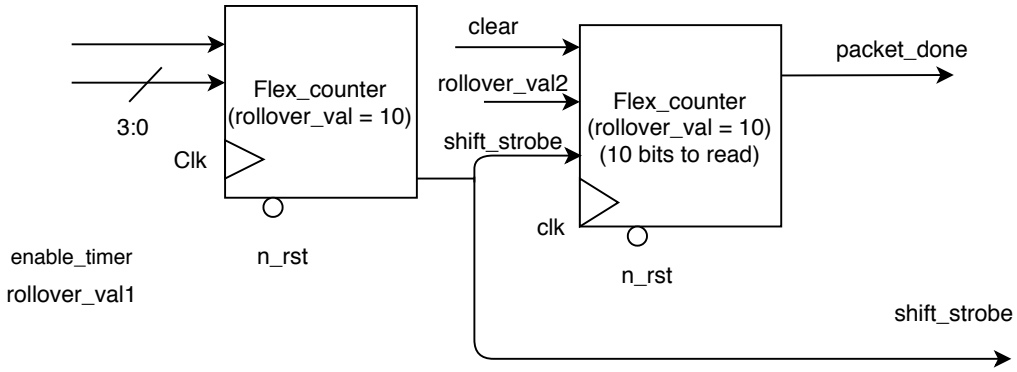
TOP LEVEL DIAGRAM



Top level



Lower Level



next state logic for First flex counter

```
if !enable_timer:
next_count_out = 7
next_shift_strobe = 0

else {
if (count_out == 9)
next_shift_strobe = 1
next_count_out = count_out + 1
else if(count_out == rollover_val1)
next_count_out = 1
next_shift_strobe = 0

else:
next_count_out = count_out1 + 1
next_shift_strobe = 0
}
```

next state logic for Second Flex Counter

```
if clear:
next_count = 0

else if !shift_strobe:
next_count = count

else {
if shift_strobe == 1
next_count = count + 1
else
next_count = count
```

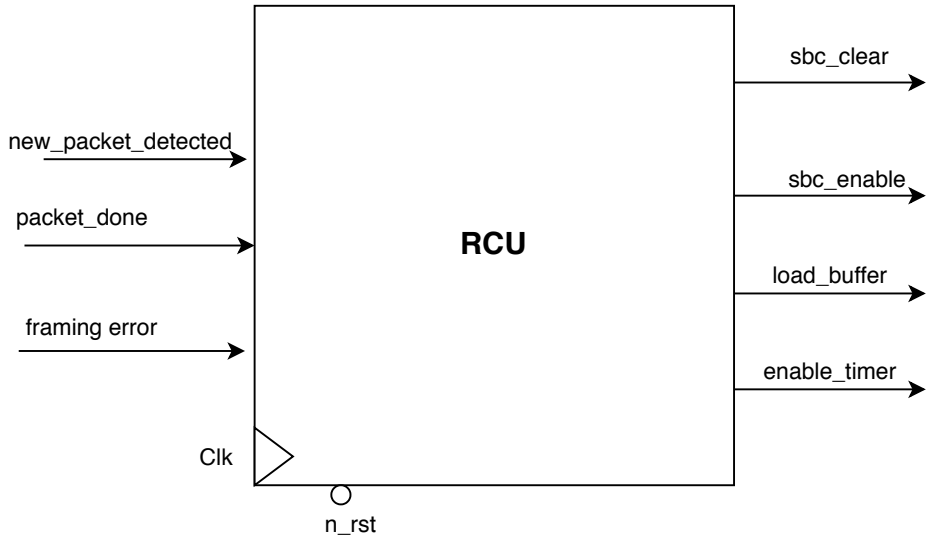
output logic for second Flex Counter

```
if count == 10
packet_done = 1

else
packet_done = 0
```

Receiver Control Unit (RCU)

Top Level Diagram



FSM TRANSITION DIAGRAM - {framing_error, packet_done, new_packet_detected} →

{sbc_clear, sbc_enable, load_buffer,_enable_timer}