Design of Five Stage Ring Oscillator

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***Abstract*— This paper proposes a five-stage ring oscillator for low-power integrated circuits and system applications which will be implemented using 28 nm technology. The circuit design, implementation and analysis will be done using Synopsys Custom Design Platform. The Ring oscillator is designed using the CMOS inverters and a feedback loop to produce oscillations. The circuit design of the ring oscillator uses MOS transistors for the construction of the inverter which is required in each of the five stages. Using the reference circuit waveforms, we can verify the circuit design. This ring oscillator can be used in the design of voltage-controlled oscillation in phase-locked loops.**

***Keywords*— Ring Oscillators, Inverter, CMOS, low power, feedback**

I. Reference Circuit Details

The ring oscillator is a device which has an odd number of inverters, which is used for the positive feedback to produce oscillations. Here we use of odd number of inverters in the oscillator design to produce positive feedback. Here in this circuit, we are going to use CMOS inverters to design the five-stage ring oscillator. The CMOS inverter consists of the complementary MOS transistor with pMOS on the top and nMOS at the bottom. The ring oscillator frequency depends upon the gate delay of the MOSFET, which is the finite time between the change of input and the corresponding change of output. If we add inverters to the existing circuit, the total gate delay increases, thereby decreasing the frequency. The frequency of oscillations of N stage ring oscillator is given by,

$$f = \frac{1}{N * (t_r + t_f)}$$

where t_r is rise in time and t_f is fall time. In this design, we include a enable circuit to control the ring oscillator. When the enable circuit is turned OFF, no oscillations are produced. There will be oscillations if you turn the enable circuit to be ON. For the enable circuit, we have to use a NAND gate as the first stage of the ring oscillator. If one input is always high, then the NAND gate acts as the inverter of the second input. From Fig.1, reference circuit design, we can see the enable circuit which comprises of the pMOS M1, M2 and nMOS M3, M4. The inverter in each stage consists of a pMOS and nMOS. Power supply for the circuit is given through V_{DD} and V_A acts as the enable pin. The output waveform is obtained through V_{OUT} when V_{DD} = 5V and V_A=5V, which represented through Fig.2, Reference Output Waveform. We will implement this five-stage ring oscillator circuit design through 28 nm technology and verify with the sinusoidal waveform obtained as an output.

II. Reference Circuit Design

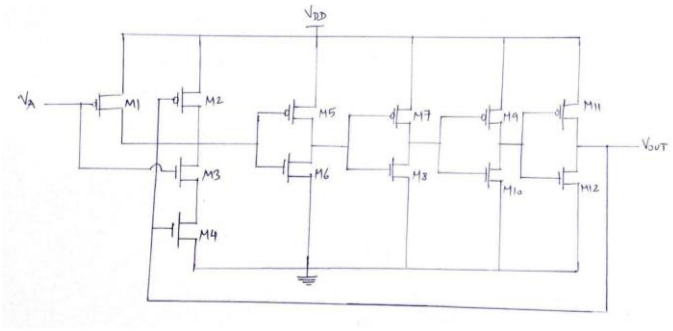

Fig. 1 Design of the reference five-stage ring oscillator circuit

III. Reference Circuit Waveform

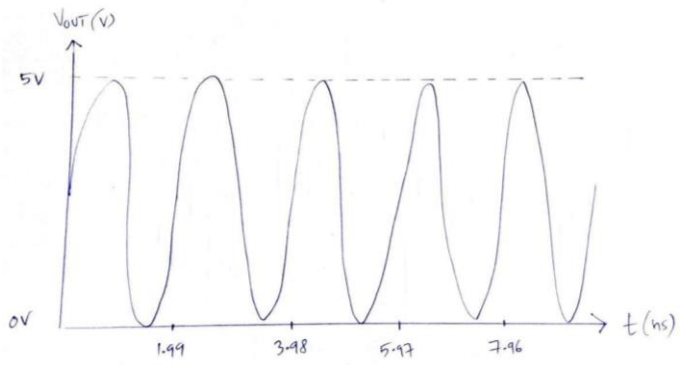

Fig. 2 Reference Output Waveform

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