

AN1200.16 Application Note:

SX1232 LNA and PA Impedance Matching Techniques



1 Table of Contents

1	Table of Contents	2
1	1.1 Index of Figures	2
1	1.2 Index of Tables	2
2	Introduction	3
3	General Impedance Matching Theory	
4	SX1232 Impedance Matching	
4	4.1 LNA Impedance Matching, split path case	3
	4.1.1 Test Setup for sensitivity measurement	
	4.1.2 Measurement of RFI optimum source impedance	
	4.1.3 Measurement of 1dB noise impedance circles	5
	4.1.4 Designing the matching network	
4	4.2 LNA Impedance Matching, combined RFI and RFO ports	
4	4.3 Power Amplifier Impedance Matching RFO port	
	4.3.1 Standard Matching Network, RFO Port	
4	4.4 Power Amplifier Matching, PA_BOOST Port	
4	4.5 Separate RFO and RFI Ports	12
	1 Index of Figures jure 1 RFI Input Match Test Setup	1
	jure 2 LNA Source Impedance Measurement Setup	
	jure 3: Smith Chart Plot of Optimum Noise Match and 1 dB Circle	
	pure 4 Smith Chart showing plot of matching components	
	jure 5 Input matching circuit schematic,	
	jure 6 Input matching with combined RFI and RFO ports	
	jure 7 Power Amplifier Load Impedance Measurement Setup	
	jure 8 PA Load Pull Results	
Figi	jure 9 Three Step Matching	10
	jure 10 PA_BOOST Matching Network	
Fig	jure 11 Combined Network for Separate RFO and RFI Ports	12
	2 Index of Tables	
Tab	ble 1 RFI Optimum and 1dB source impedance values	5
	ble 2 Tabulated Load Pull Results	
Tab	ble 3 RFO Port Performanceble 3 RFO Port Performance	11



2 Introduction

The purpose of this technical note is to assist the engineer in understanding the techniques necessary for proper impedance matching of the LNA and PA ports of the SX1232. Included in this discussion are methods for optimizing receiver sensitivity by providing the optimum impedance transformation from a 50 Ohm source to the SX1232 RFI port. In addition, a similar discussion will describe techniques for providing the optimum load impedance for both the RFO and PA_BOOST ports, which will simultaneously provide maximum power, minimum current, and reduced harmonic content. Minimizing harmonic content by proper matching is important because it will simplify the additional filtering necessary to meet regulatory requirements for harmonic and spurious radiation.

The three ports provided on the SX1232, the RFI, RFO, and PA_BOOST can be used independently by connecting to a T/R switch. Alternatively, the RFI and RFO can be connected together using passive components to provide a transmit/receive port. Configuring these ports will also be discussed.

3 General Impedance Matching Theory

In practice, impedance matching involves designing a circuit which transfers power efficiently from one impedance to another. In most cases, one of the impedances is a known 50 Ohm resistive load while the other can be a combination of a higher or lower resistive component along with a reactive component. Maximum power transfer is achieved when the resistive component of the source is identical to that of the load while the reactance of the load is cancelled by the source. So the problem becomes one of developing a network which simultaneously transforms the source impedance to the load while cancelling out the reactive components. The conventional approach would be to measure the unknown impedance using a vector network analyzer (VNA) or other impedance measuring device. Then using analytic techniques (Smith Chart or computer simulation), develop the network that provides the required matching function. For the case of both LNA and Power Amplifier impedance matching however, simply measuring the device impedance and matching that impedance to the desired 50 Ohm load will not yield the best performance. In order to achieve the optimum source impedance for the LNA and load impedance for the PA, a technique referred to as "load pull" is generally used. This involves using an adjustable tuner which can provide a continuously variable impedance match from a 50 Ohm port to the LNA or PA port allowing independent adjustment of both the resistive and reactive components. The tuner is adjusted while monitoring critical performance parameters (receiver sensitivity, power output, current drain, harmonic content etc) until an optimum level of performance is achieved. Then the impedance of this tuner input is measured and that becomes the optimum LNA source or PA load impedance. A network is then developed that transforms 50 Ohms to this value.

4 SX1232 Impedance Matching

4.1 LNA Impedance Matching, split path case

The following tutorial will illustrate how to measure optimum LNA noise match impedance and how to create a 50 Ohm impedance matching network for the case where the RFI port is connected to a T/R switch or Front End Module. In 4.2, we will discuss the case where the RFI and RFO ports are combined into a single antenna port.

4.1.1 Test Setup for sensitivity measurement

As discussed earlier, the optimum impedance match for the SX1232 RFI port involves the use of an adjustable tuner to vary the source impedance while monitoring performance, in this case receive sensitivity. A simplified block diagram of the test setup is shown in Figure 1. An R/S SMIQ03B signal generator with BERT option is used in this application, but any equivalent generator with bit error rate test capability can be used. An FSK modulated pseudo-random data pattern is used to provide the input test signal for the SX1232. This signal amplitude is varied by the R/S SMIQ03B output level

control. This FSK modulated signal is connected to the SX1232 RFI port through the adjustable tuner. The characteristics of this modulated signal are not important, as long as the SX1232 is properly configured to demodulate it and delivers it with recovered clock back to the R/S SMIQ. The BERT function compares this demodulated data with what was originally sent. This way, bit errors and hence bit error rate (BER) can be measured and observed in real time. By simultaneously reducing the signal level, and adjusting the tuner for minimum BER and further reducing the signal level, an iterative process is used to find the minimum signal level for a given BER (0.1% in this case). The optimum source impedance is achieved when no further improvement by tuning can be measured. When this tuner setting has been reached, the tuner is disconnected from the RFI input and its impedance is measured. It is recommended that this test be performed in a shielded room or to place the SX1232 in a shielded enclosure so that interfering signals will not impact the sensitivity measurement.

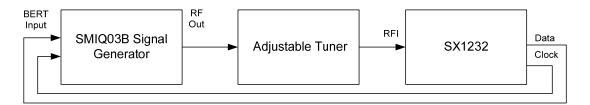


Figure 1 RFI Input Match Test Setup

4.1.2 Measurement of RFI optimum source impedance

Once the tuner has been adjusted for minimum signal level (or best sensitivity) the source impedance driving the RFI port is measured. If an automatic tuner is used, then a measurement setup as shown in Figure 2 can be used. Two identical signal paths are established (same cable length, connectors, etc.) so that this impedance can be easily measured by simply throwing a switch. Thus the tuner impedance presented at the RFI port can also be presented directly to the calibration plane of the VNA for accurate measurement. Or use a manual tuner and RF switch. The tuner can be automated or manual (refer to AN1200.04).

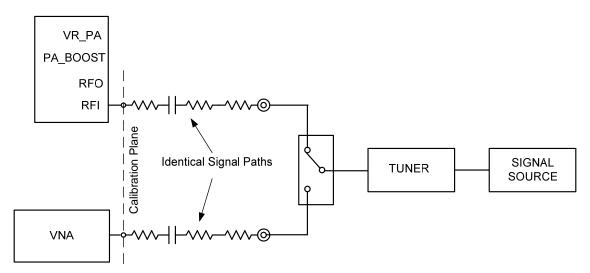


Figure 2 LNA Source Impedance Measurement Setup

4.1.3 Measurement of 1dB noise impedance circles

After the optimum RFI source impedance value is measured, the signal level is increased by 1 dB, and the tuner is again connected to the RFI port. The tuner is re-adjusted to provide a 0.1% BER, and the impedance value at the cable end is again measured by the VNA. There are a number of different tuner settings that will provide this BER value, and when plotted on a Smith Chart they form a circle of impedance values around the optimum match. This plot is referred to as the 1 dB noise circle. Points on this circle represent source impedance values that provide 1 dB degradation in sensitivity from the optimum match. This plot shows how critical the input impedance match is, providing useful information about required component tolerance. The Smith Chart in Figure 3 shows the results of this measurement, and the associated tabulated source impedance values are shown in Table 1 RFI Optimum and 1dB source impedance values.

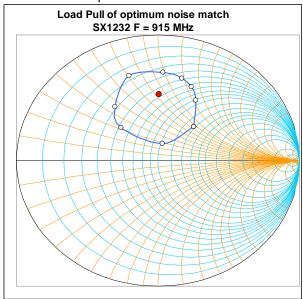


Figure 3: Smith Chart Plot of Optimum Noise Match and 1 dB Circle

Fo 915 MHz	Re	lm
Zs Opt	28.5	+j41.7
Zs Opt -1dB	68.6	+j43.1
	51.3	+j13.9
	26.1	+j15.9
	19.3	+j22.7
	13.2	+j35.5
	17.7	+j49.3
	24.1	+j58.5
	32.2	+j63.4
	45.6	+j62.4
	68.6	+j43.1

Table 1 RFI Optimum and 1dB source impedance values

4.1.4 Designing the matching network

The 50 Ohm source case is reasonably straightforward and can be analyzed using a Smith Chart. The Smith Chart in Figure 4 below shows the matching methodology. Starting at the center representing the 50 Ohm port, adding first a series capacitive reactance specifically –j5.2 Ohms (33 pF), then adding a shunt reactance, specifically –j64 Ohms (2.7pF) then a series reactance, specifically +j69 Ohms (12nH) provides the desired optimum source impedance for the RFI port for 915 MHz. Figure 5 shows the final matching circuit. Combining RFI and RFO ports into a single antenna port case is described in 4.2. Theory and practice don't always align so some manual adjustment of values may be required. Also, the 1 dB circle (in blue) shows that there is some tolerance for component accuracy and variation.

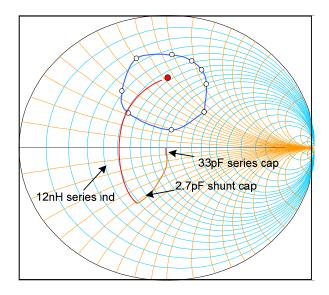


Figure 4 Smith Chart showing plot of matching components

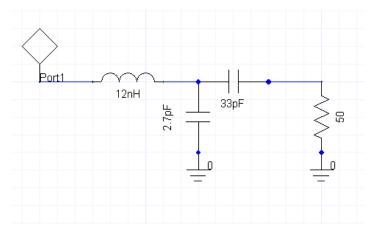


Figure 5 Input matching circuit schematic,

4.2 LNA Impedance Matching, combined RFI and RFO ports

Figure 6, below, shows the topology for matching the LNA when the RFI and RFO ports are combined. Because the source impedance is not 50 Ohms, and there is interaction between this network and the PA match, component selection is not simple but instead involves a rather time consuming iterative process. Because this process is rather involved, Semtech recommends that the following values be used:

$$C = 1.5 pF, L = 5.5 nH$$

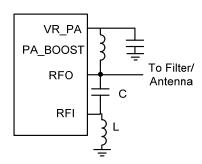


Figure 6 Input matching with combined RFI and RFO ports

4.3 Power Amplifier Impedance Matching RFO port

Figure 7 shows the setup used to determine the optimum load impedance of the PA RFO port for 13 dBm output at 915 MHz. As discussed in 4.2, a 1.5 pF capacitor is needed to join RFI and RFO. This is shown in Figure 7. A 33nH to 100nH choke is connected between VR_PA and RFO for isolation while providing bias to the RFO port. A 47 pF capacitor is used to bypass the VR_PA output. A duplicate network is used at the input port of the VNA in order to assure that the signal paths are identical. A load pull with this network was performed and the results are shown in Figure 8 and Table 2. The optimum load is 28.5 + j 22 Ohms which provides a maximum output power of 13.5 dBm. The range of impedances which provide 13 dBm is also identified on the Smith chart. As before, this provides information about required matching component tolerance in so much as the larger the circle, component selection is less critical and accomplishing first time success is more likely.



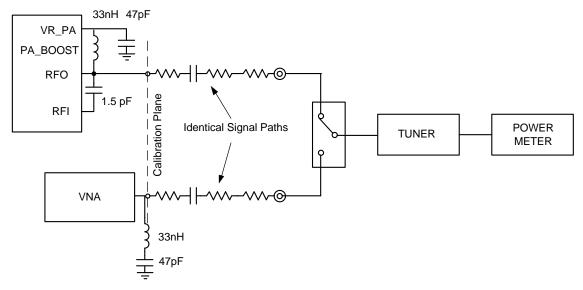


Figure 7 Power Amplifier Load Impedance Measurement Setup

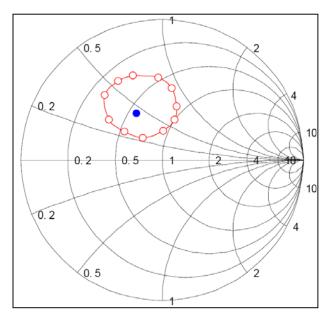


Figure 8 PA Load Pull Results

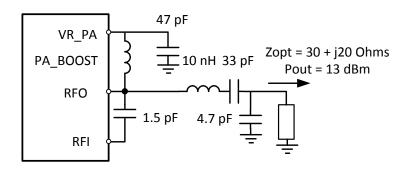


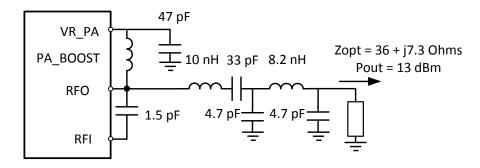
REAL	IMAG	ICONS	POUT	
[Ohms]	[Ohms]	[mA]	[dBm]	
28.5	22	28.9	13.5	C _{RFO RFI} =1.5pF
28.5	22	28.9	13.5	
16.5	33.1	25.4	13	C _{RFO RFI} =1.5pF
23.3	41.9	26.5	13	
32.6	45.1	27.6	13	
44.4	40.4	28.8	13	
49.7	31	29.4	13	
46.7	20.4	29.7	13	
36.2	11.9	29.7	13	
26.9	12.4	30	13	
19.6	14.6	30	13	
14.1	21.1	28.8	13	
14.5	27.5	26.6	13	
16.5	33.1	25.4	13	

Table 2 Tabulated Load Pull Results

4.3.1 Standard Matching Network, RFO Port

The matching of the RFO is done in three steps as shown in Figure 9. In each step an LC section is added and the optimum load impedance is measured with the tuner. After the PA is matched, the 5.6nH inductor is used to tune the RFI port and achieve the best sensitivity. It should be noted that while in transmit mode, the RFI port is internally shorted to ground. The performance is shown in Table 3.





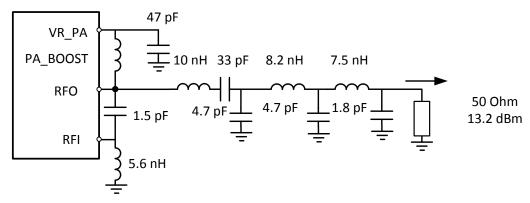


Figure 9 Three Step Matching



	13 dBm Power
Parameter	Setting
H1	13.14 dBm
H2	-52 dBm
H3	-75 dBm
H4	-62 dBm
H5	-51 dBm
H6	-53 dBm
H7	-64 dBm
Idd PA	27 mA

Table 3 RFO Port Performance

4.4 Power Amplifier Matching, PA_BOOST Port

Using a similar approach, the following network was developed for the PA_BOOST port.

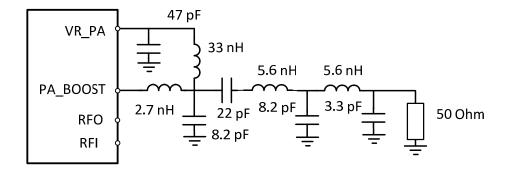


Figure 10 PA_BOOST Matching Network

4.5 Separate RFO and RFI Ports

In cases where a T/R switch or a Front End Module (FEM) with separate TX in and RX out ports are used, the circuit below is recommended.

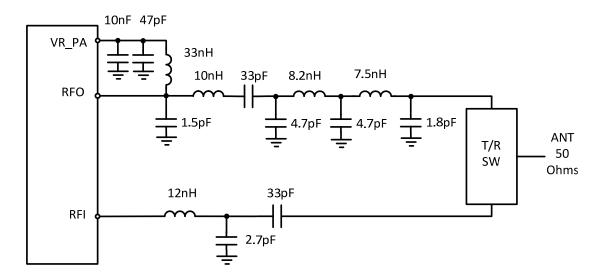


Figure 11 Combined Network for Separate RFO and RFI Ports



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