**Hexagon Application Kit**

For XMC4000 Family

**CPU_45B-V1**

CPU Board XMC4500 SDRAM

**Board User's Manual**

Revision 1.0, 2013-02-20

**Microcontroller**

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**Revision History**

| Page or Item | Subjects (major changes since previous revision) |
|---|---|
| **Revision 1.0**<br>**2013-02-20** | |
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Last Trademarks Update 2011-02-24

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## Introduction

This document describes the features and hardware details of the CPU board "CPU Board XMC4500 SDRAM" (CPU_45B-V1) designed to work with Infineon's XMC4500 Microcontroller. This board is part of Infineon's Hexagon Application Kits. Please visit www.infineon.com/xmc-dev for more information about the Hexagon Application Kit family.

# 1        Overview

The CPU board CPU_45B-V1 houses the XMC4500 Microcontroller and three satellite connectors (HMI, COM, ACT) for application expansion. The board along with satellite cards (e.g. HMI_OLED-V1, COM_ETH-V1, AUT_ISO-V1 boards) demonstrates the capabilities of XMC4500.

The main use case of this board is to demonstrate the external bus unit (EBU) of the XMC4500 device including the tool chain. For this purpose a 64 Mbit SDRAM is connected to the XMC4500 and for external bus extension an asynchronous 16-bit wide bus interface is available at the COM satellite connector.

***Attention: This board (CPU_45B) has not been designed to work with the "General Purpose Motor Drive Card" (MOT_GPDLV). For this purpose please use the CPU boards CPU_45A, CPU_44A or CPU_42A.***

The focus is safe operation under evaluation conditions. The board is neither cost nor size optimized and does not serve as a reference design.

## 1.1        Key Features

The CPU_45B-V1 board is equipped with the following features

- XMC4500 (ARM$^®$ Cortex™-M4-based) Microcontroller, 1 MByte Flash, 160 kByte SRAM, LFBGA-144
- 8 MByte On-board SDRAM, 1 Mbit x 16 bits x 4 banks
- Connection to satellite cards via satellite connectors COM, HMI  and ACT
- USB OTG Host/Device support via micro USB connector
- Debug options
    - On-board Debugger via the Debug USB connector
    - Cortex Debug connector 10-pin (0.05")
    - Cortex Debug+ETM connector 20-pin (0.05")
- Reset push button
- 32 MBit quad SPI flash memory
- Boot option switch
- PowerScale Connector: Ready for power consumption analysis
- Two User Buttons connected to P5.10 and P0.10
- 7 LED's
        3 Power indicating LED's
        2 User LEDs (P5.2 and P1.1)
        1 RESET LED
        1 Debug LED
- Potentiometer, connected to analog input P14.1
- Power supply
    - Via Debug USB connector
    - Via Micro-USB connector in USB device mode
    - Via satellite connector pins (COM/ACT satellites cards can supply power to CPU board)
    - RTC backup battery

## 1.2 Block Diagram

Figure 1 shows the functional block diagram of the CPU_45B-V1 board. For more information about the power supply please refer to chapter 2.1.

The CPU board has got the following building blocks:

- 3 Satellite Connectors (COM, HMI ACT)
- 2 User LEDs connected to GPIOs P5.2 and P1.1
- 2 User Buttons connected to GPIOs P5.10 and P0.10.
- Quad SPI flash memory (32 Mbit)
- Synchronous Dynamic RAM (SDRAM, 64Mbit)
- 2 Cortex Debug Connectors
- Variable resistor (POTI) connected to GPIO P14.1
- USB On-The-Go Connector (Micro-USB)
- On-board Debugger via USB connector (Micro-USB)
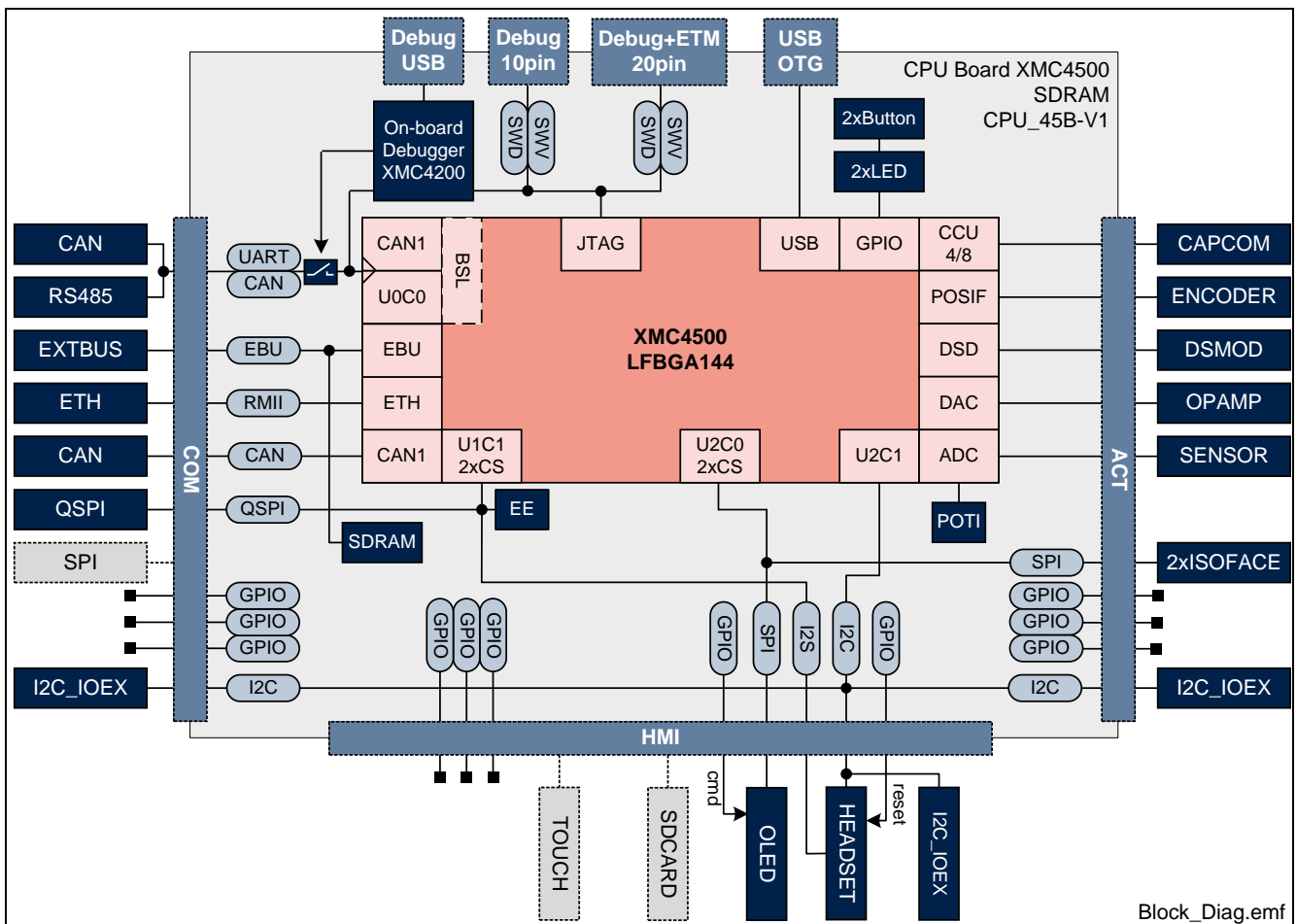


**Figure 1    CPU_45B-V1 Board Block Diagram**

# 2 Hardware Description

The following sections give a detailed description of the hardware and how it can be used.
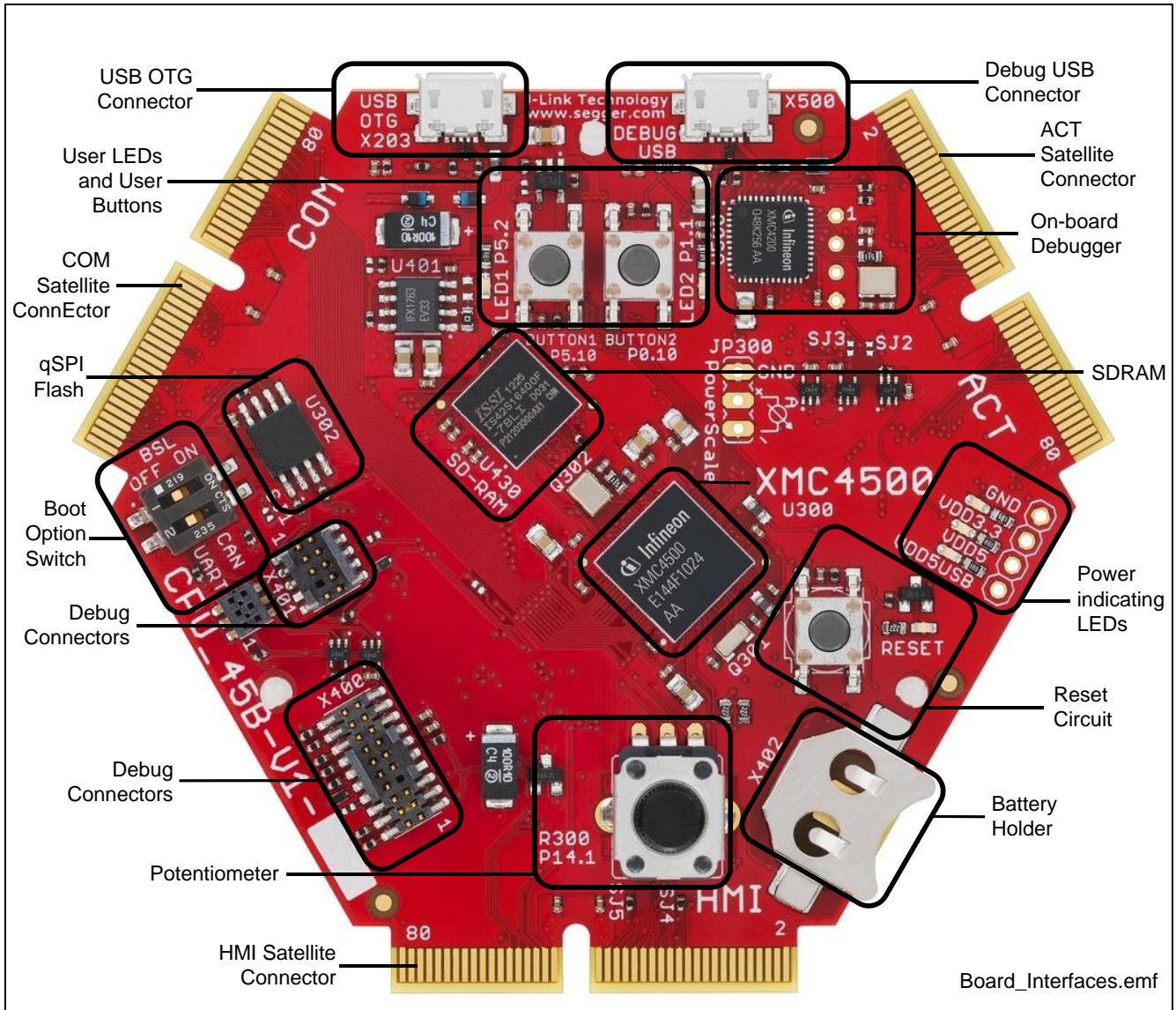


**Figure 2    CPU Board XMC4500 SDRAM (CPU_45B-V1)**

## 2.1 Power Supply

The CPU_45B-V1 board can be powered via either of the USB plugs (5 V); however, there is a current limit that can be drawn from the host PC through USB. If the CPU_45B-V1 board is used to drive other satellite cards (e.g. AUT_ISO-V1 or MOT_GPDLV-V2) and the total current required exceeds 500 mA, then the board needs to be powered by a satellite card, which supports external power supply like e.g. AUT_ISO-V1, MOT_GPDLV-V2, COM_ETH-V1.

The typical current drawn by the CPU board without any satellite cards connected is about 220 mA (@5V).

For powering the board through an USB interface, connect the USB cable provided with the kit to either of the Micro-USB connector on board as shown in Figure 3.
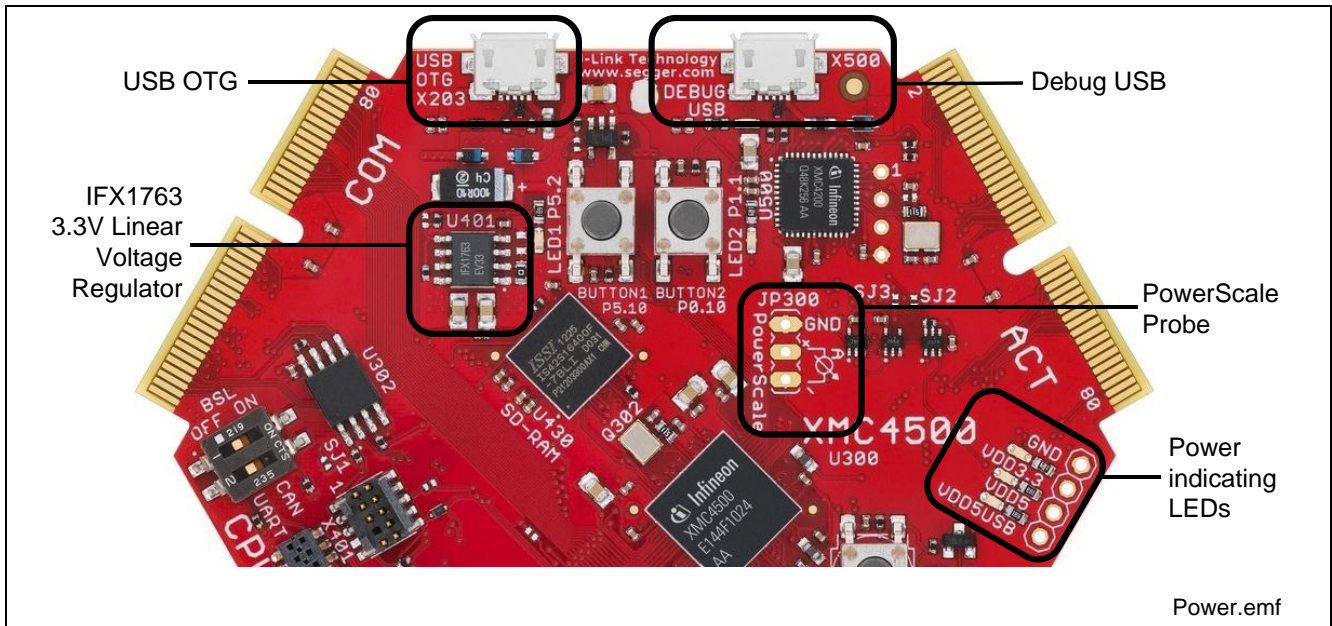
**Figure 3      Powering option**

To indicate the power status of CPU_45B-V1 board three power indicating LED's are provided on board (see Figure 3). The LED will be "ON" when the corresponding power rail is powered.

**Table 1      Power status LEDs**

| LED Reference | Power Rail | Voltage | Note |
|---|---|---|---|
| V401 | VDD5 | 5 V | Must always be "ON" |
| V402 | VDD5USB | 5 V | "ON" if powered by USB OTG connector X203 "OFF" in all other supply cases |
| V403 | VDD3.3 | 3.3 V | Must always be "ON" |
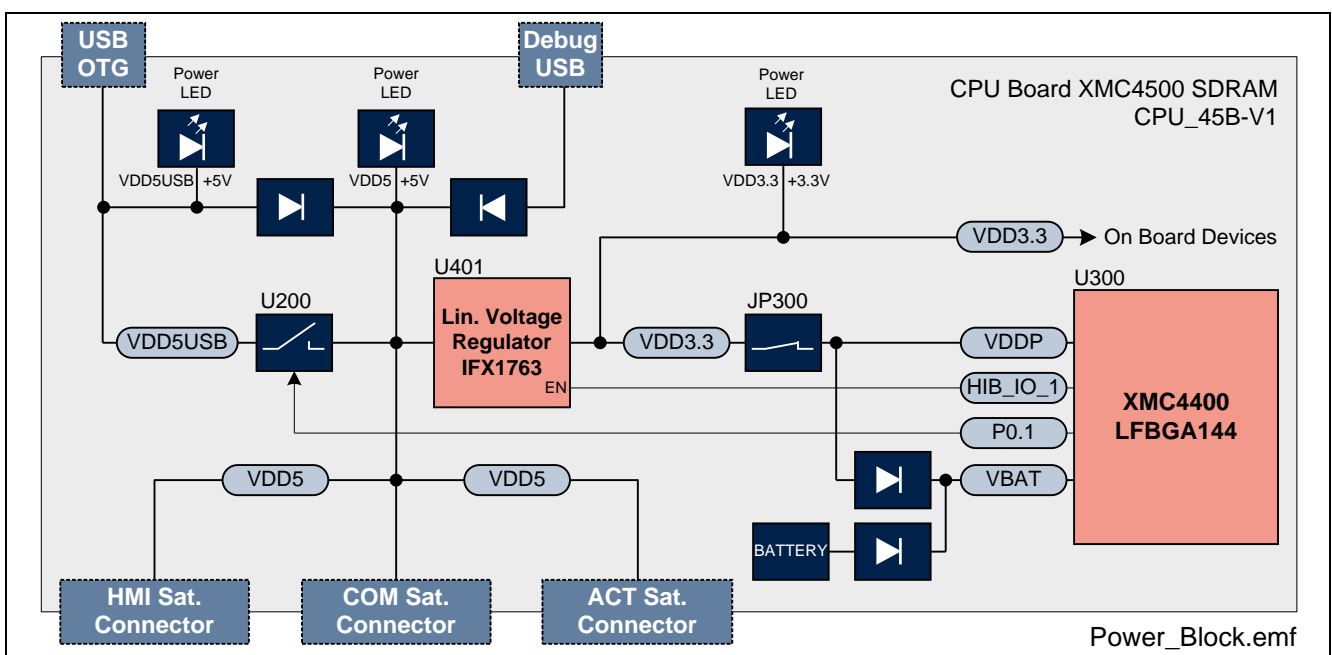


**Figure 4      Block Diagram Of Power Supply**

Hitex PowerScale probe is provided on the CPU_45B-V1 board to measure the power consumption of the XMC4500 device.

**Table 2    Power Measurement**

| Jumper | Function | Description |
|--------|----------|-------------|
| JP300 | PowerScale | A Hitex PowerScale probe can be connected for current sensing the VDD3.3 (CPU power source). Default: pos. 1-2 (closed) |
| | | *Note: On the PCB there is a shorting trace between pin 1-2. This trace has to be cut first, before using PowerScale. Pin 3 is GND.* |

## 2.2 Reset

A reset signal connected to the low-active PORST# pin of the target CPU (U300) can be issued by

- an on-board Reset Button (SW400, RESET)
- an on-board debug device (U500)
- an external debugger connected to either Cortex Debug connector X400 or X401

The RESET signal is routed to all satellite connectors. The reset circuit includes a red LED (V407) to indicate the reset status: The Reset LED (V407) will be "ON" during active reset state and will be "OFF" if reset is not active.

Be aware that PORST# is a bidirectional reset pin of the XMC4000 family which can also be pulled low by the XMC4000 device itself.
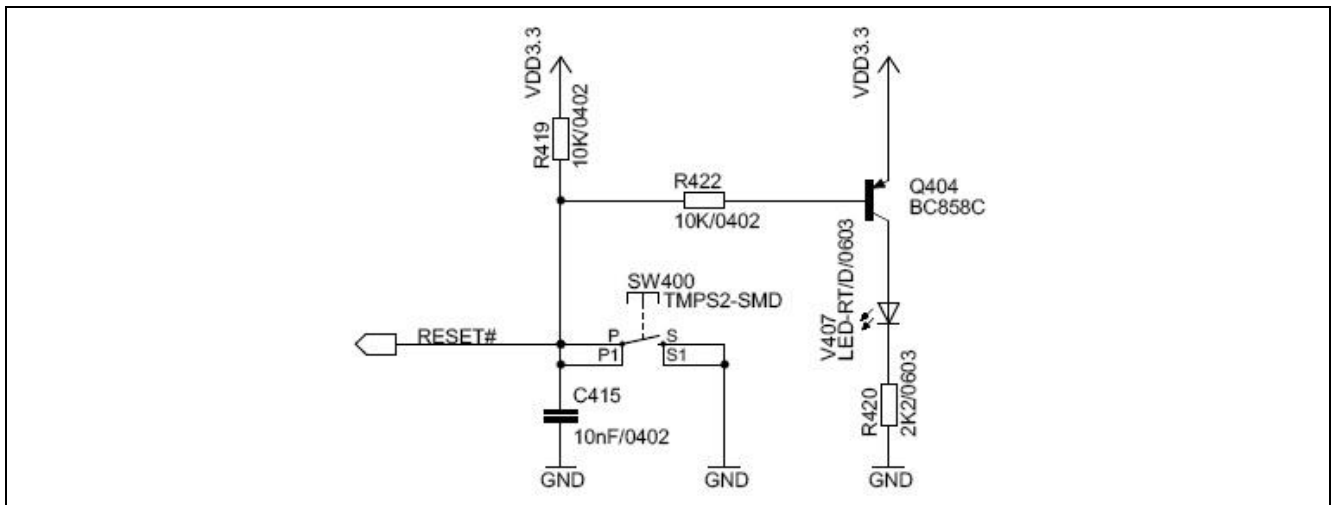


**Figure 5    Reset Circuit**



**Figure 6    Reset LED and Reset Button**

## 2.3 Clock Generation

An external 12 MHz crystal provides the clock signal to the XMC4500 microcontroller. The drive strength of the oscillator is set to maximum by software, in order to ensure a safe start-up of the oscillator even under worst case conditions. A serial 510 Ohm resistor will attenuate the oscillations during operations.

For the RTC clock a separate external 32.768 kHz crystal is used on board.
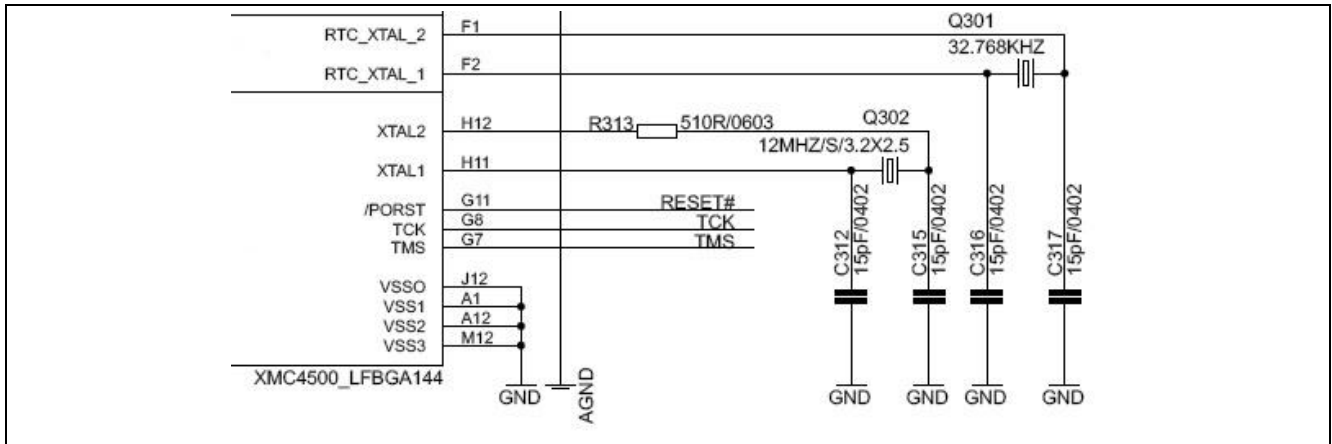


**Figure 7      Clock Generation Circuit**

## 2.4 Boot Option

During power-on-reset the XMC4500 latches the dip switch SW300 settings via the TCK and the TMS pin. Based on the values latched different boot options are possible.

**Table 3      Boot Options Settings**

| BSL (TMS) | CAN/UART (TCK) | Boot Option |
|-----------|----------------|-------------|
| OFF (1) | UART (0) | Normal Mode (Boot from flash) |
| ON (0) | UART (0) | ASC BSL Enabled (Boot from UART) |
| OFF (1) | CAN (1) | BMI Customized Boot Enabled |
| ON (0) | CAN (1) | CAN BSL Enabled (Boot from CAN) |



Boot
Option
Switch

Boot_Switch.emf
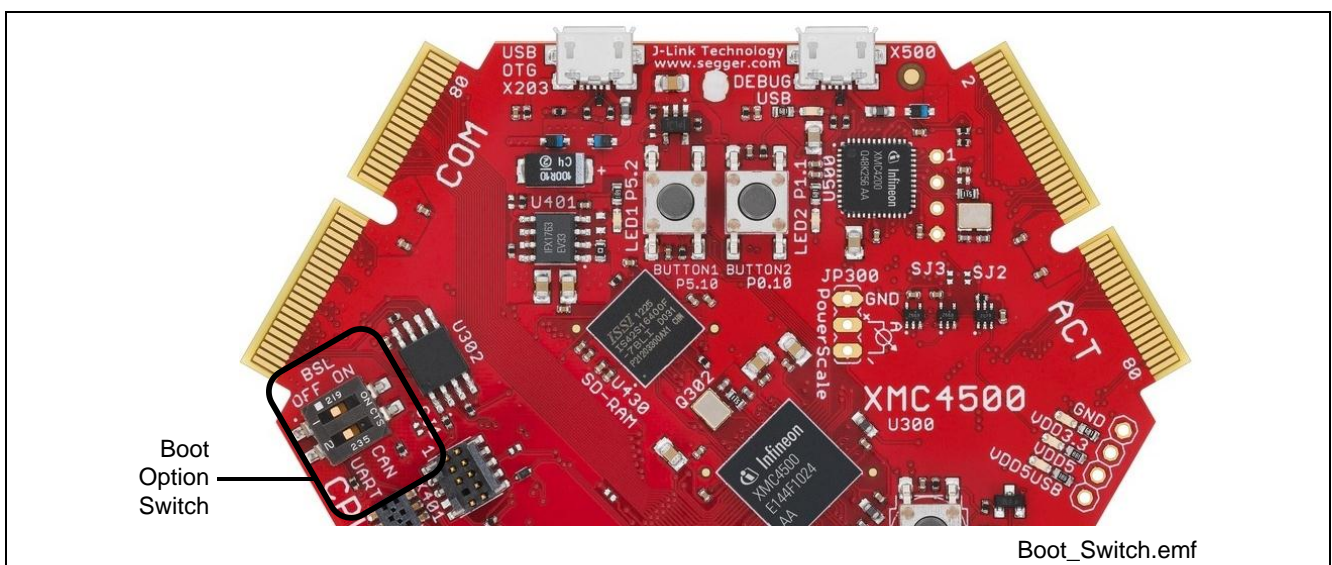
**Figure 8      Boot Options Switch**

## 2.5     Debug Interface

The CPU_45B-V1 board supports debugging via 3 different channels:

- On-board Debugger
- Cortex Debug Connector (10-pin)
- Cortex Debug+ETM Connector (20-pin)

The Hexagon Application Boards are designed to use "Serial Wire Debug" as debug interface. JTAG debug is not supported by default because the GPIO P0.7, where the required TDI function is mapped to also, is used by the on-board SDRAM device and various Actuator boards connected to the ACT satellite connector.

***Attention:*** *It is strongly recommended not to use JTAG debug mode, especially if satellites boards are connected, which uses the GPIO 0.7. For the same reason also do not use the on-board debugger in JTAG mode.*

If you want to use the JTAG debug mode through the cortex debug connectors (X400, X401) anyway, enable the JTAG interface of the XMC device by assembling the pull-up resistor R427 (4k7 Ohm) and the resistor R410 (0 - 33 Ohm).

## 2.5.1    On-board USB Debugger

The on-board debugger [1] supports

* Serial Wire Debug

* Serial Wire Viewer [2]

* Full Duplex UART communication via a USB Virtual COM

[1]    Newer firmware versions of the on-board debugger require the latest J-Link driver (V4.62 or higher) and a Serial Port Driver (CDC driver) installed on your computer. Please check "Install J-Link Serial Port Driver" when installing the latest J-Link driver (see Figure 9)

[2]    Serial Wire Viewer operation does not work during use of the on-board SDRAM.
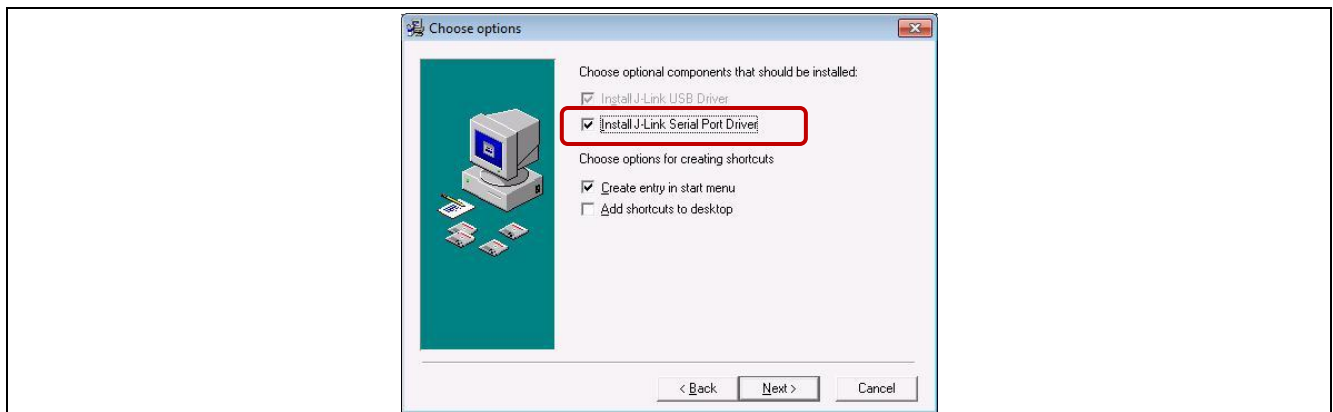


**Figure 9    Installation of Serial Port Driver**

The on-board debugger can be accessed through the Debug USB connector shown in Figure 10. The Debug LED V502 shows the status during debugging.
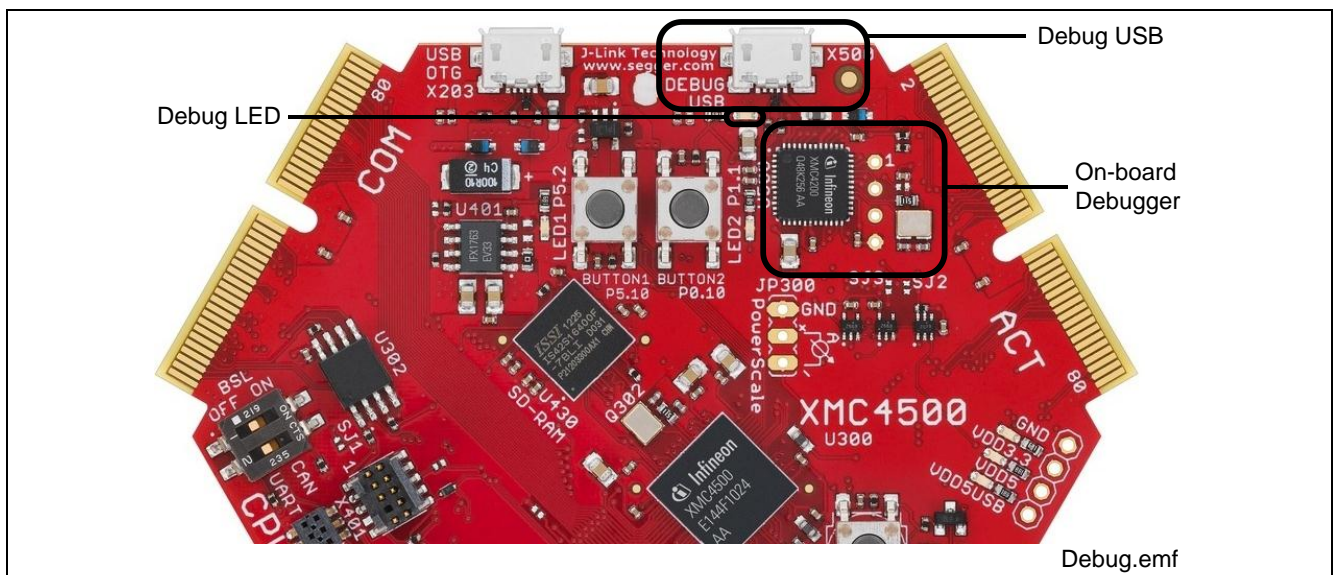


**Figure 10    On-Board USB Debugger**

When using an external debugger connected to the 10pin/20pin Cortex Debug Connector, the on-board debugger is switched off.

When using the USB virtual COM port function of the on-board debugger (connected to P1.4 and P1.5 of the XMC4500) the UART interface to the COM satellite is disabled through the switches U301 and U306.

## 2.5.2 Cortex Debug Connector (10-pin)

The CPU_45B-V1 board supports Serial Wire Debug operation through the 10-pin Cortex Debug Connector.

By default the board does not support Serial Wire Viewer operation through the 10-pin Cortex Debug Connector, because the required SWO pin mapped to P2.1 is used for the connection to the on-board SDRAM. If Serial Wire Viewer operation is required anyway the resistor R404 needs to be assembled.

JTAG operation additionally would require the TDI (P0.7) signal. By default the TDI signal is disconnected from the Cortex Debug Connectors by a not assembled resistor R410, because the pin P0.7 can be used by the on-board SDRAM, by Actuator boards connected to the ACT satellite connector and by boards connected to the COM satellite connector.
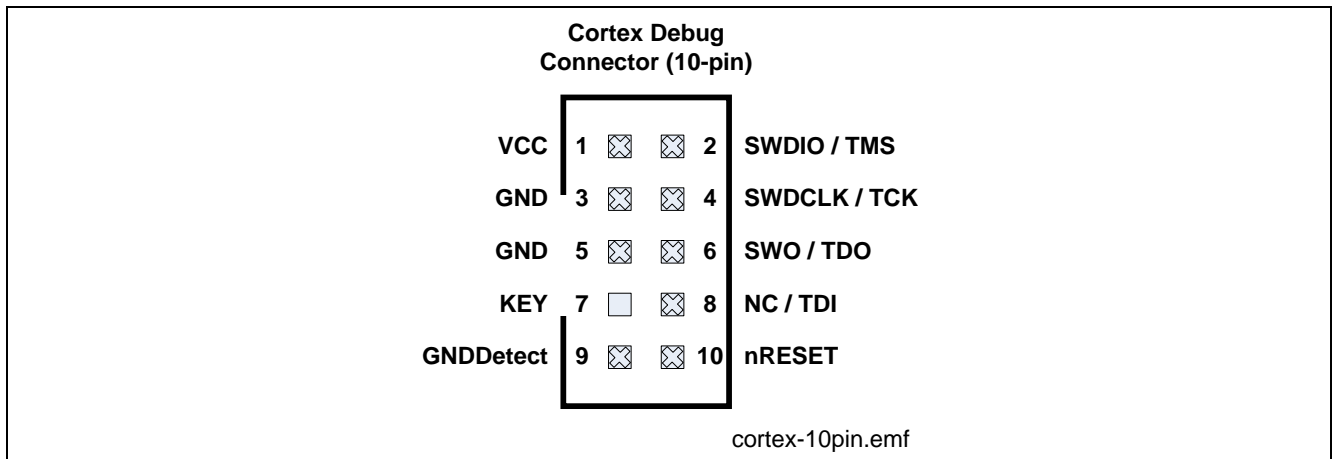


**Figure 11    Cortex Debug Connector (10-pin)**

**Table 4        Cortex Debug Connector (10 Pin)**

| Pin No. | Signal Name | Serial Wire Debug | JTAG Debug |
|---------|-------------|-------------------|------------|
| 1 | VCC | +3.3 V | +3.3 V |
| 2 | SWDIO / TMS | Serial Wire Data I/O | Test Mode Select |
| 3 | GND | Ground | Ground |
| 4 | SWDCLK / TCK | Serial Wire Clock | Test Clock |
| 5 | GND | Ground | Ground |
| 6 | SWO / TDO | Trace Data OUT | Test Data OUT |
| 7 | KEY | KEY | KEY |
| 8 | NC / TDI | Not connected | Test Data IN |
| 9 | GNDDetect | Ground Detect | Ground Detect |
| 10 | nRESET | Reset (Active Low) | Reset (Active Low) |

**Figure 12    Cortex Debug Connector (10-pin) Layout**

## 2.5.3    Cortex Debug+ETM Connector (20-pin)

The CPU_45B-V1 board supports Serial Wire Debug operation and Instruction Trace operation through the 20-pin Cortex Debug+ETM Connector.

The board does not support Serial Wire Viewer operation through the Cortex Debug Connectors by default, because the required SWO pin mapped to P2.1 is used for the connection to the on-board SDRAM. If Serial Wire Viewer operation is required anyway the resistor R404 needs to be assembled.

JTAG operation additionally would require the TDI (P0.7) signal. By default the TDI signal is disconnected from the Cortex Debug Connectors by a not assembled resistor R410, because the pin P0.7 can be used by the on-board SDRAM, by Actuator boards connected to the ACT satellite connector and by boards connected to the COM satellite connector.



**Figure 13    Cortex Debug+ETM Connector (20-pin)**

**Table 5        Cortex Debug+ETM Connector (20 Pin)**

| Pin No. | Signal Name | Serial Wire Debug | JTAG Debug |
|---------|-------------|-------------------|------------|
| 1 | VCC | +3.3 V | +3.3 V |
| 2 | SWDIO / TMS | Serial Wire Data I/O | Test Mode Select |
| 3 | GND | Ground | Ground |
| 4 | SWDCLK / TCK | Serial Wire Clock | Test Clock |
| 5 | GND | Ground | Ground |
| 6 | SWO / TDO | Trace Data OUT | Test Data OUT |
| 7 | KEY | KEY | KEY |
| 8 | NC / TDI | Not connected | Test Data IN |
| 9 | GNDDetect | Ground Detect | Ground Detect |
| 10 | nRESET | Reset (Active Low) | Reset (Active Low) |
| 11 | GND/TgtPwr+Cap | Ground | Ground |
| 12 | TRACECLK | Trace Clock | Trace Clock |
| 13 | GND/TgtPwr+Cap | Ground | Ground |
| 14 | TRACEDATA[0] | Trace Data 0 | Trace Data 0 |
| 15 | GND | Ground | Ground |
| 16 | TRACEDATA[1] | Trace Data 1 | Trace Data 1 |
| 17 | GND | Ground | Ground |
| 18 | TRACEDATA[2] | Trace Data 2 | Trace Data 2 |
| 19 | GND | Ground | Ground |
| 20 | TRACEDATA[3] | Trace Data 3 | Trace Data 3 |
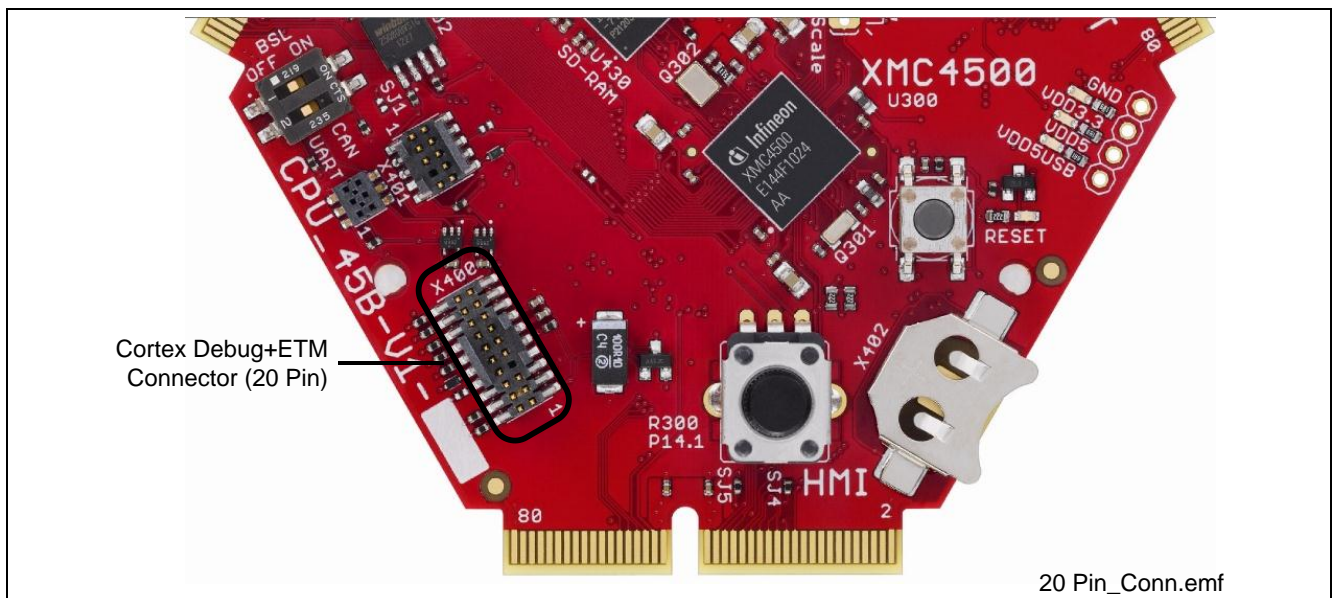


**Figure 14        Cortex Debug+ETM Connector (20-pin) Layout**

## 2.6 Serial Flash Memory

The CPU_45B-V1 board has 32Mbit serial flash memory interfaced to XMC4500 through a SPI interface. The SPI interface can be configured as single, dual or quad SPI.

**Table 6      Quad SPI Signals**

| Pin No. | Signal Name | Signal Description |
|---------|-------------|--------------------|
| P0.13 | CLK | Clock |
| P3.3 | CS# | Active Low Chip Select |
| P3.15 | DI | Data Input of Flash (MTSR) |
| P3.14 | DO | Data Output of Flash (MRST) |
| P0.14 | Data I/O | Data Input/Output |
| P0.15 | Data I/O | Data Input/Output |
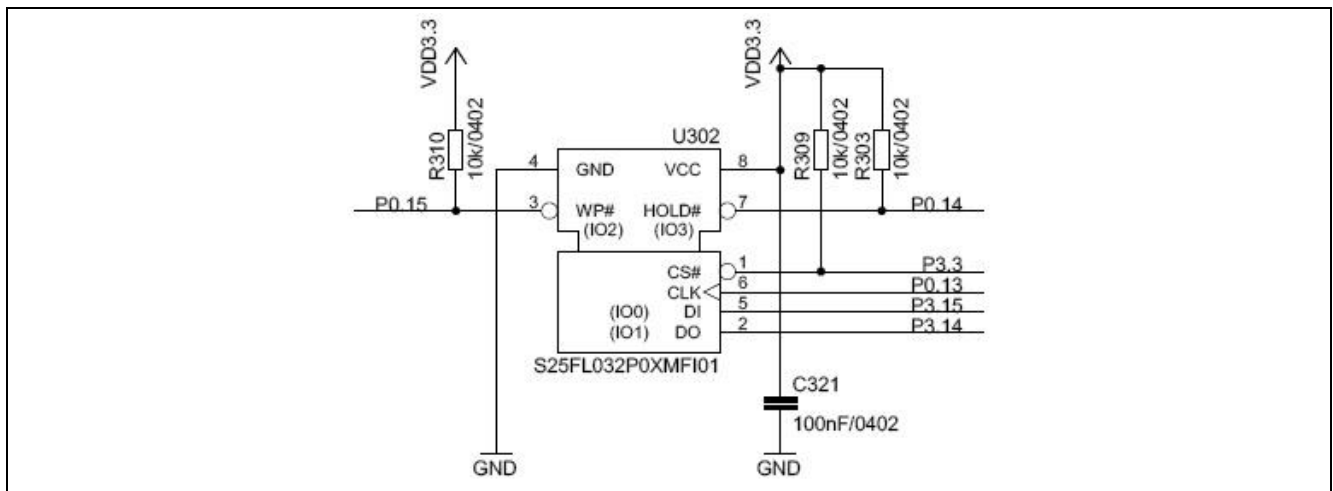


**Figure 15     Quad SPI Flash Interface**

## 2.7 SDRAM

The CPU_45B-V1 board has a 64 Mbit SDRAM interfaced to the XMC4500. The SDRAM interface is shown in Figure 16.
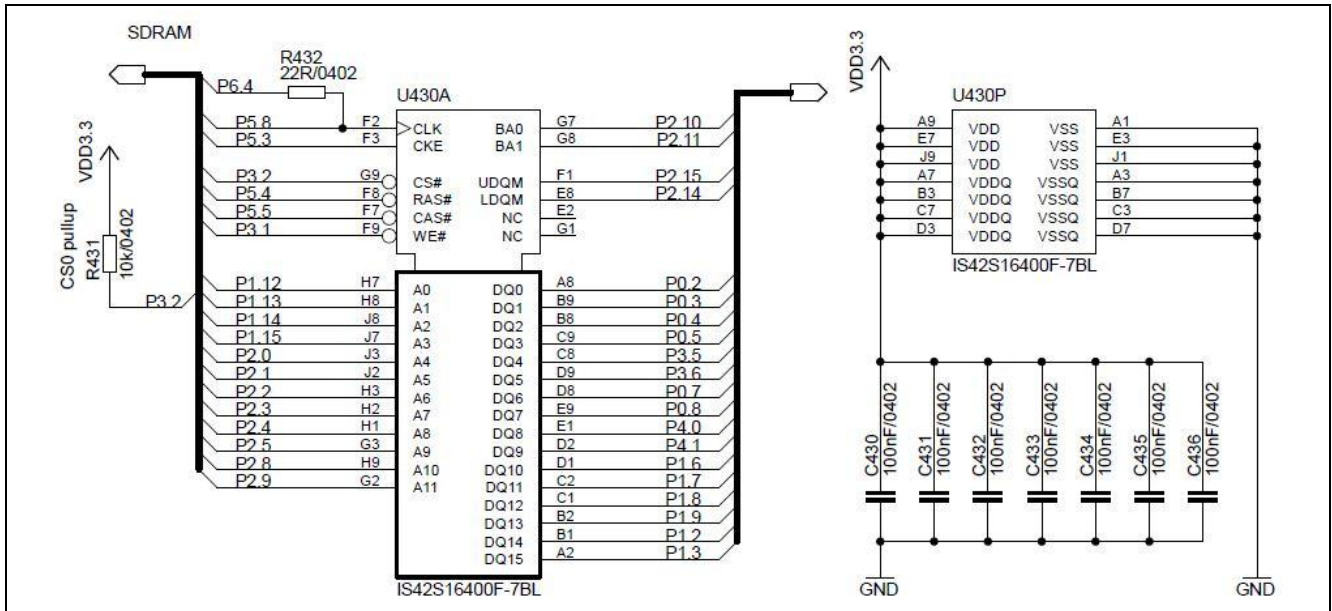


**Figure 16    SDRAM Interface**

## 2.8 USB

The XMC4500 supports USB interface in host only mode, device only mode or as an OTG Dual Role Device (DRD). In USB device mode, power is expected through VBUS (pin 1 of X203) from an external host (e.g. PC).

When the current consumption of the application running on the Hexagon Application system is higher than 500 mA, power from an external source through satellite cards shall be used.

*Note: Some PCs, notebooks or hubs have a weak USB supply which is not sufficient for proper supply. In this case use an external 5 Volt power supply or a powered USB hub.*
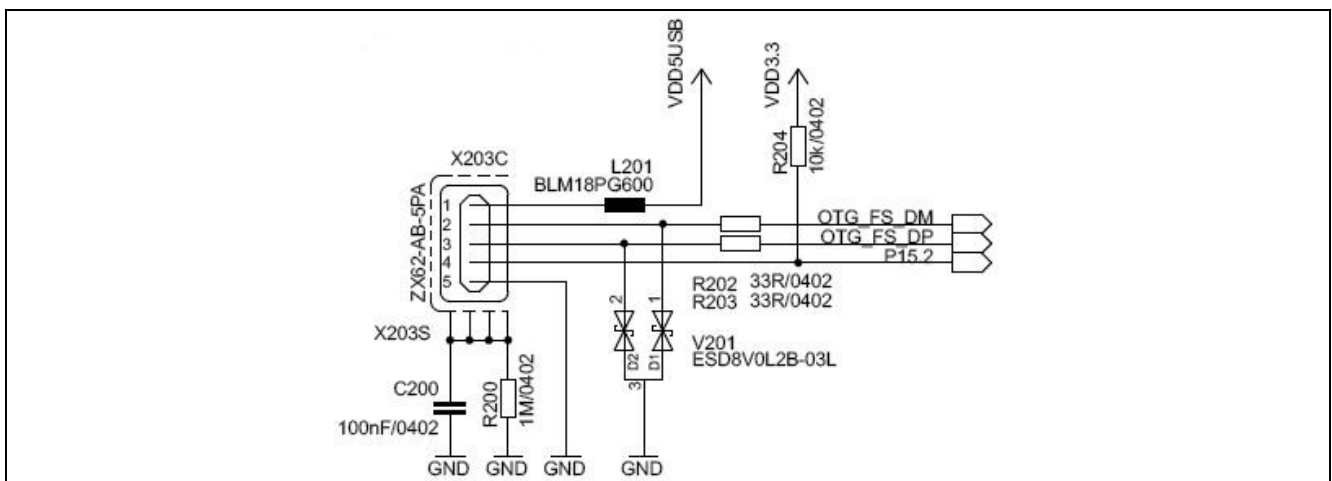


**Figure 17    USB Connector**

The USB ID pin of the USB connector is connected to the port pin P15.2 of the XMC4500. This pin must be polled by software, because this pin does not support USB_ID detection.
An OTG device will detect whether a USB 3.0 Micro-A or Micro-B plug is inserted by checking the ID pin. When the ID = FALSE, Micro-A connector is plugged and when ID = TRUE a Micro-B connector is plugged in. When ID is true the XMC4500 acts as USB host else as USB device.

**Table 7        USB micro AB connector Pinout**

| Pin No. | Pin Name | Pin Description |
|---------|----------|-----------------|
| 1 | VBUS | 5 V |
| 2 | D- | Data Minus |
| 3 | D+ | Data Plus |
| 4 | ID | Identification |
| 5 | GND | Ground |
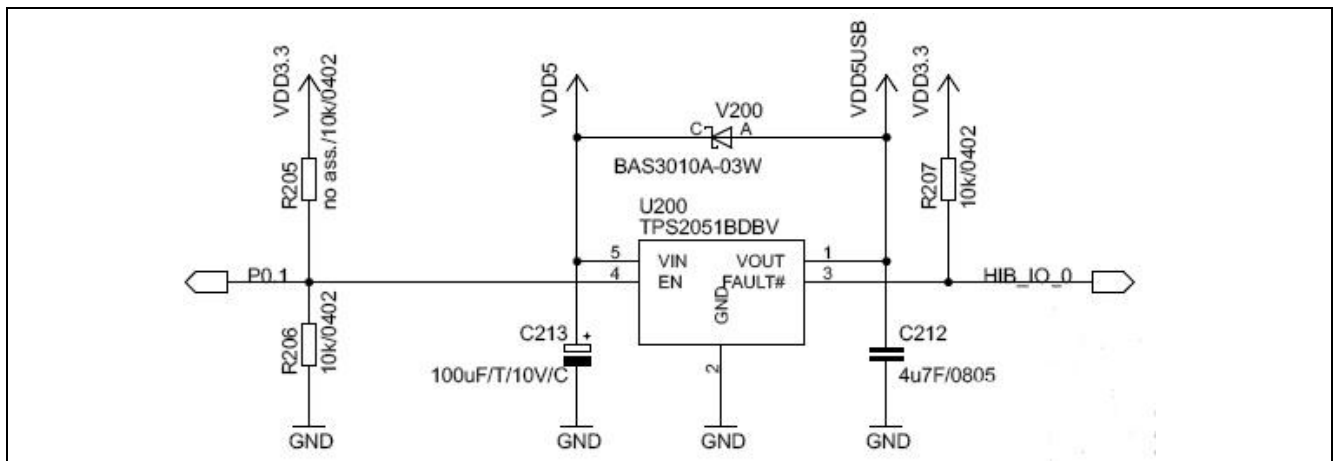


**Figure 18        USB power generation - Host/OTG mode**

In the host only mode and OTG mode the CPU_45B-V1 board is capable of supplying power to the connected device (e.g. USB mouse). The board has a power-switch which is controlled by the USB.BUSDRIVE signal of XMC4500. USB.BUSDRIVE is mapped to Port P0.1 (active high).

In the Host/OTG mode a low active FAULT signal indicates to XMC4500 via HIB_IO_0 signal, if more than 500 mA current is drawn by the external device. HIB_IO_0 signal is used as general purpose input pin for this implementation.

Diode V200 will allow powering the board through USB in all USB modes via e.g. a PC.

## 2.9 RTC

The XMC4500 CPU has two power domains, the Core Domain and Hibernate Domain.

The Core Domain (VDDP pins) is connected to the VDD3.3 rail. An on-board LDO voltage regulator generates VDD3.3 (3.3 V) from VDD5 (5 V).

The Hibernate Domain is powered via the auxiliary supply pin VBAT, which is supplied by either a 3 V coin cell (size 1216, 1220, 1225) plugged into the battery holder or 3.3 V (VDD3.3) generated by the on-board voltage regulator.



Batt.emf

**Figure 19    Battery Holder for Coin Cells**

The Real Time Clock (RTC) is located in the hibernate domain. The XMC4500 uses the HIB_IO_1 signal (active low) to shutdown the external LDO voltage regulator which generates VDD3.3 (core domain). Even if the Core Domain is not powered the Hibernate Domain will operate if VBAT is available. The RTC keeps running as long as the Hibernate Domain is powered via the auxiliary supply VBAT. The RTC is capable to wake-up the whole system from Hibernate mode by setting HIB_IO_1 to high.



RTC.emf
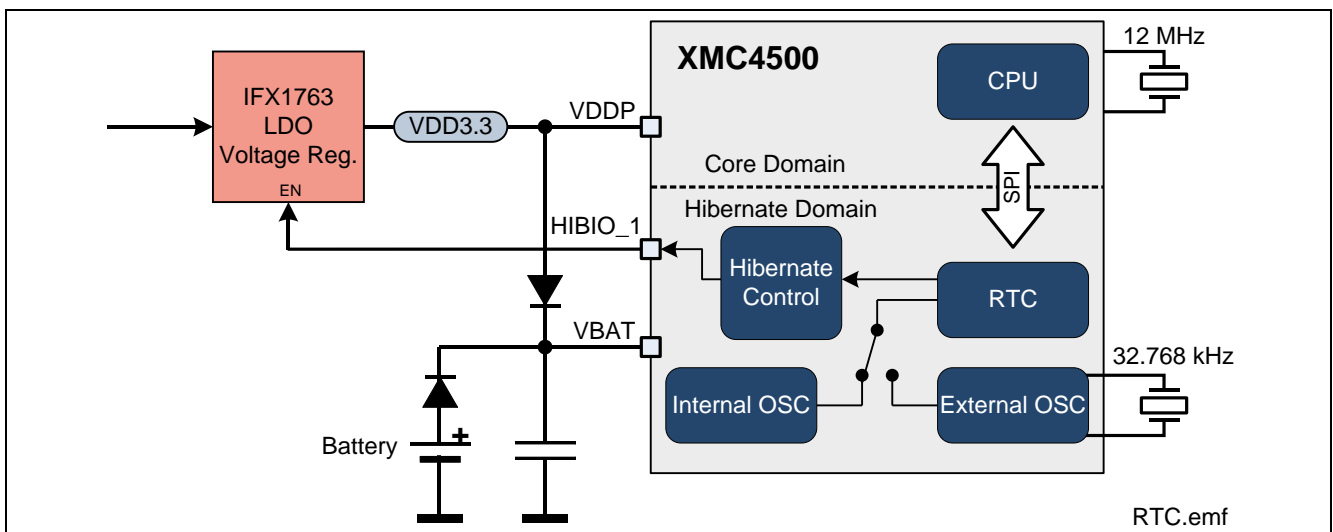
**Figure 20    XMC4500 Power Domains and Real Time Clock**

## 2.10 User LEDs and User Button

The port pins P5.2 and P1.1 of XMC4500 on the CPU_45B-V1 board are connected to the LEDs V300 and V301 respectively. More User LED's are available through the I2C GPIO expander on most of the satellite cards.

**Table 8        User LEDs**

| LED | Connected to Port Pin |
|---|---|
| LED1 / V300 | GPIO P5.2 |
| LED2 / V301 | GPIO P1.1 |

Two User Buttons, SW401 and SW402 are connected to P5.10 and P0.10 of XMC4500

**Table 9        User Buttons**

| Button | Connected to Port Pin |
|---|---|
| Button1 / SW401 | GPIO P5.10 |
| Button2 / SW402 | GPIO P0.10 |
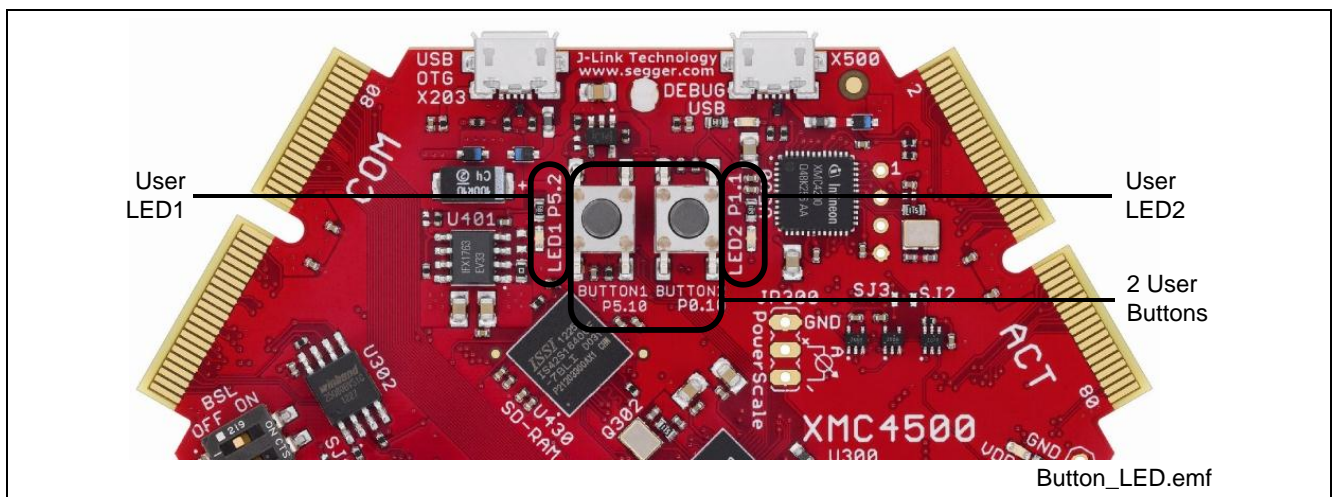


**Figure 21    User LEDs and User Buttons**

## 2.11 Potentiometer

The CPU_45B-V1 board provides a potentiometer for ease of use and testing of the on-chip analog to digital converter. The potentiometer is connected to the analog input G0_CH1 (P14.1). The analog output of the potentiometer ranges from 0 V to 3.3 V.

**Table 10      Potentiometer**

| Potentiometer | Connected to Port Pin |
|---|---|
| R300 | P14.1/ G0_CH1 (Group 0, channel 1) |

## 2.12 Satellite Connectors

The CPU_45B-V1 board provides three satellite connectors for application expansion by satellite cards:

- COM satellite connector (Communication)
- HMI satellite connector (Human Machine Interface)
- ACT satellite connector (Actuator)

*Note: Satellite cards shall be connected to their matching connectors only. (For e.g. COM satellite cards shall be connected to COM satellite connector only)*



**Figure 22    Satellite Connectors**

## 2.12.1 COM Connector

The COM satellite connector on the CPU_45B-V1 board allows interface expansion through COM satellite cards (e.g. COM_ETH-V1)

**Left block (COM pins 1–44)**

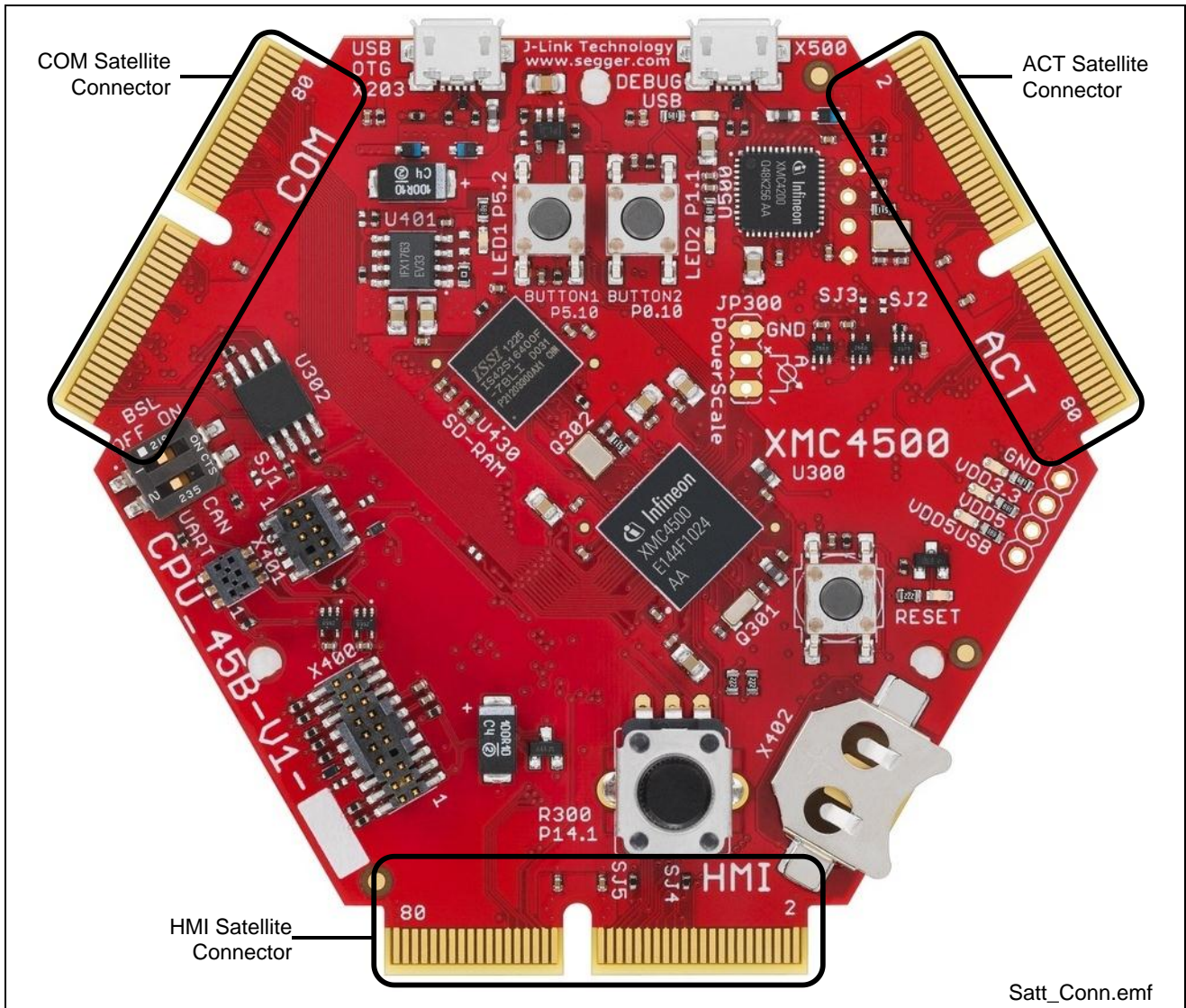| COM (even) | XMC Pin (top) | XMC Function (top) | Sat Function (top) | Sat Function (bot) | XMC Function (bot) | XMC Pin (bot) | COM (odd) |
|---|---|---|---|---|---|---|---|
| 2 | VSS | GND | GND | GND | GND | VSS | 1 |
| 4 | P3.15 | U1C1_DOUT0 | qSPI_D0 | qSPI_SCLK | U1C1_SCLKOUT | P0.13 | 3 |
| 6 | P3.14 | U1C1_DOUT1 | qSPI_D1 | qSPI_CS | U1C1_SELO0 | P0.12 | 5 |
| 8 | P0.15 | U1C1_DOUT2 | qSPI_D2 | qSPI_CS | U1C1_SELO1 | P3.3 * | 7 |
| 10 | P0.14 | U1C1_DOUT3 | qSPI_D3 | RSVD | nc | nc | 9 |
| 12 | nc | nc | RSVD | RSVD | nc | nc | 11 |
| 14 | P2.13 | ETH0_TXD1 | ETH_RMII | ETH_RMII | ETH0_RXD1D | P5.1 | 13 |
| 16 | P2.12 | ETH0_TXD0 | ETH_RMII | ETH_RMII | ETH0_RXD0D | P5.0 | 15 |
| 18 | P15.9 | ETH0_CRS_DVC | ETH_RMII | ETH_RMII | ETH0_MDO | P1.11 | 17 |
| 20 | P0.11 | ETH0_RXERB | ETH_RMII | ETH_RMII | ETH0_MDC | P1.10 | 19 |
| 22 | P15.8 | ETH0_CLK_RMIIC | ETH_RMII | ETH_RMII | ETH0_TX_EN | P5.9 | 21 |
| 24 | VSS | GND | GND | RSVD | nc | nc | 23 |
| 26 | nc | nc | RSVD | ASC_DIR | nc | nc | 25 |
| 28 | P2.7 | CAN_N1_TXD | CAN_TXD | ASC_RXD | U0C0_DX0B | P1.4 ** | 27 |
| 30 | P2.6 | CAN_N1_RXDA | CAN_RXD | ASC_TXD | U0C0_DOUT0 | P1.5 ** | 29 |
| 32 | nc | nc | SPI_MTSR | SPI_CSC0 | nc | nc | 31 |
| 34 | nc | nc | SPI_MRST | SPI_CSC1 | nc | nc | 33 |
| 36 | nc | nc | SPI_SCLK | SPI_CSC2 | nc | nc | 35 |
| 38 | P3.13 | U2C1_SCLKOUT | I2C_SCL | I2C_SDA | U2C1_DOUT0/DX0D | P3.11/P3.12 | 37 |
| 40 | P6.3 | P6.3 | GPIO | COM_GPIO1 | P14.13 | P14.13 | 39 |
| 42 | PORST | RESET# | RESET | COM_GPIO0 | P0.0 | P0.0 | 41 |
| 44 |  |  | VDD5 | VDD5 |  |  | 43 |

**Right block (COM pins 45–80)**

| COM (even) | XMC Pin (top) | XMC Function (top) | Sat Function (top) | Sat Function (bot) | XMC Function (bot) | XMC Pin (bot) | COM (odd) |
|---|---|---|---|---|---|---|---|
| 46 |  |  | VDD5 | VDD5 |  |  | 45 |
| 48 | P0.2 | EBU_AD0 | EBU_AD | EBU_ADV | EBU_nADV | P0.6 | 47 |
| 50 | P0.3 | EBU_AD1 | EBU_AD | EBU_WR | EBU_RD/EBU_nWR | P3.1 | 49 |
| 52 | P0.4 | EBU_AD2 | EBU_AD | EBU_RD | EBU_RD | P3.0 | 51 |
| 54 | P0.5 | EBU_AD3 | EBU_AD | EBU_BC | EBU_nBC1 | P2.15 | 53 |
| 56 | P3.5 | EBU_AD4 | EBU_AD | EBU_BC | EBU_nBC0 | P2.14 | 55 |
| 58 | P3.6 | EBU_AD5 | EBU_AD | EBU_CS | EBU_nCS1 | nc | 57 |
| 60 | P0.7 | EBU_AD6 | EBU_AD | EBU_CS |  | P0.9 | 59 |
| 62 | P0.8 | EBU_AD7 | EBU_AD | GND | GND | VSS | 61 |
| 64 | P4.0 | EBU_AD8 | EBU_AD | EBU_A | nc | nc | 63 |
| 66 | P4.1 | EBU_AD9 | EBU_AD | EBU_A | nc | nc | 65 |
| 68 | P1.6 | EBU_AD10 | EBU_AD | EBU_A | nc | nc | 67 |
| 70 | P1.7 | EBU_AD11 | EBU_AD | EBU_A | EBU_A19 | P6.4 | 69 |
| 72 | P1.8 | EBU_AD12 | EBU_AD | EBU_A | EBU_A18 | P6.2 | 71 |
| 74 | P1.9 | EBU_AD13 | EBU_AD | EBU_A | EBU_A17 | P6.1 | 73 |
| 76 | P1.2 | EBU_AD14 | EBU_AD | EBU_A | EBU_A16 | P6.0 | 75 |
| 78 | P1.3 | EBU_AD15 | EBU_AD | EBU_A |  |  | 77 |
| 80 | VSS | GND | GND | GND | GND | VSS | 79 |

CPU side: CPU_45B-V1 (SDRAM) — XMC Pin / XMC Function. Middle: Satellite Connector — Function / Pin (COM) / Function.

**Figure 23 Satellite Connector Type COM**

*Attention: * This pin is used as chip select signal for the on-board EEPROM and therefore disconnected by solder jumper SJ1*

*Attention: ** This pin is connected with the satellite connector via an analog switch*

## 2.12.2    HMI Connector

The HMI satellite connector on the CPU_45B-V1 board allows interface expansion through HMI satellite cards.



The figure lists the HMI Satellite Connector pinout. The connector columns are: CPU_45B-V1 (SDRAM) XMC Pin and XMC Function, the Satellite Connector Function, the HMI Pin, and the CPU_45B-V1 (SDRAM) XMC Function and XMC Pin. The pin assignments are:

| Pin | Satellite Connector Function | CPU XMC Function | CPU XMC Pin |
|---|---|---|---|
| 1 | GND | GND | VSS |
| 2 | GND | GND | VSS |
| 3 | MMC_CLK | nc | nc |
| 4 | MMC_nRST | nc | nc |
| 5 | MMC_DATA1 | nc | nc |
| 6 | MMC_DATA0 | nc | nc |
| 7 | MMC_DATA3 | nc | nc |
| 8 | MMC_DATA2 | nc | nc |
| 9 | MMC_DATA5 | nc | nc |
| 10 | MMC_DATA4 | nc | nc |
| 11 | MMC_DATA7 | nc | nc |
| 12 | MMC_DATA6 | nc | nc |
| 13 | MMC_BUSPOW | nc | nc |
| 14 | MMC_CMD | nc | nc |
| 15 | MMC_nSDCD | nc | nc |
| 16 | MMC_LED | nc | nc |
| 17 | RSVD | nc | nc |
| 18 | MMC_SDWC | nc | nc |
| 19 | RSVD | nc | nc |
| 20 | RSVD | nc | nc |
| 21 | RSVD | nc | nc |
| 22 | RSVD | nc | nc |
| 23 | AudioRST | P4.2 | P4.2 |
| 24 | OLED_CMD | P5.11 | P5.11 |
| 25 | I2S_WA | U1C1.SELO2 | P3.4 |
| 26 | I2S_MTSR | U1C1.DOUT0 | P3.15 |
| 27 | I2S_MCLK | nc | nc |
| 28 | I2S_MRST | U1C1.DX0B | P3.14 |
| 29 | I2S_SYNCLK | nc | nc |
| 30 | I2S_SCLK | U1C1.SCLKOUT | P0.13 |
| 31 | SPI_CSH0 | U2C0.SELO0 | P3.10 |
| 32 | SPI_MTSR | U2C0.DOUT0 | P3.8 |
| 33 | SPI_CSH1 | U2C0.SELO3 | P5.6 |
| 34 | SPI_MRST | U2C0.DX0C | P3.7 |
| 35 | SPI_CSH2 | nc | nc |
| 36 | SPI_SCLK | U2C0.SCLKOUT | P3.9 |
| 37 | I2C_SDA | U2C1_DOUT0/DX0D | P3.11/P3.12 |
| 38 | I2C_SCL | U2C1.SCLKOUT | P3.13 |
| 39 | HMI_GPIO1 | P15.5 Input | P15.5 |
| 40 | GPIO | P6.3 | P6.3 |
| 41 | HMI_GPIO0 | P5.7 | P5.7 |
| 42 | RESET | RESET# | POSRT |
| 43 | VDD5 | | |
| 44 | VDD5 | | |
| 45 | VDD5 | VDD5 | |
| 46 | VDD5 | VDD5 | |
| 47 | AGND | AGND | VAGND |
| 48 | AREF | VAREF | VAREF |
| 49 | DAC0/ADC1 | DAC.OUT1 | P14.9 |
| 50 | DAC1/ADC0 | VADC_G1CH0 | P14.8 |
| 51 | ADC3/ORC0 | nc | nc |
| 52 | ADC2/DACREF | VADC_G0CH4 | P14.4 |
| 53 | ADC15 | VADC_G1CH4 | P14.12 |
| 54 | ADC14 | VADC_G0CH3 | P14.3 |
| 55 | ADC17 | VADC_G3CH5 | P15.13 |
| 56 | ADC16 | VADC_G2CH3 | P15.3 |
| 57 | ADC19 | VADC_G3CH4 | P15.12 |
| 58 | ADC18 | nc | nc |
| 59 | RSVD | nc | nc |
| 60 | RSVD | nc | nc |
| 61 | RSVD | nc | nc |
| 62 | RSVD | nc | nc |
| 63 | RSVD | nc | nc |
| 64 | TP7 | nc | nc |
| 65 | TPx1 | nc | nc |
| 66 | TP6 | nc | nc |
| 67 | TPx0 | nc | nc |
| 68 | TP5 | nc | nc |
| 69 | COL3 | nc | nc |
| 70 | TP4 | nc | nc |
| 71 | COL2 | nc | nc |
| 72 | TP3 | nc | nc |
| 73 | COL1 | nc | nc |
| 74 | TP2 | nc | nc |
| 75 | COL0 | nc | nc |
| 76 | TP1 | nc | nc |
| 77 | COLA | nc | nc |
| 78 | TP0 | nc | nc |
| 79 | GND | GND | VSS |
| 80 | GND | GND | VSS |

**Figure 24    Satellite Connector Type HMI**

### 2.12.3 ACT Satellite Connector

The ACT satellite connector on the CPU_45B-V1 board allows interface expansion through ACT satellite cards.

**Figure 25  Satellite Connector Type ACT**

| ACT Pin | Satellite Connector Function | CPU_45B-V1 (SDRAM) XMC Function | CPU_45B-V1 (SDRAM) XMC Pin |
|---|---|---|---|
| 1 | GND | GND | VSS |
| 2 | GND | GND | VSS |
| 3 | PIF1IN0 | nc | nc |
| 4 | PIF0IN1 | PIF0_IN0B | P14.7 |
| 5 | PIF1IN1 | nc | nc |
| 6 | PIF0IN2 | PIF0_IN1B | P4.16 |
| 7 | PIF1IN2 | nc | nc |
| 8 | PIF0IN3 | PIF0_IN2B | P14.5 |
| 9 | PWMN | DSD_PWMN | P1.0 |
| 10 | DSDIN0 | nc | nc |
| 11 | PWMP | DSD_PWMP | P1.1 |
| 12 | DSDIN1 | nc | nc |
| 13 | DSDCLK0 | nc | nc |
| 14 | DSDIN2 | nc | nc |
| 15 | DSDCLK1 | DSD_MCLK3 | P6.6 (3) |
| 16 | DSDIN3 | DSD_DIN3A | P6.5 (3) |
| 17 | RSVD | nc | nc |
| 18 | RSVD | nc | nc |
| 19 | CC_IN3 | nc | nc |
| 20 | CC_IN0 | nc | nc |
| 21 | CC_IN4 | nc | nc |
| 22 | CC_IN1 | nc | nc |
| 23 | CC_IN5 | nc | nc |
| 24 | CC_IN2 | nc | nc |
| 25 | TRAP_A | nc | nc |
| 26 | ENA_A | nc | nc |
| 27 | TRAP_B | nc | nc |
| 28 | ENA_B | nc | nc |
| 29 | TRAP_X | nc | nc |
| 30 | ENA_X | nc | nc |
| 31 | SPI_CSA0 | U2C0.SELO3 | P5.6 (5) |
| 32 | SPI_MTSR | U2C0.DOUT0 | P3.8 |
| 33 | SPI_CSA1 | U2C0.SELO0 | P3.10 (5) |
| 34 | SPI_MRST | U2C0.DX0C | P3.7 |
| 35 | SPI_CSA2 | U2C1_DOUT0/DX0D | P3.11/P3.12 |
| 36 | SPI_SCLK | U2C0.SCLKOUT | P3.9 |
| 37 | I2C_SDA | P15.4 Input | P15.4 |
| 38 | I2C_SCL | U2C1.SCLKOUT | P3.13 |
| 39 | ACT_GPIO1 | P4.7 | P4.7 |
| 40 | GPIO | P6.3 | P6.3 |
| 41 | ACT_GPIO0 |  |  |
| 42 | RESET | RESET# | PORTS |
| 43 | VDD5 |  |  |
| 44 | VDD5 |  |  |
| 45 | VDD5 | AGND | VAGND |
| 46 | VDD5 | VAREF | VAREF |
| 47 | AGND | VADC_G1CH1 | P14.9 |
| 48 | AREF | VADC_G1CH0 | P14.8 |
| 49 | DAC0/ADC1 | nc | nc |
| 50 | DAC1/ADC0 | VADC_G0CH4 | P14.4 |
| 51 | ADC3/ORC0 | VADC_G0CH0 | P14.0 |
| 52 | ADC2/DACREF | VADC_G1CH6 | P14.14 |
| 53 | ADC5/ORC2 | VADC_G3CH6 | P15.14 |
| 54 | ADC4/ORC1 | VADC_G1CH7 | P14.15 |
| 55 | ADC7 | VADC_G3CH7 | P15.15 |
| 56 | ADC6/ORC3 | VADC_G0CH2 | P14.2 |
| 57 | ADC9 | nc | nc |
| 58 | ADC8 | VADC_G2CH6 | P15.6 |
| 59 | ADC11 | nc | nc |
| 60 | ADC10 | VADC_G2CH7 | P15.7 |
| 61 | ADC13 | nc | nc |
| 62 | ADC12 | nc | nc |
| 63 | PWMB0_H | nc | nc |
| 64 | PWMA0_H | nc | nc |
| 65 | PWMB0_L | nc | nc |
| 66 | PWMA0_L | nc | nc |
| 67 | PWMB1_H | nc | nc |
| 68 | PWMA1_H | nc | nc |
| 69 | PWMB1_L | nc | nc |
| 70 | PWMA1_L | nc | nc |
| 71 | PWMB2_H | nc | nc |
| 72 | PWMA2_H | nc | nc |
| 73 | PWMB2_L | nc | nc |
| 74 | PWMA2_L | nc | nc |
| 75 | PWMX2 | CCU43OUT0 | P4.6 |
| 76 | PWMX0 | CCU43OUT2 | P4.4 |
| 77 | PWMX3 | CCU43OUT1 | P4.5 |
| 78 | PWMX1 | CCU43OUT3 | P4.3 |
| 79 | GND | GND | VSS |
| 80 | GND | GND | VSS |

(1) P0.7 can also be used for JTAG Debugging (TDI)

(2) P0.8 is used as TRST in order to enable JTAG Debug

(3) This pin is connected with the satellite connector via an analog switch

(4) This ADC input does not support "Out of Range Detection"

(5) This pin is disconnected by a solder jumper

(6) Support High Resolution PWM

# 3 Production Data

## 3.1 Schematics

This chapter contains the schematics for the CPU board:
- Satellite Connectors, USB-OTG
- XMC4500
- Power, Debug Connector, Reset
- On-board Debugger

The board has been designed with Eagle. The full PCB design data of this board can also be downloaded from www.infineon.com/xmc-dev.
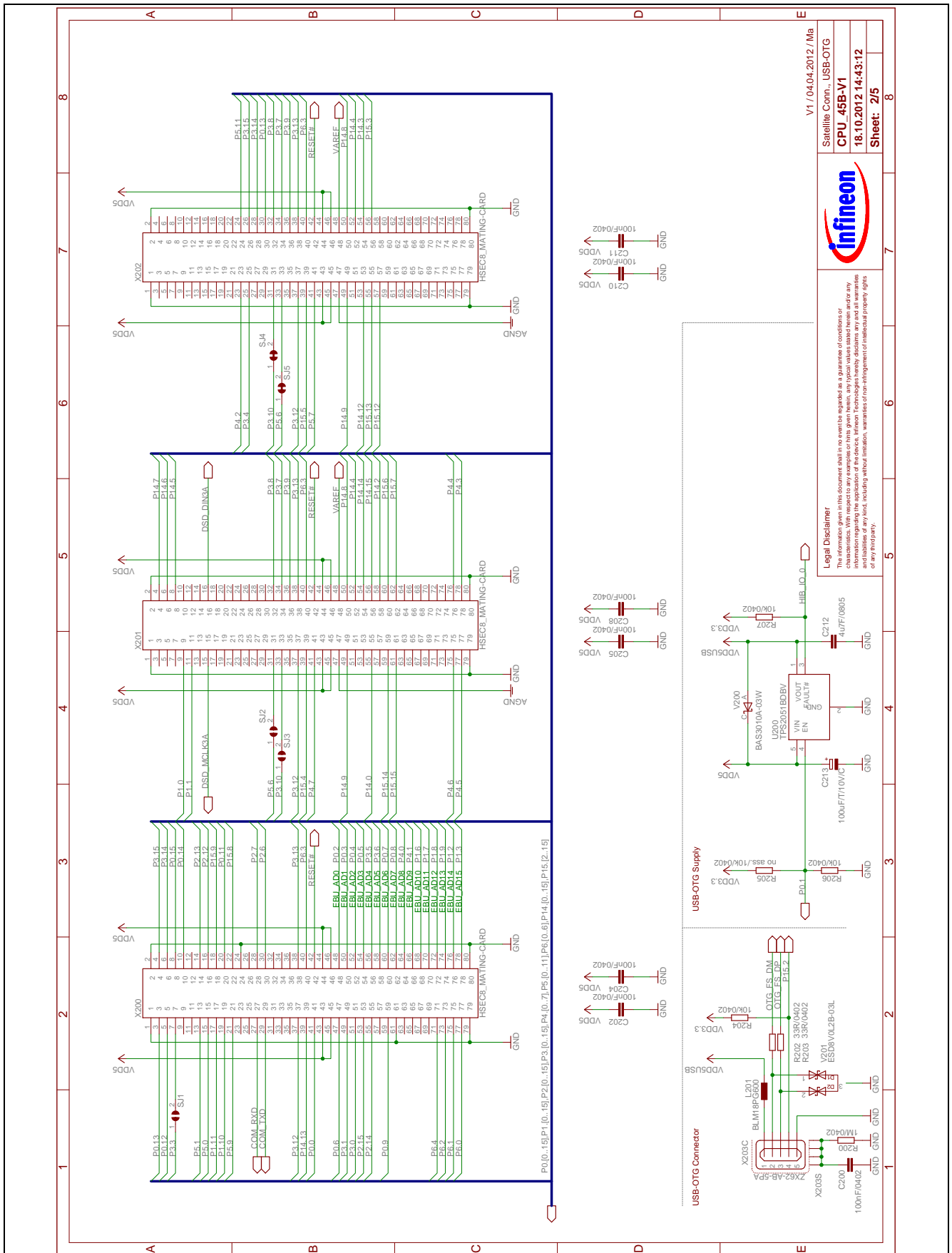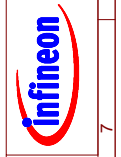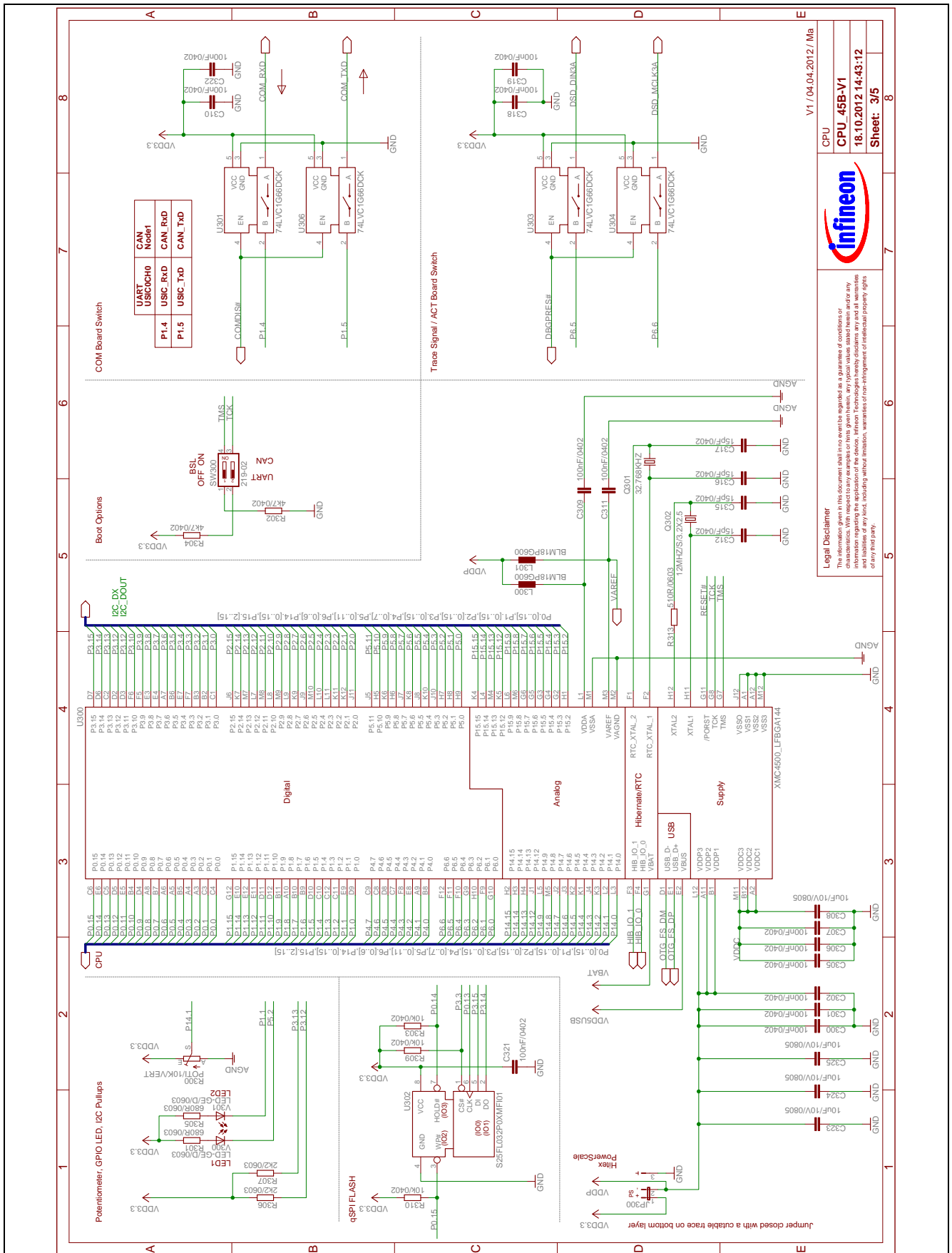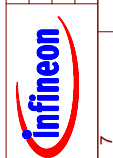
**Figure 26    Satellite Connectors, USB-OTG**
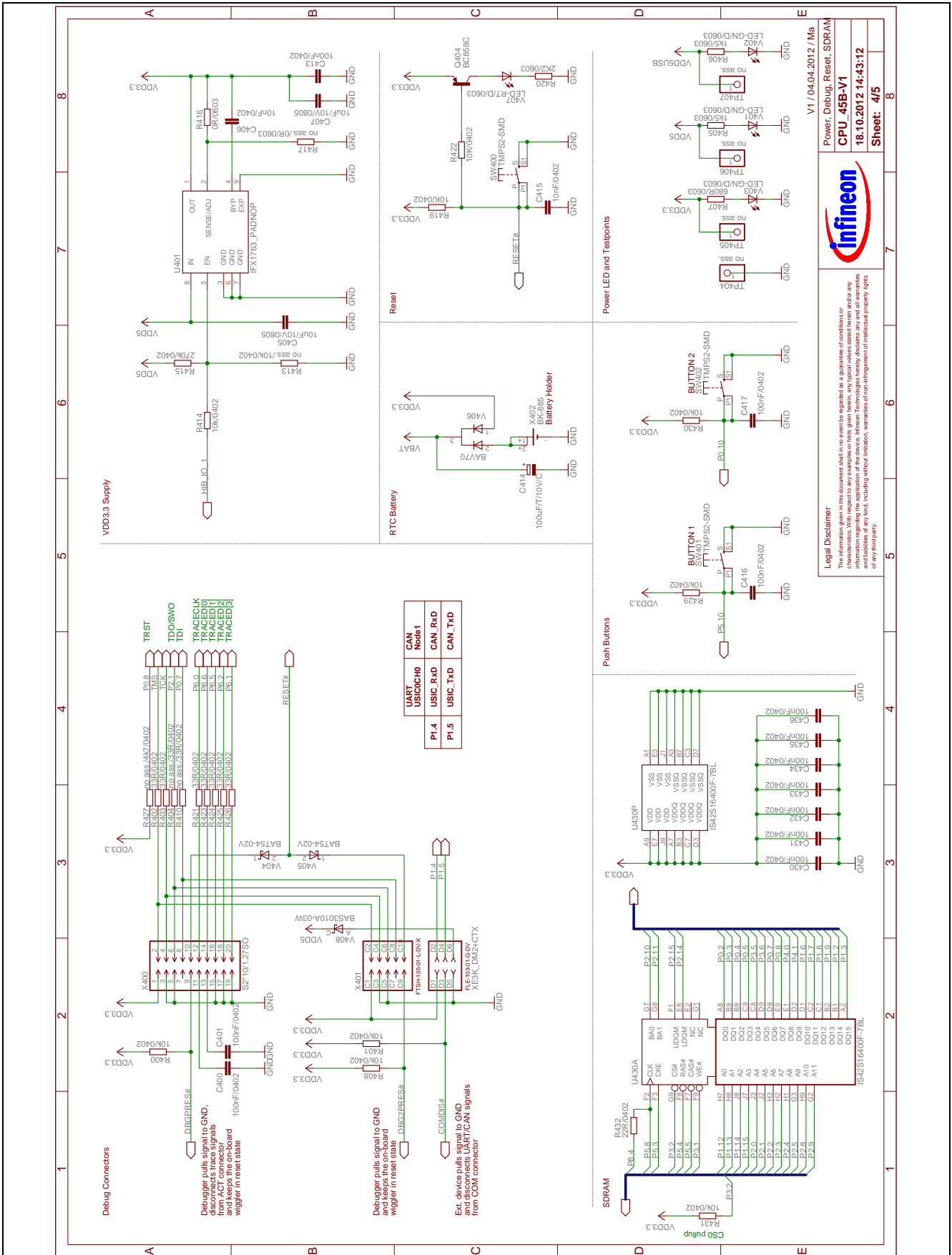
**Figure 27    XMC4500**

**Figure 28    Power, Debug Connector, Reset, SDRAM**

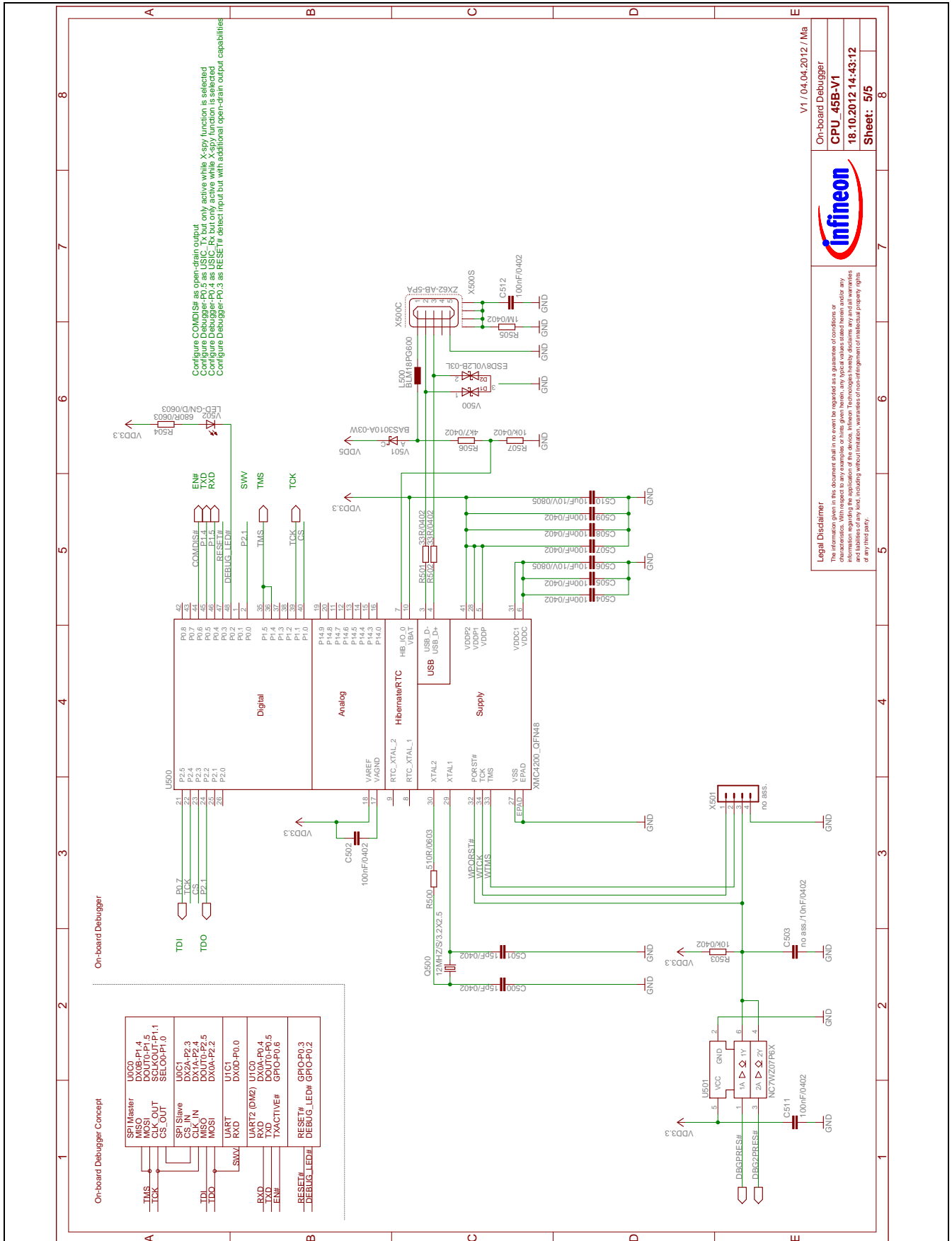**Figure 29    On-board Debugger**
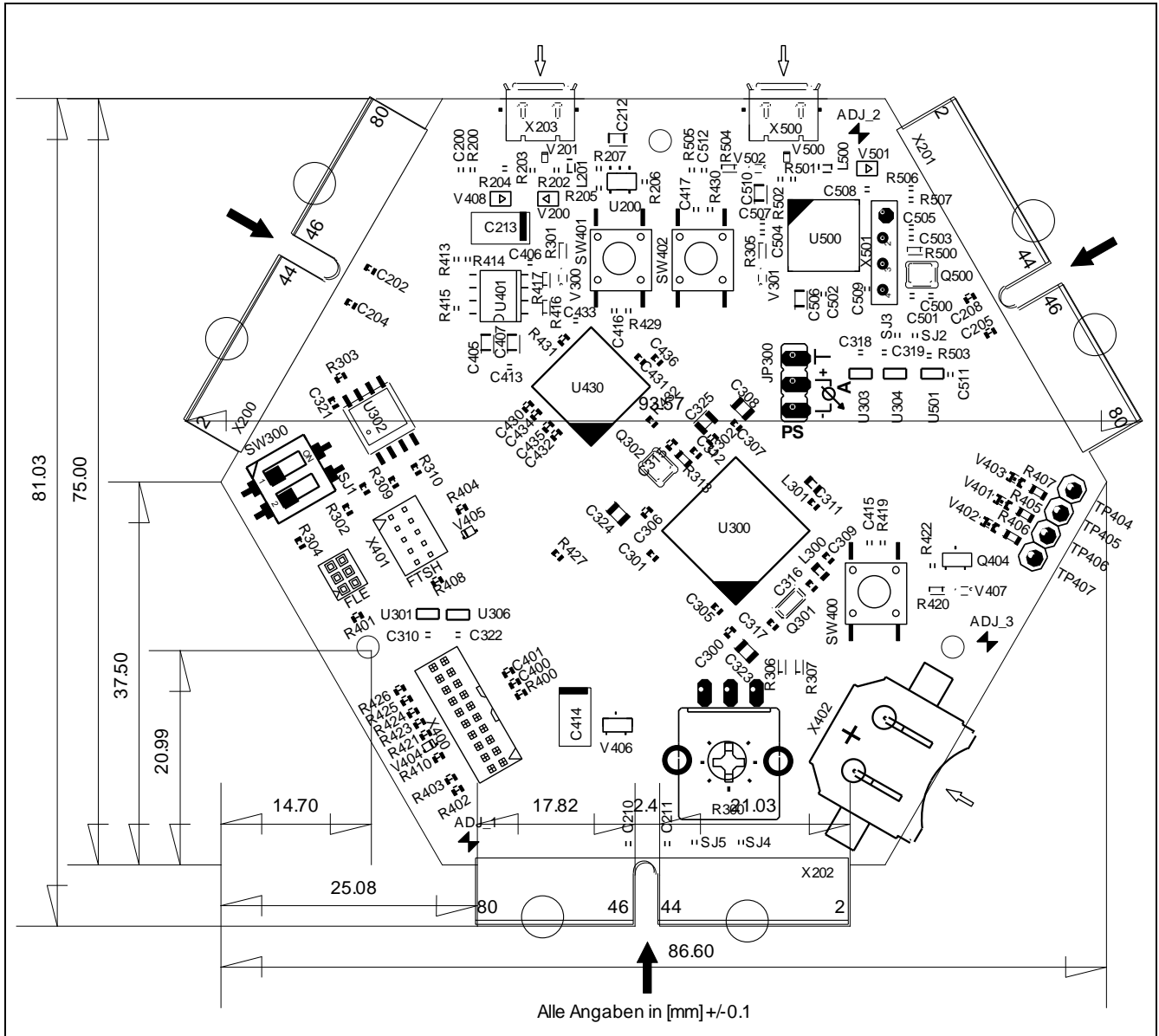
## 3.2    Component Placement and Geometry



**Figure 30    Component Placement and Geometry**

## 3.3    Bill of Material (BOM)

**Table 11    BOM of CPU_45B-V1 Board**

| Pos No. | Qty | Value | Device | Reference Des. |
|---|---|---|---|---|
| 1 | 1 | 0R/0603 | Resistor | R416 |
| 2 | 2 | 1M/0402 | Resistor | R200, R505 |
| 3 | 2 | 1k5/0603 | Resistor | R405, R406 |
| 4 | 3 | 2k2/0603 | Resistor | R306, R307, R420 |
| 5 | 3 | 4k7/0402 | Resistor | R302, R304, R506 |
| 6 | 1 | 4u7F/0805 | Capacitor, ceramic | C212 |
| 7 | 17 | 10k/0402 | Resistor | R204, R206, R207, R303, R309, R310, R400, R401, R408, R414, R419, R422, R429, R430, R431, R503, R507 |
| 8 | 2 | 10nF/0402 | Capacitor | C406, C415 |
| 9 | 8 | 10uF/10V/0805 | Capacitor, ceramic | C308, C323, C324, C325, C405, C407, C506, C510 |
| 10 | 2 | 12MHZ/S/3.2X2.5 | Crystal, NX3225GD, NDK | Q302, Q500 |
| 11 | 6 | 15pF/0402 | Capacitor | C312, C315, C316, C317,C500, C501 |
| 12 | 1 | 22R/0402 | Resistor | R432 |
| 13 | 1 | 32.768KHZ | Crystal, NX3215SA, NDK | Q301 |
| 14 | 11 | 33R/0402 | Resistor | R202, R203, R402, R403, R421, R423, R424, R425, R426, R501, R502 |
| 15 | 4 | 74LVC1G66DCK | IC, Single Analog Switch | U301, U303, U304, U306 |
| 16 | 40 | 100nF/0402 | Capacitor | C200, C202, C204, C205, C208, C210, C211, C300, C301, C302, C305, C306, C307, C309, C310, C311, C318, C319, C321, C322, C413, C416, C417, C430, C431, C432, C433, C434, C435, C436, C400, C401, C502, C504, C505, C507, C508, C509, C511, C512 |
| 17 | 2 | 100uF/T/10V/C | Capacitor, bipolar | C213, C414 |
| 18 | 1 | 219-02 | Dual DIP-Switch, 0.1" SMD | SW300 |
| 19 | 1 | 270k/0402 | Resistor | R415 |
| 20 | 2 | 510R/0603 | Resistor | R313, R500 |
| 21 | 4 | 680R/0603 | Resistor | R301, R305, R407, R504 |
| 22 | 3 | BAS3010A-03W | Diode, SOD323, Infineon | V200, V408, V501 |
| 23 | 2 | BAT54-02V | Diode, SC79, Infineon | V404, V405 |
| 24 | 1 | BAV70 | Diode, SOT23-3, Infineon | V406 |
| 25 | 1 | BC858C | Transistor, SOT23-3, Infineon | Q404 |

| 26 | 1 | BK-885 | Battery Holder, 12mm Coin Cell | X402 |
|----|---|--------|--------------------------------|------|
| 27 | 4 | BLM18PG600 | Ferrite Bead, 0603, Murata | L201, L300, L301, L500 |
| 28 | 2 | ESD8V0L2B-03L | Diode, TSLP-3-1, Infineon | V201, V500 |
| 29 | 3 | HSEC8_MATING-CARD | Connector, Edgecard, Samtec | X200, X201, X202 |
| 30 | 1 | IFX1763_PADNOP | Voltage Regulator, 3.3V LDO, Infineon | U401 |
| 31 | 2 | LED-GE/D/0603 | LED, yellow | V300, V301 |
| 32 | 4 | LED-GN/D/0603 | LED, green | V401, V402, V403, V502 |
| 33 | 1 | LED-RT/D/0603 | LED, red | V407 |
| 34 | 1 | IS42S16400F-7BL | Synchronous Dynamic RAM, ISSI | U430 |
| 35 | 1 | NC7WZ07P6X | IC, Dual Buffer OD, SC70-6 | U501 |
| 36 | 1 | POTI/10K/VERT | Potentiometer, K09K1130A8G, ALPS | R300 |
| 37 | 1 | S2*10/1.27SO | Connector, FTSH-110-01-L-DV-K-P, Samtec | X400 |
| 38 | 1 | S25FL032P0XMFI01 | IC, qSPI Flash Memory, SPANSION | U302 |
| 39 | 3 | TMPS2-SMD | Switch, tactile | SW400, SW401, SW402 |
| 40 | 1 | TPS2051BDBV | IC, Power Switch, SOT23-5 | U200 |
| 41 | 1 | XE3K_DM2+CTX | Connector, FTSH-105-01-LM-DV-K, w/o pin 7, Samtec Connector, FLE-103-01-G-DV, Samtec | X401 |
| 42 | 1 | XMC4200_QFN48 | IC, XMC4200, QFN48, Infineon | U500 |
| 43 | 1 | XMC4500_LFBGA144 | IC, XMC4500, LFBGA144, Infineon | U300 |
| 44 | 2 | ZX62-AB-5PA | Connector, Micro-USB, Hirose | X203, X500 |
| 45 | 1 | no ass. | Pinheader, 4-pin, 0.1" TH | X501 |
| 46 | 4 | no ass. | Pinheader, 1-pin, 0.1" TH | TP404, TP405, TP406, TP407 |
| 47 | 1 | no ass./0R/0603 | Resistor | R417 |
| 48 | 1 | no ass./4k7/0402 | Resistor | R427 |
| 49 | 2 | no ass./10k/0402 | Resistor | R205, R413 |
| 50 | 1 | no ass./10nF/0402 | Capacitor | C503 |
| 51 | 2 | no ass./33R/0402 | Resistor | R404, R410 |
| 52 | 1 | no ass. | Pinheader, 3-pin, 0.1" TH, Hitex PowerScale | JP300 |
| 53 | 3 | no ass. | Solder Bridge (open) | SJ1, SJ2, SJ3 |
| 54 | 2 | 0R/0402 | Solder Bridge (closed by resistor) | SJ4, SJ5 |