DEVICE MODELLING LAB

Assignment-05

Q1.Simulate 2-i/p XOR Gate with the minimum number of 2-i/p NAND Gates?

Q2.Simulate 3-i/p AND Gate with the minimum number of 2-i/p NAND Gates?

Q3.Simulate 3-i/p NAND Gate with the minimum number of 2-i/p NAND Gates?

Q4.Simulate AB+C Boolean Expression using CMOS Logic?

Q5.Simulate Majority 3 Gate Using Nand Gates Only? (You are allowed to use only 2-i/p and 3-i/p NAND Gates Only)?