AIM: To plot V-I characteristics and calculate the Threshold and pinch off voltages of P-MOSFET.

Software used: Cadence Virtuoso

Experimental Procedure:

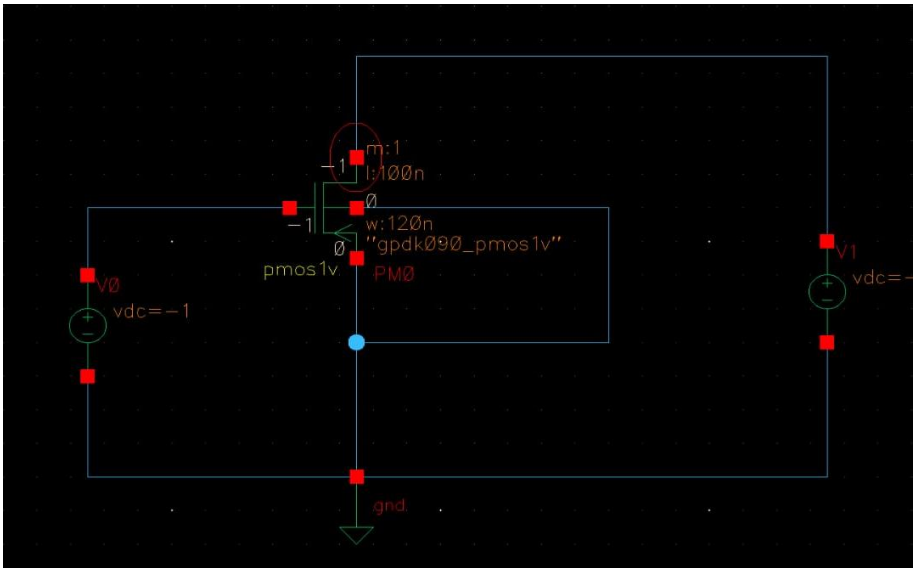
1. Invoke Cadence Virtuoso tool

2. Construct the schematic of P-MOSFET as Shown

3. Invoke ADEL tool for simulations. Perform DC analysis in order to plot transfer and

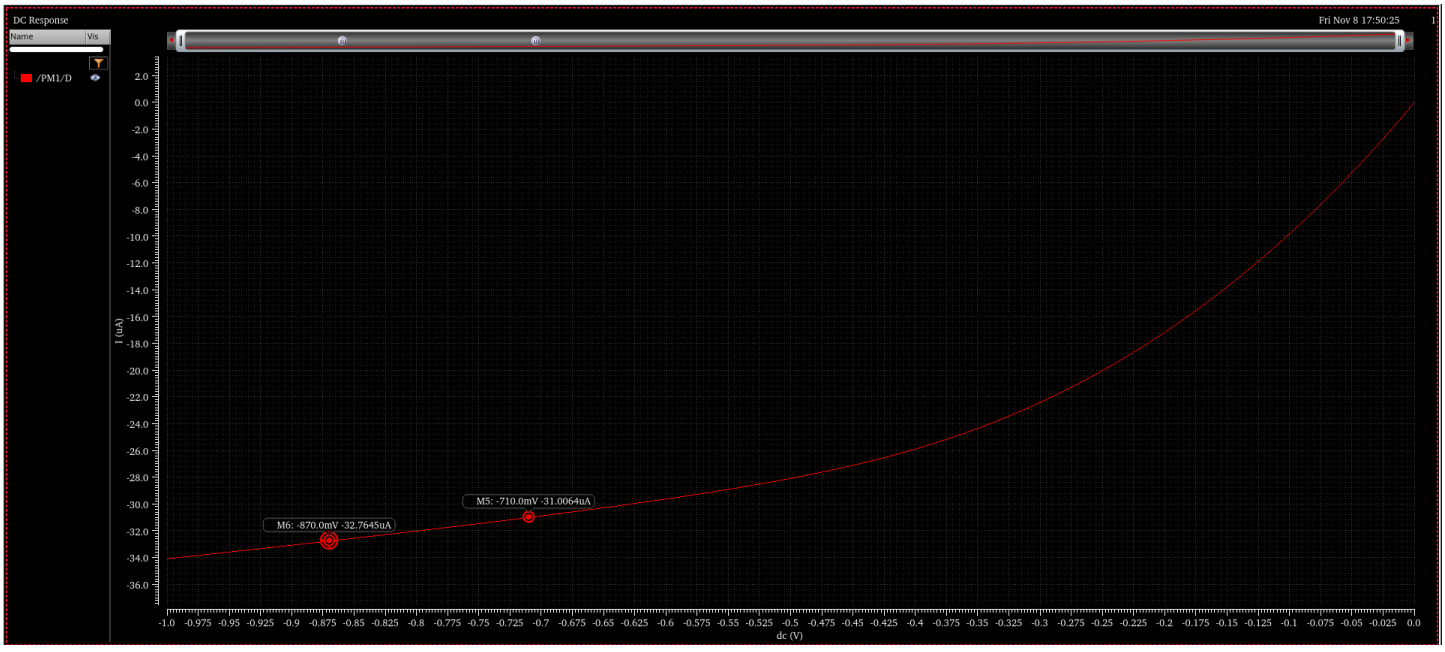
Output characterizes.

Circuit Diagrams:

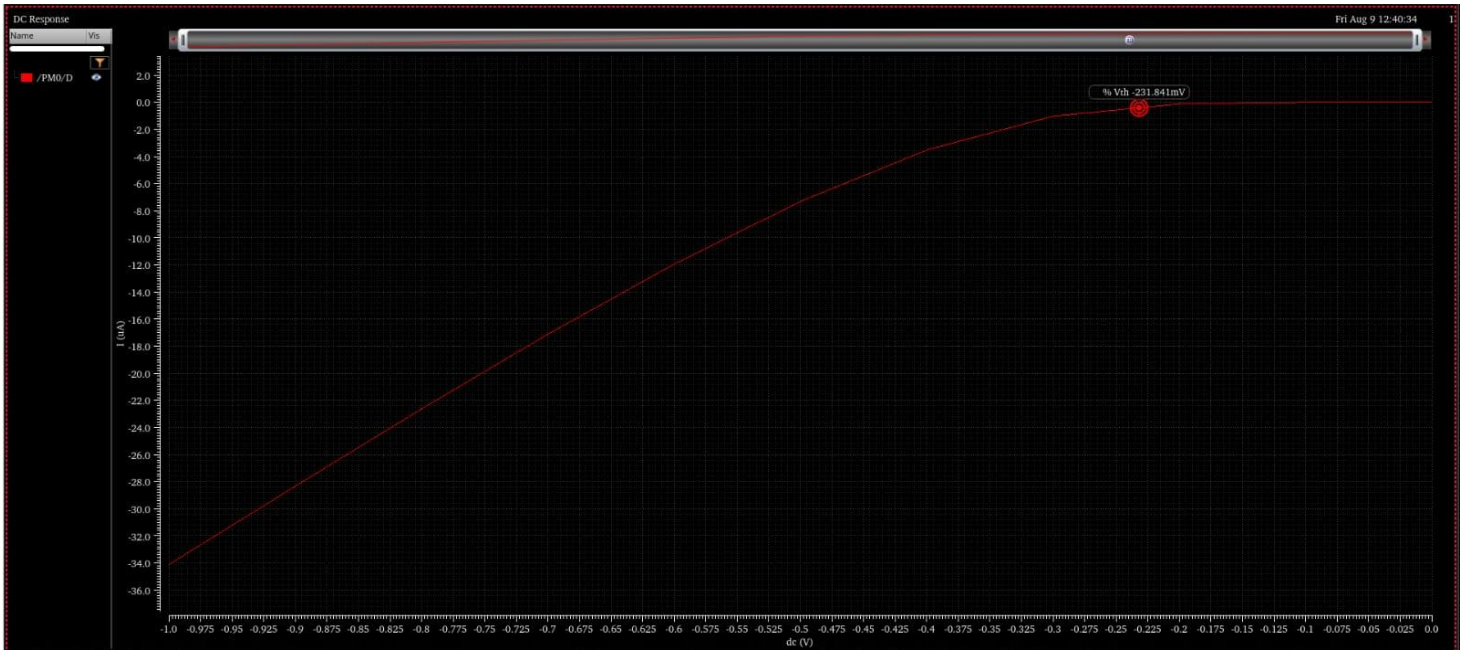


GRAPHS:

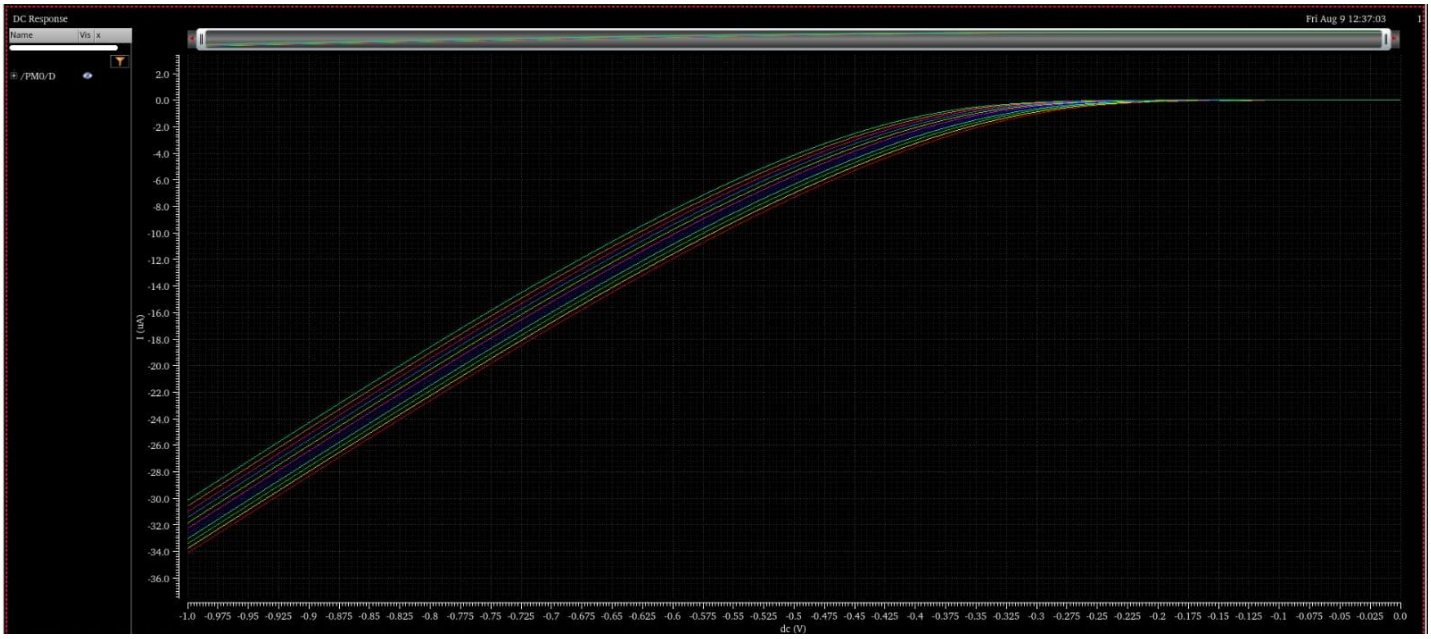
a) Id vs Vds:



2)Id vs Vgs:

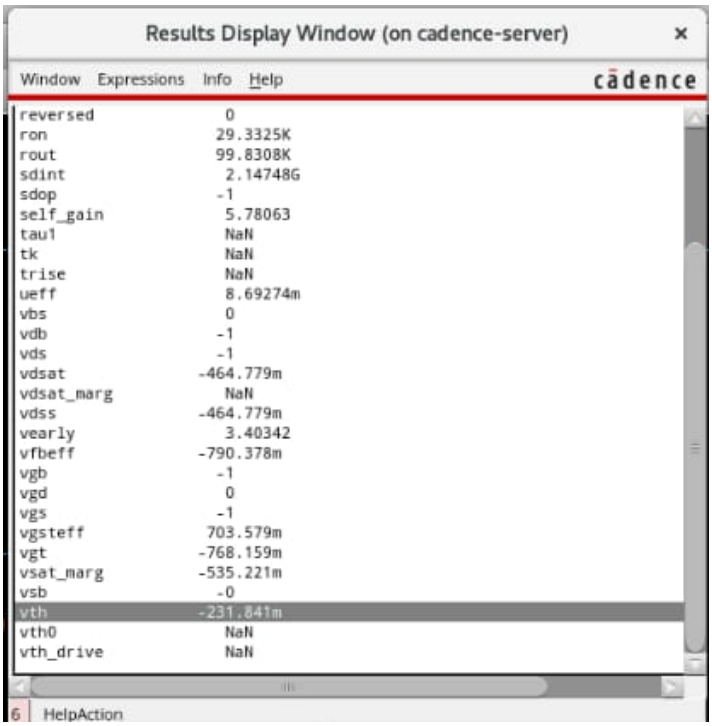


3)Body Bias Effect:

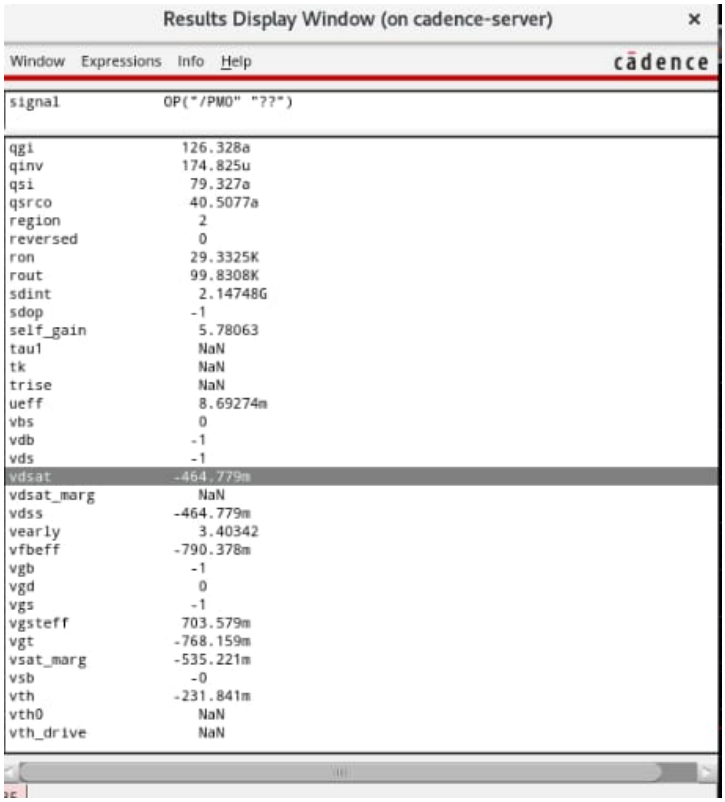


OBSERVATIONS:

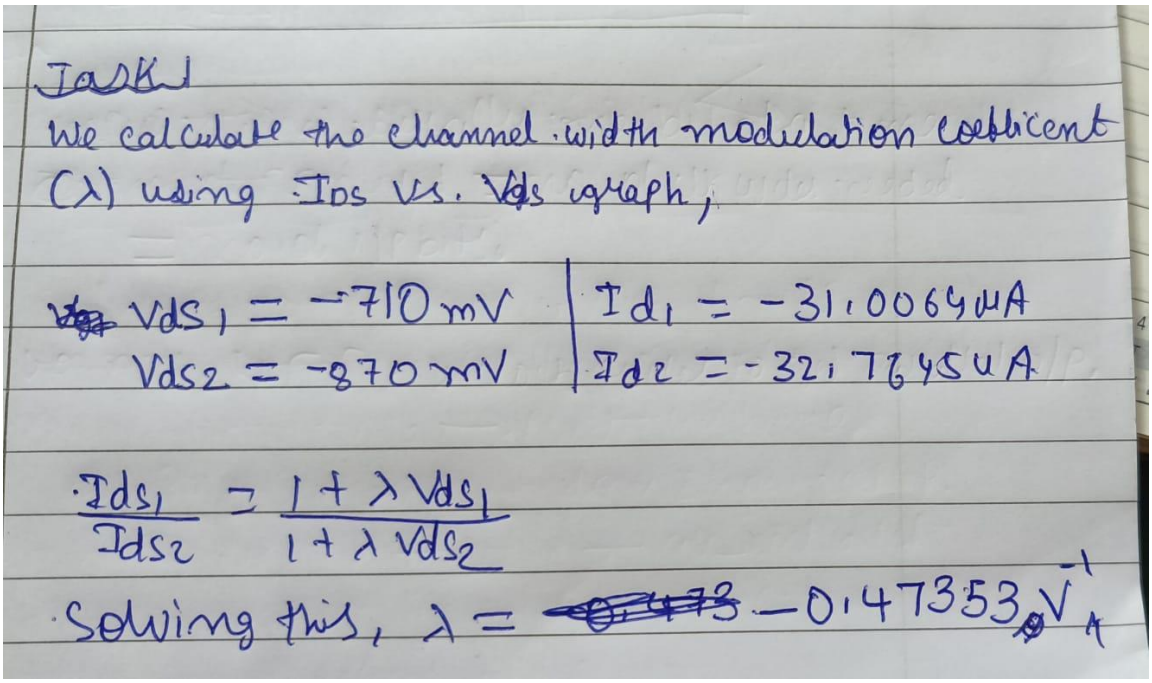
1)Vth :



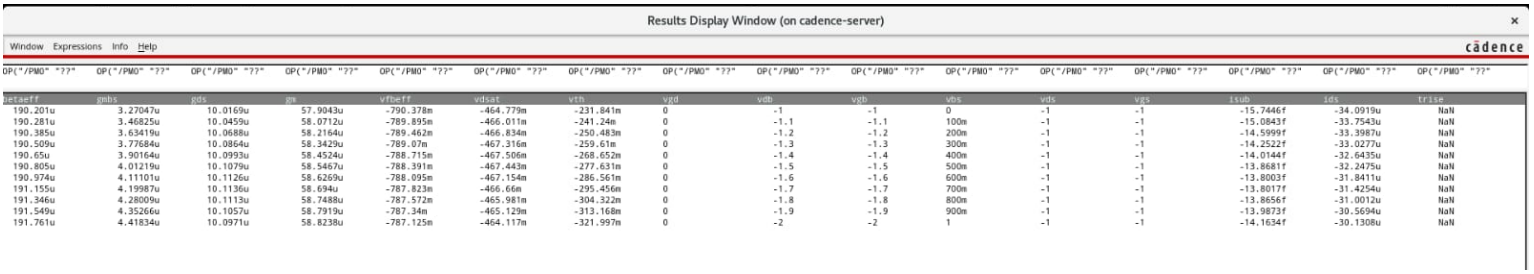
2)Vdsat :



4) Channel Length Modulation Coefficient (λ):



3)Overall Results:



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betaeff	gmbs	gds	gm	vtheff	vdsat	vth	vtd	vdb	vyb	vbs	vds	vgs	isub	ids	trise
190.201u	3.27047u	10.0169u	57.9043u	-790.378m	-464.779m	-231.841m	0	-1	-1	0	-1	-1	-15.7446f	-34.0919u	NaN
190.281u	3.46825u	10.0459u	58.0712u	-789.895m	-466.011m	-241.24m	0	-1.1	-1.1	100m	-1	-1	-15.0843f	-33.7543u	NaN
190.385u	3.63419u	10.0688u	58.2164u	-789.462m	-466.834m	-250.483m	0	-1.2	-1.2	200m	-1	-1	-14.5999f	-33.3987u	NaN
190.509u	3.77684u	10.0864u	58.3429u	-789.07m	-467.316m	-259.61m	0	-1.3	-1.3	300m	-1	-1	-14.2522f	-33.0277u	NaN
190.65u	3.90164u	10.0993u	58.4524u	-788.715m	-467.506m	-268.652m	0	-1.4	-1.4	400m	-1	-1	-14.0144f	-32.6435u	NaN
190.805u	4.01219u	10.1079u	58.5467u	-788.391m	-467.443m	-277.631m	0	-1.5	-1.5	500m	-1	-1	-13.8681f	-32.2475u	NaN
190.974u	4.11101u	10.1126u	58.6269u	-788.095m	-467.154m	-286.561m	0	-1.6	-1.6	600m	-1	-1	-13.8003f	-31.8411u	NaN
191.155u	4.19987u	10.1136u	58.694u	-787.823m	-466.66m	-295.456m	0	-1.7	-1.7	700m	-1	-1	-13.8017f	-31.4254u	NaN
191.346u	4.28009u	10.1113u	58.7488u	-787.572m	-465.981m	-304.322m	0	-1.8	-1.8	800m	-1	-1	-13.8656f	-31.0012u	NaN
191.549u	4.35266u	10.1057u	58.7919u	-787.34m	-465.129m	-313.168m	0	-1.9	-1.9	900m	-1	-1	-13.9873f	-30.5694u	NaN
191.761u	4.41834u	10.0971u	58.8238u	-787.125m	-464.117m	-321.997m	0	-2	-2	1	-1	-1	-14.1634f	-30.1308u	NaN

Calculations:

1. Channel Length Modulation Coefficient (λ) for PMOS=-0.47353

Result and Inference:

In this experiment using Cadence Virtuoso, the PMOS transistor was tested to observe the relationship between its drain current (Id) and drain-to-source voltage (Vds) across different gate-to-source voltages (Vgs). The setup involved applying varying Vds values while keeping Vgs constant for each sweep. Transient analysis produced output plots showing Id versus Vds, revealing characteristic PMOS behavior: as Vds increases, Id initially rises and then saturates, with higher Vgs values (more negative) leading to increased current due to stronger inversion. This experiment confirmed the expected PMOS operation, highlighting its current control based on Vgs and illustrating key principles of PMOS behavior essential for analog and digital circuit design.