AIM: To design a Serial-In Parallel-Out(SIPO) Shift Register

Software used: Cadence Virtuoso

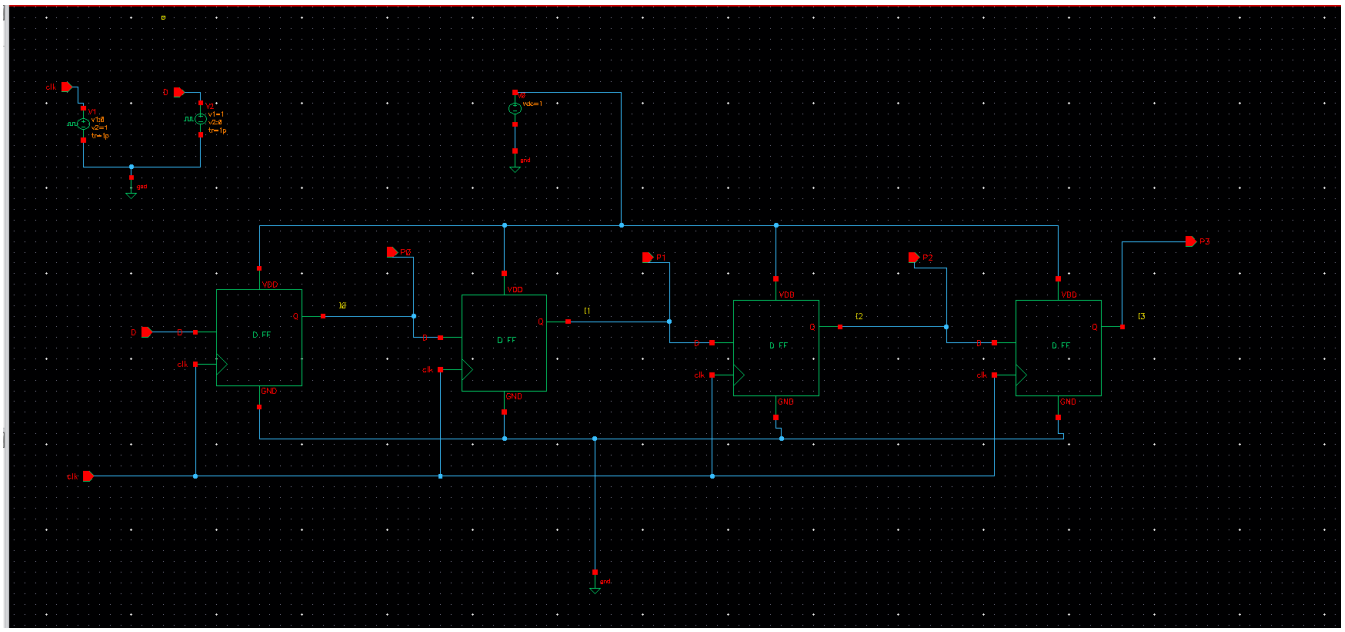
Experimental Procedure:

1. Invoke Cadence Virtuoso tool

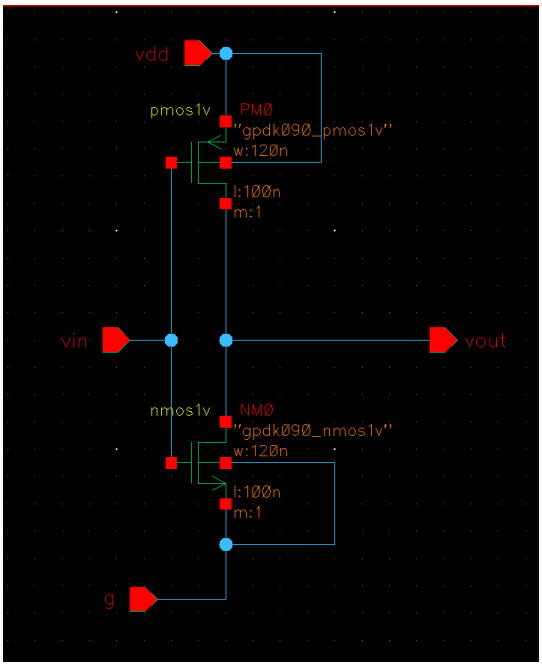
2. Construct the schematic as per given Circuit Diagrams

3. Invoke ADEL tool for simulations. Perform Transient Analysis for analyzing its working.

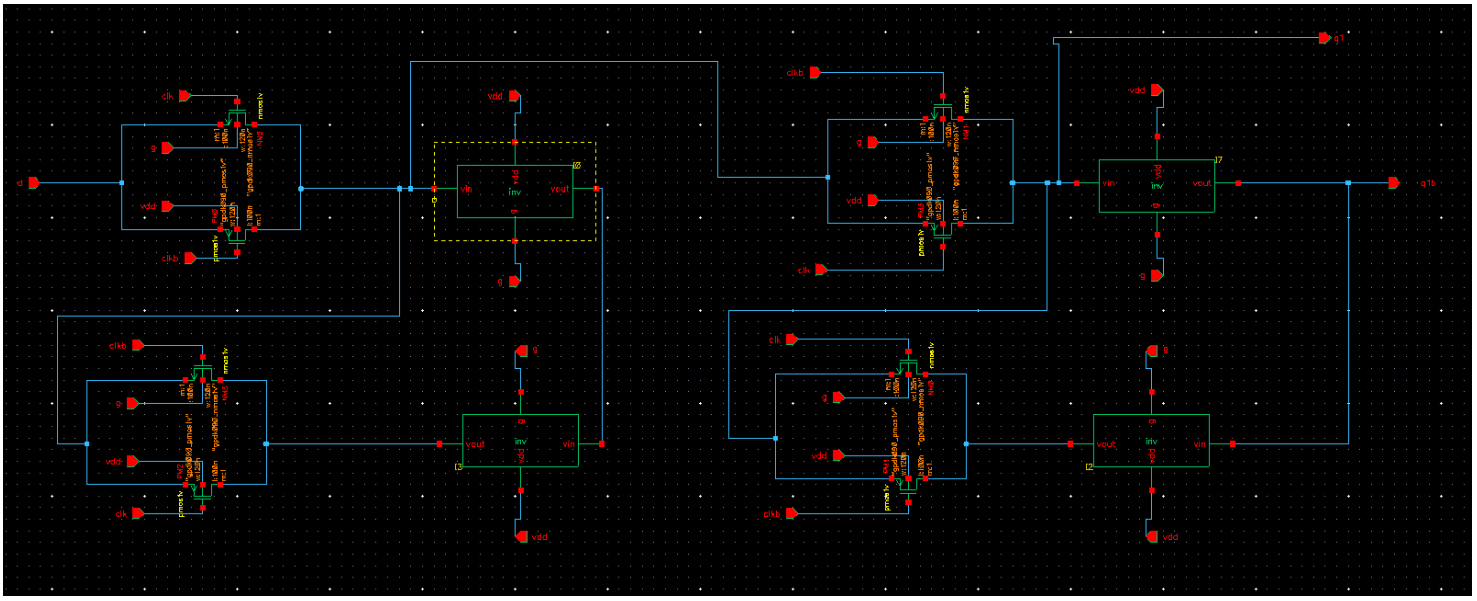
Circuit Diagrams:



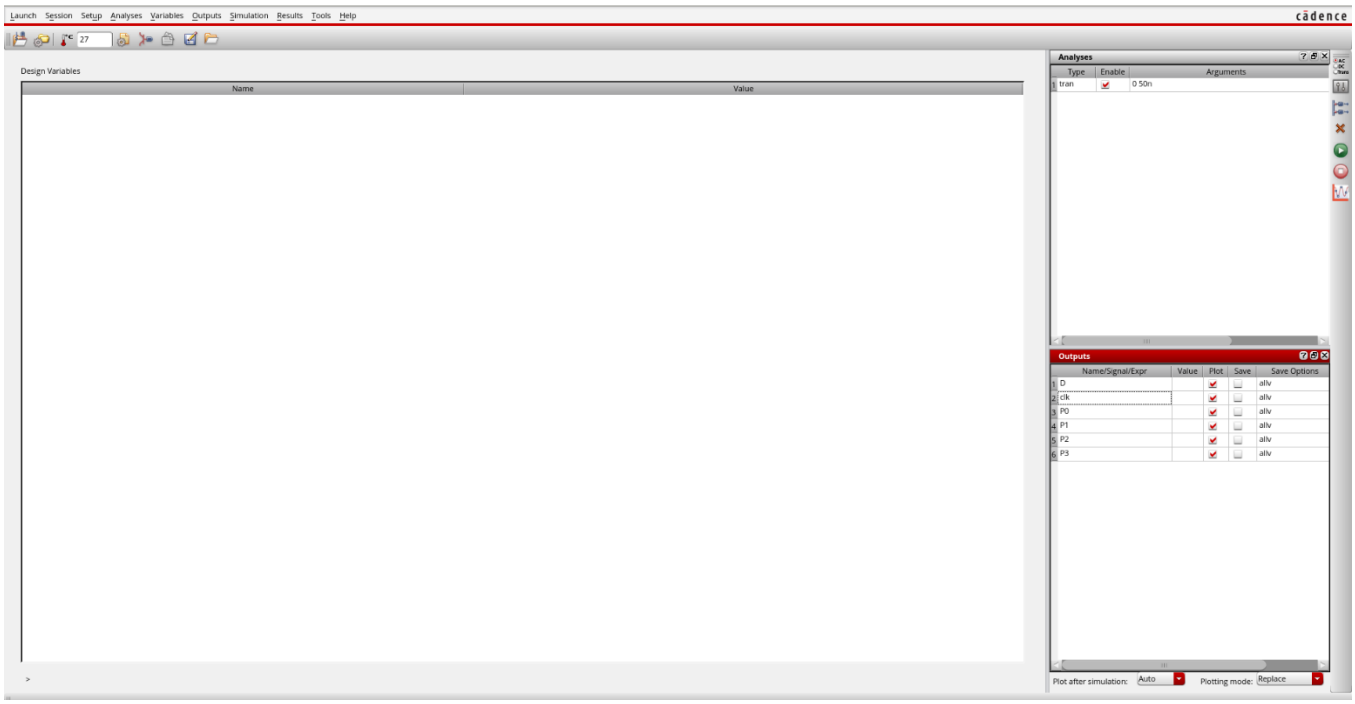
Experiment:



Inverter Schematic

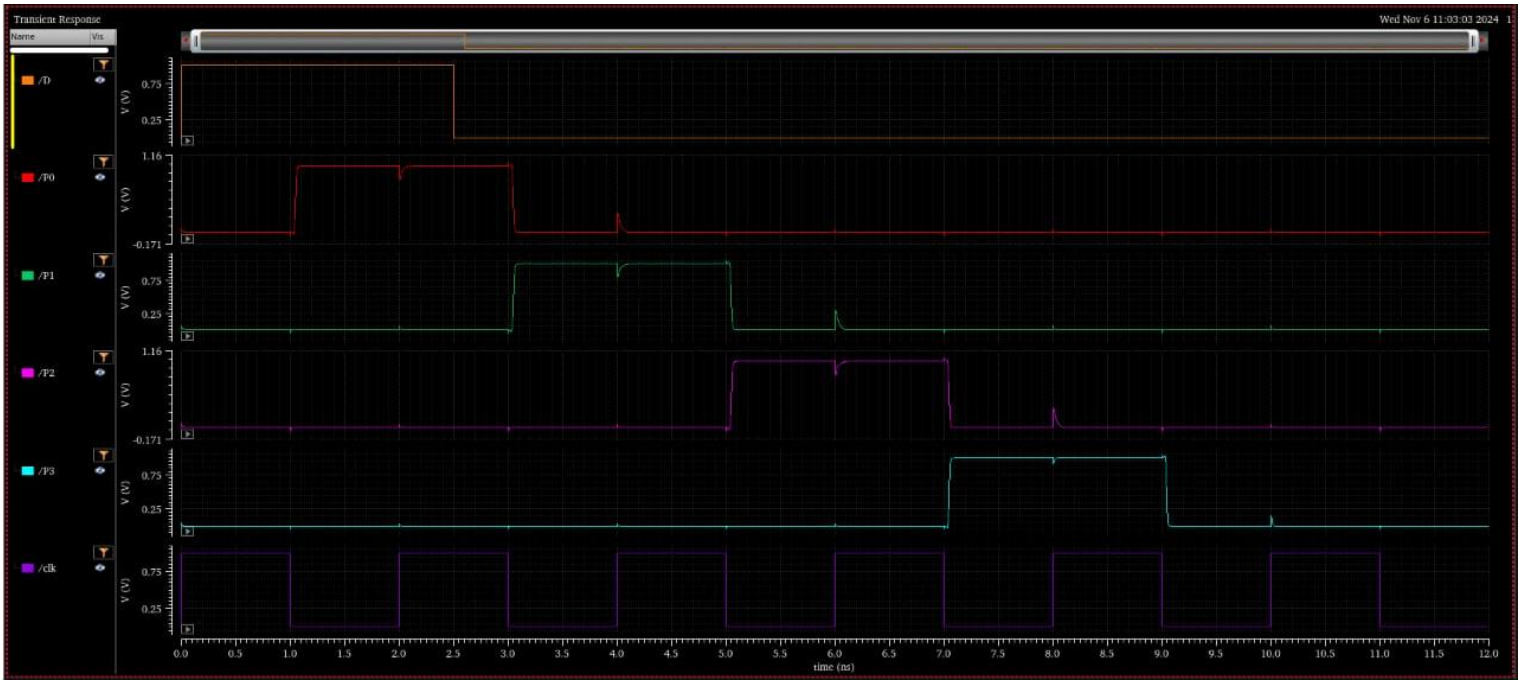


D Flip Flop Schematic



ADEL Window

GRAPH:



Result and Inference:

In a SIPO (Serial-In Parallel-Out) experiment simulated using Cadence Virtuoso, a SIPO shift register was tested to convert serial input data into parallel output. The setup included a clock signal, serial data input, and CMOS-based flip-flops. During transient analysis, output waveforms were observed for serial input, clock, and parallel output signals. The results showed that with each clock pulse, data bits shifted correctly to parallel outputs, confirming data integrity and synchronization with the clock. This validated the SIPO design's ability to accurately convert serial data to parallel form, a critical function for applications in data buffering and serial-to-parallel data conversion.