AIM: To design a 4:1 Mux using CMOS Logic and Transmission Gate Logic

Software used: Cadence Virtuoso

Experimental Procedure:

1. Invoke Cadence Virtuoso tool

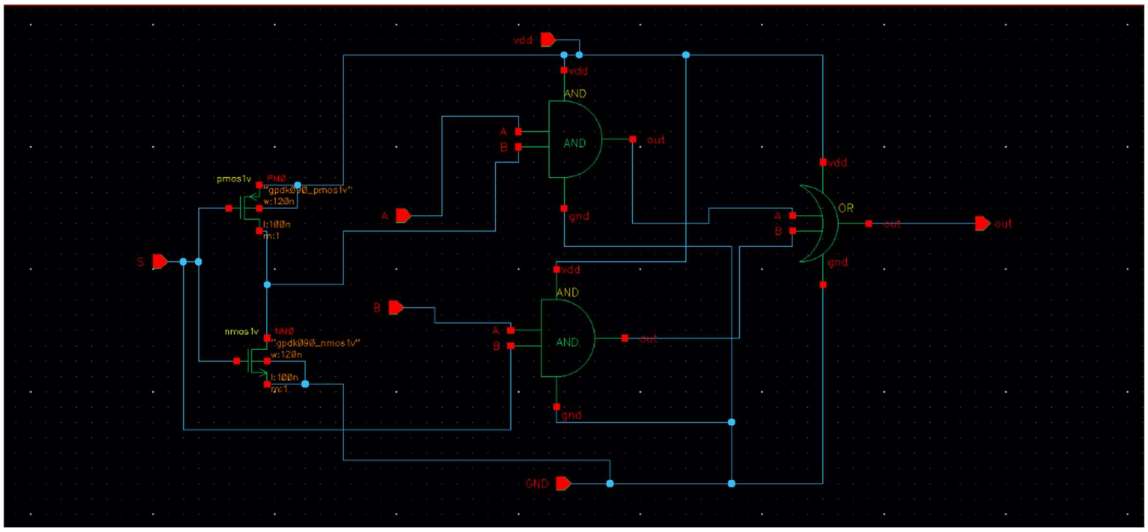
2. Construct a 2:1 Mux and then use it to construct a 4:1 Mux as per following Circuit Diagrams in CMOS Logic.

3.Construct a 4:1 Mux using Transmission Gate Logic as per following Circuit Diagrams.

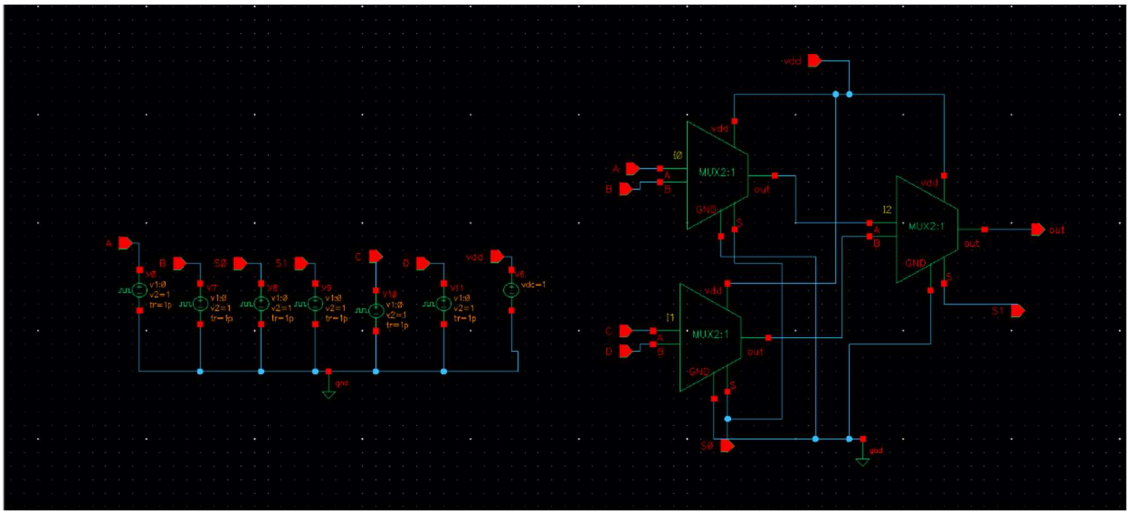
3. Invoke ADEL tool for simulations. Perform Transient Analysis for analyzing its working.

Circuit Diagrams:

1)CMOS:

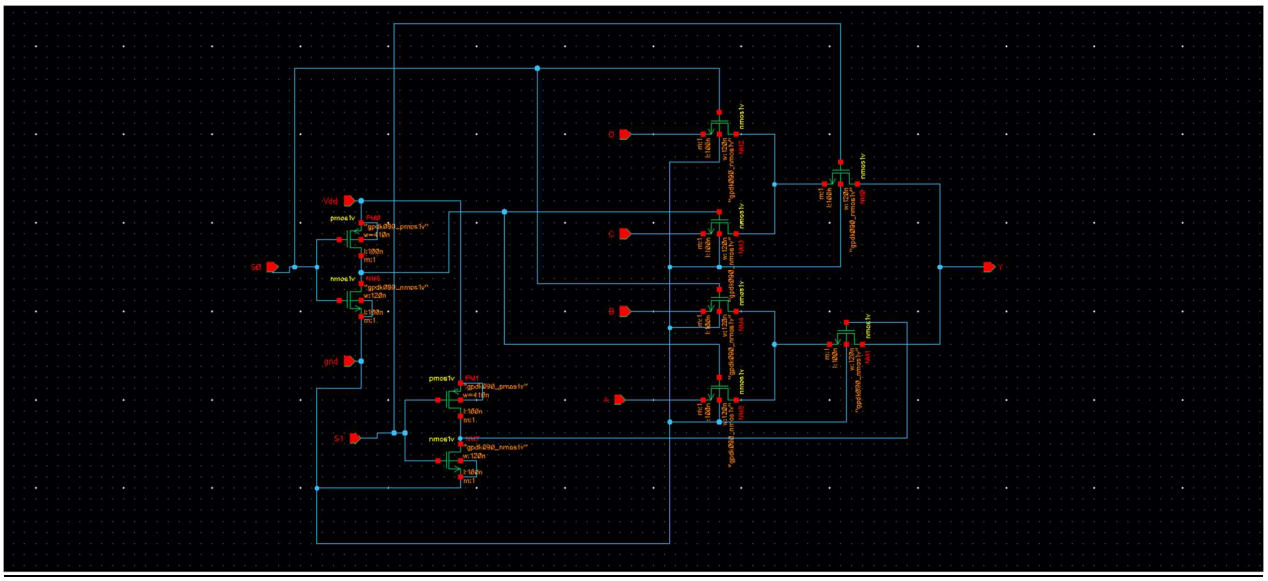


Mux 2:1

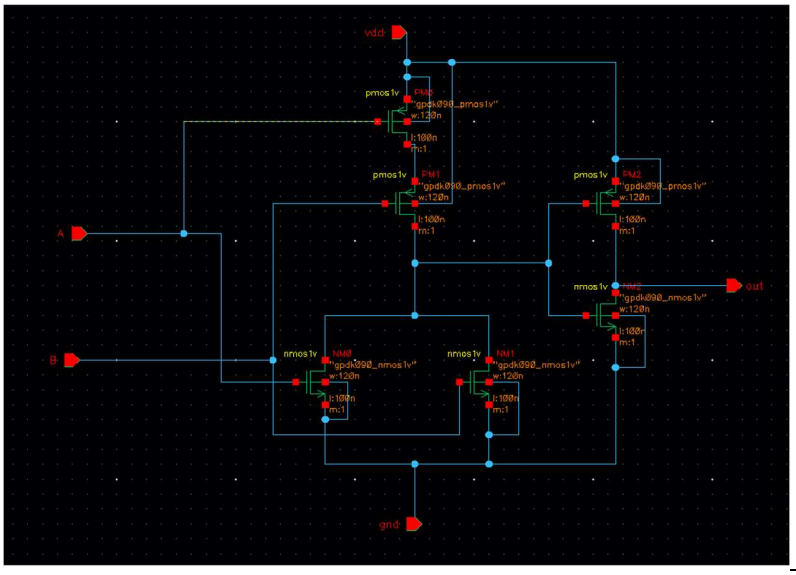


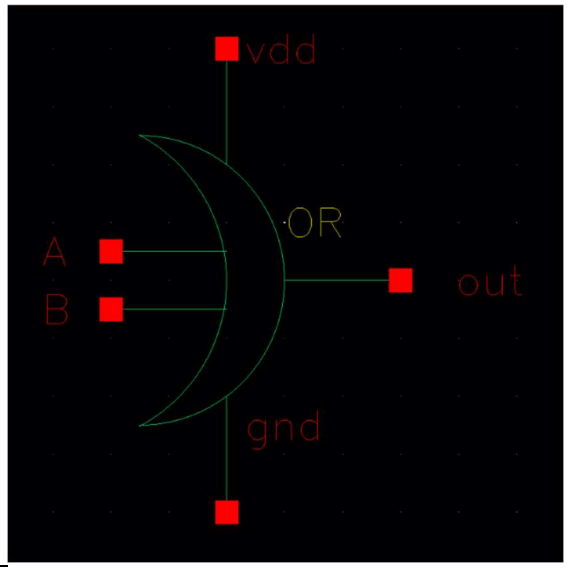
Mux 4:1

2)Transmission-Gate Logic:

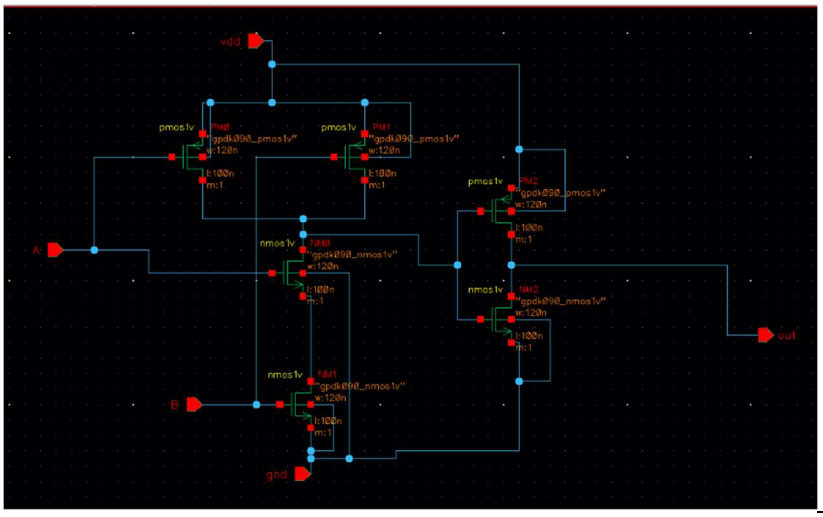


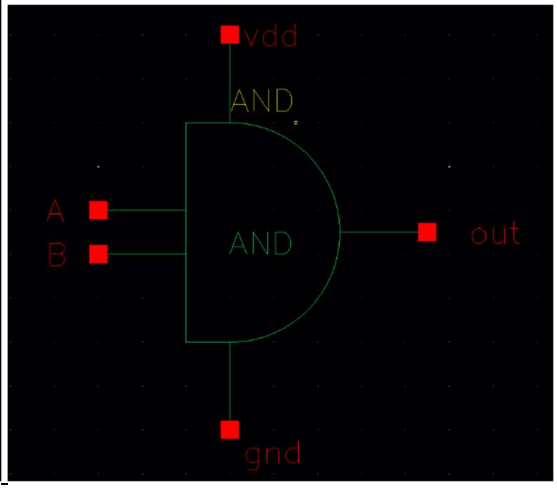
CMOS Experiment:



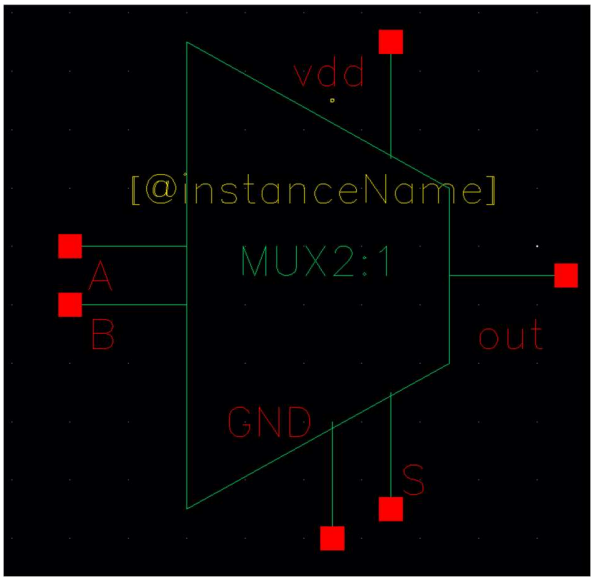


OR GATE





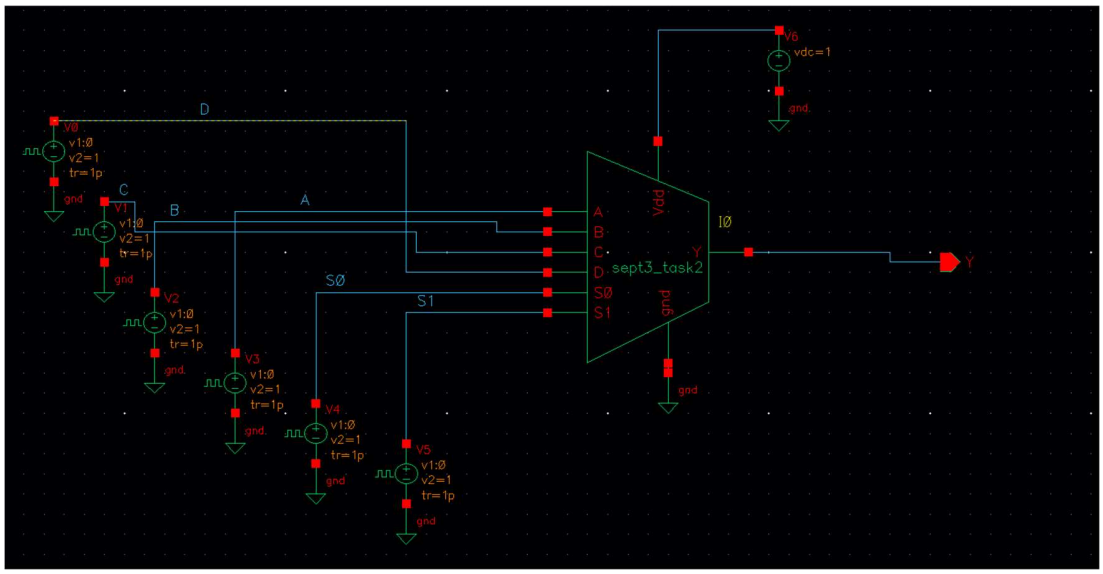
AND GATE



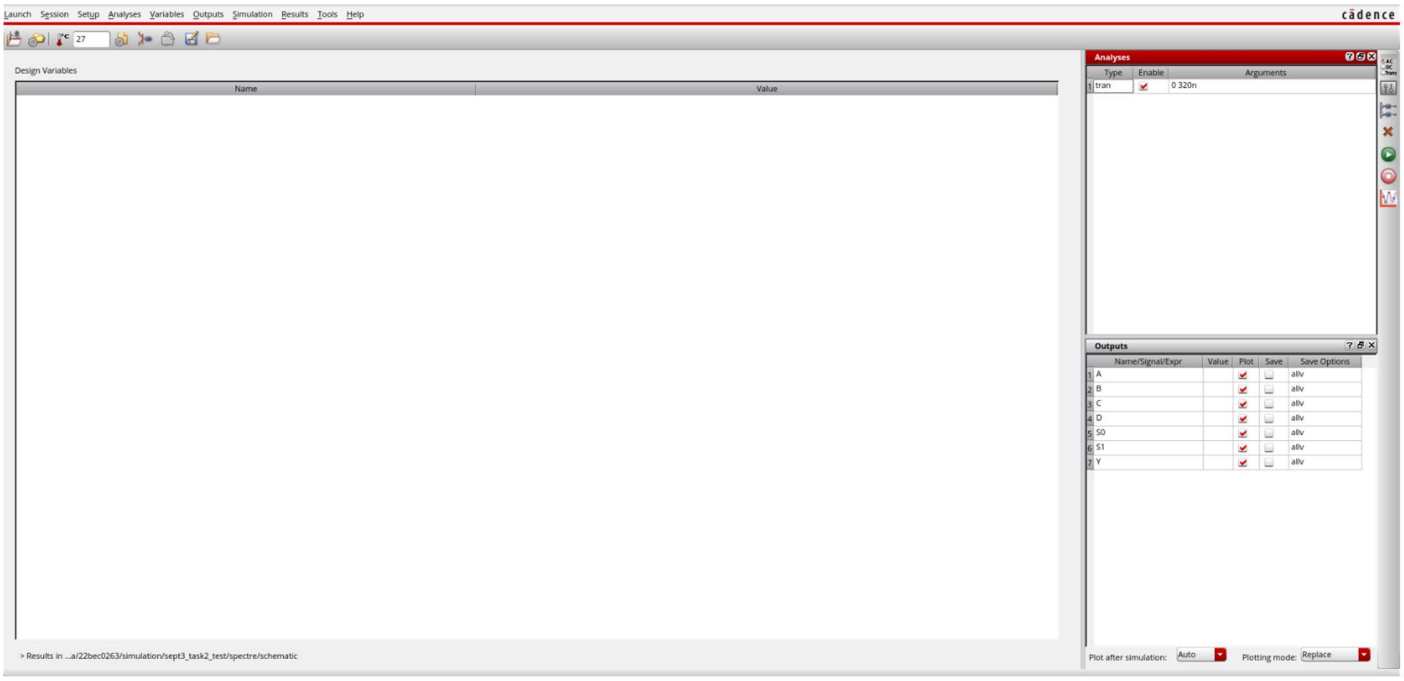
MUX 2:1 SYMBOL

ADEL Window

Transmission-Gate Logic Experiment:



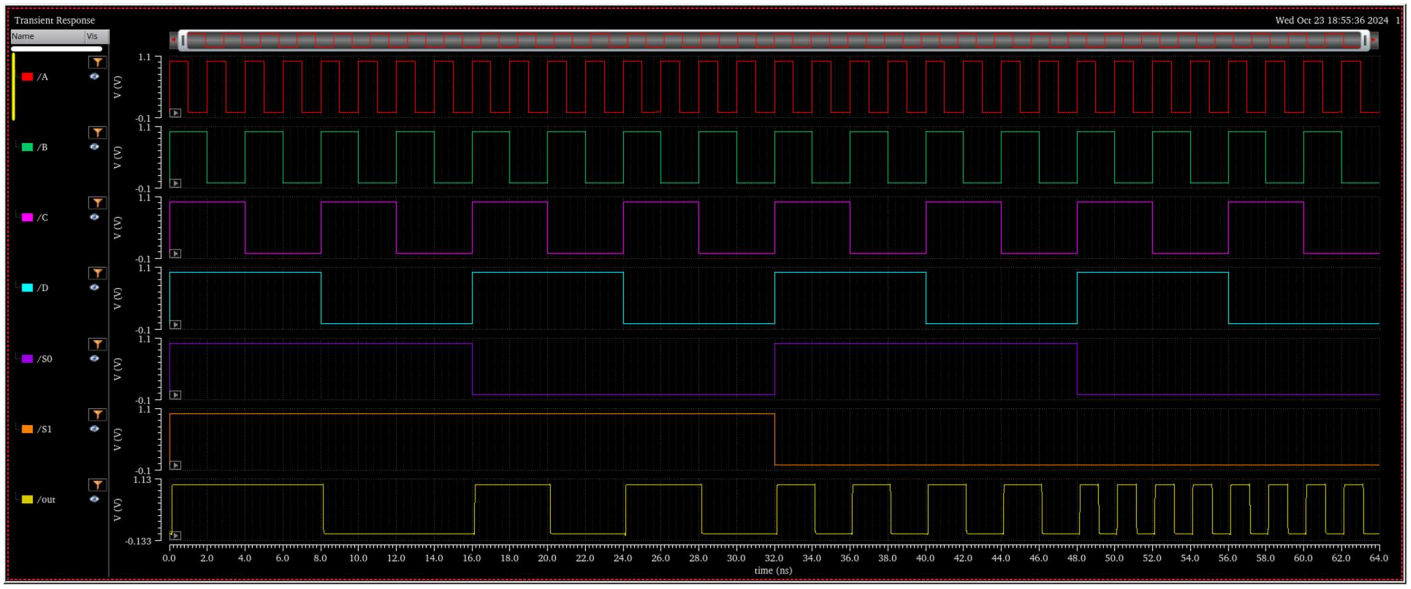
Mux 4:1 Symbol



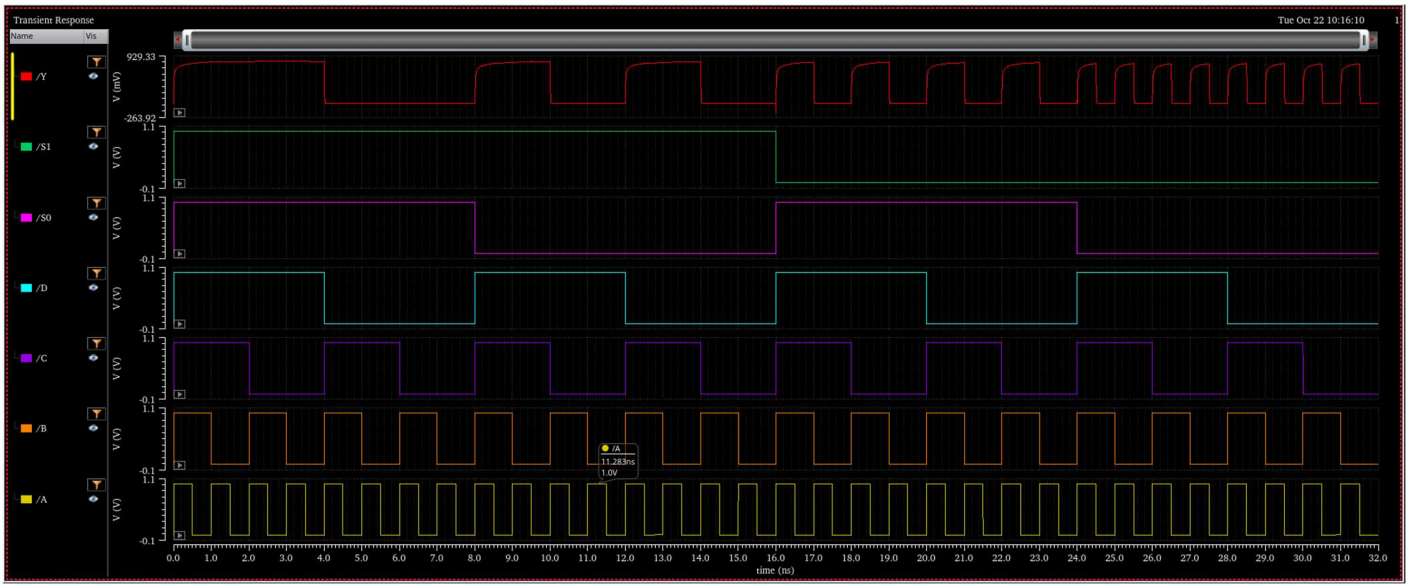
ADEL Window

GRAPHS:

1)CMOS Logic:



2)Transmission Gate Logic:



Result and Inference:

In designing a 4:1 multiplexer using a 2:1 multiplexer in Cadence Virtuoso with CMOS and transmission gate logic, two 2:1 multiplexers are cascaded to form a 4:1 structure, selecting one of four inputs based on two select lines . Each 2:1 MUX is built with CMOS and transmission gate configurations, ensuring low-resistance paths for selected inputs and high resistance for unselected paths, thus providing strong logic levels. Transient analysis was conducted to observe the output response based on select line combinations. The simulation results confirmed that the 4:1 MUX reliably passed the correct input to the output, showing proper functionality and effective switching control, validating the cascaded 2:1 design and the approaches for efficient and accurate multiplexing.We also practised the various Design Techniques and Rules associated with CMOS Logic and Transmission Gate Logic. We also simulated the Designs and analysed the Device Working using Different Inputs and analysed the Outputs.