AIM: To create a layout of a 2 input CMOS NOR Gate and perform the post layout simulations.

Software used: Cadence Virtuoso

Experimental Procedure:

1. Invoke Cadence Virtuoso tool

2. Construct the NOR schematic as shown in Fig.

3. Perform transient analysis and calculate the propagation delay.

4. Invoke the cadence virtuoso layout editor.

5. Draw the layout of the inverter circuit shown in fig.

6. Run DRC to make sure you are not violating any process design rules.

7. Run LVS to check whether the layout and schematic matches.

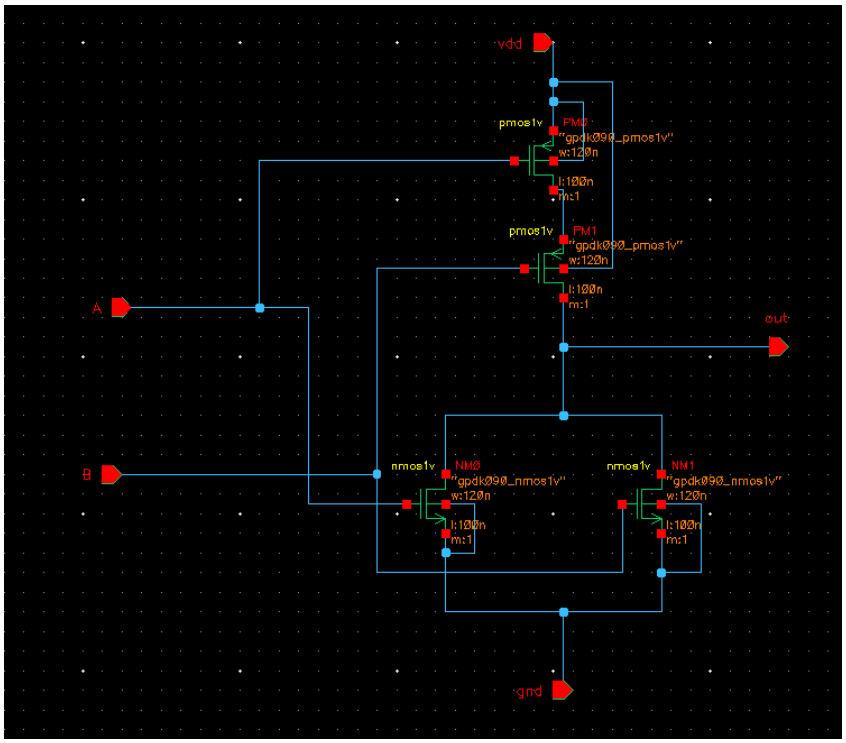
8. Extract the design (RC extraction) that generates a net list based layout which

includes parasitic capacitances and resistances.

9. Perform the post layout simulations using Spectre.

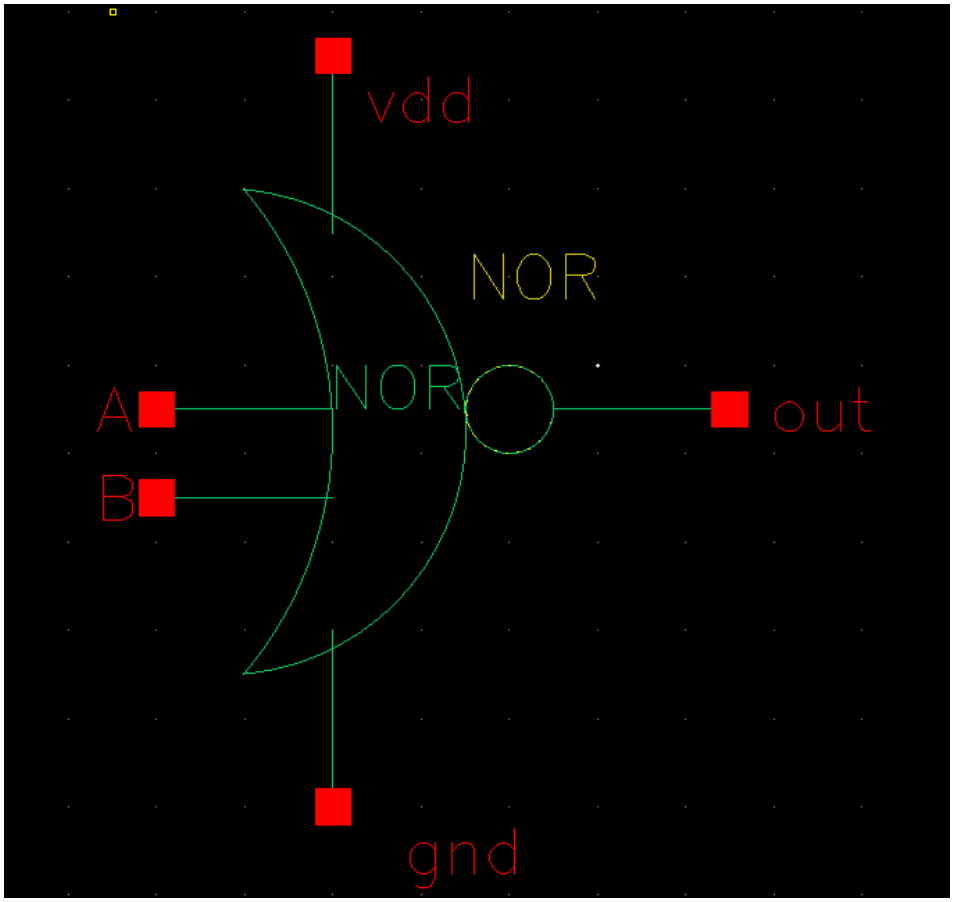
10. Observe the prop agation delays for both schematic and extracted net list of the layout.

Circuit Diagrams:

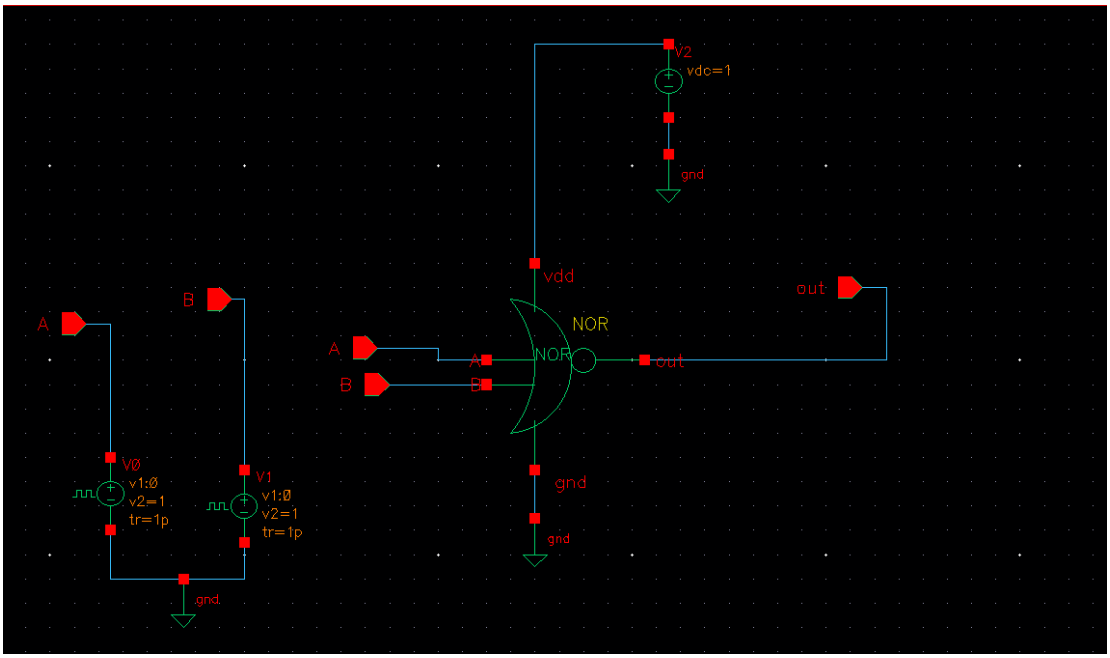


Experiment:

1)NOR Gate:

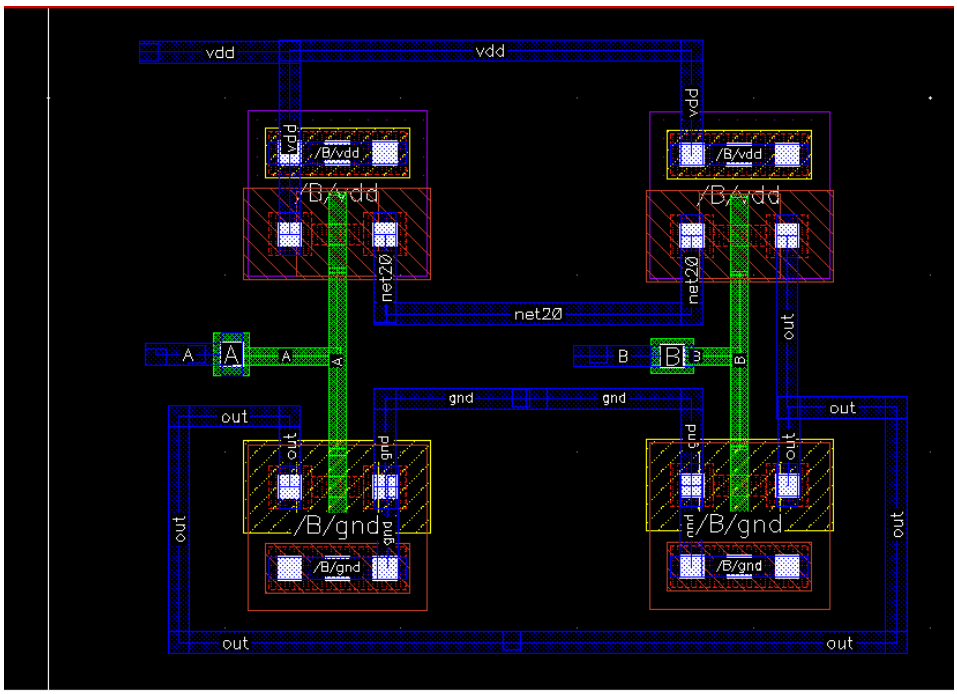


NOR Gate Symbol



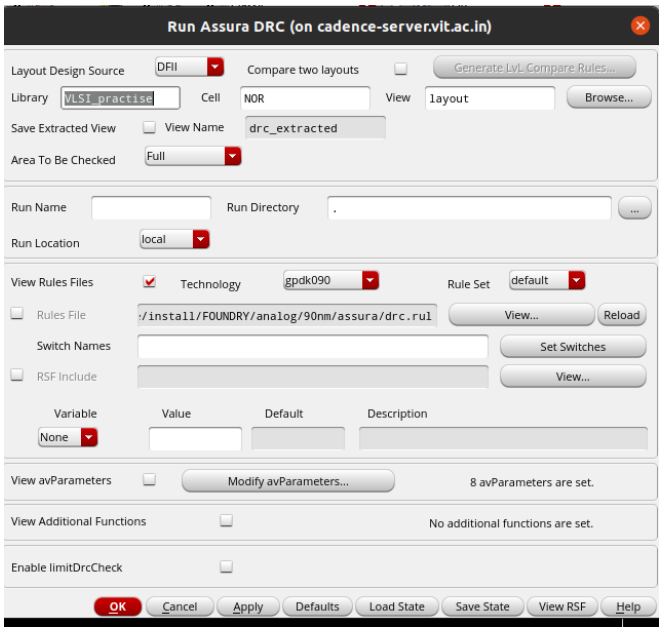
NOR Gate Implementation

2)Physical Design/Layout:

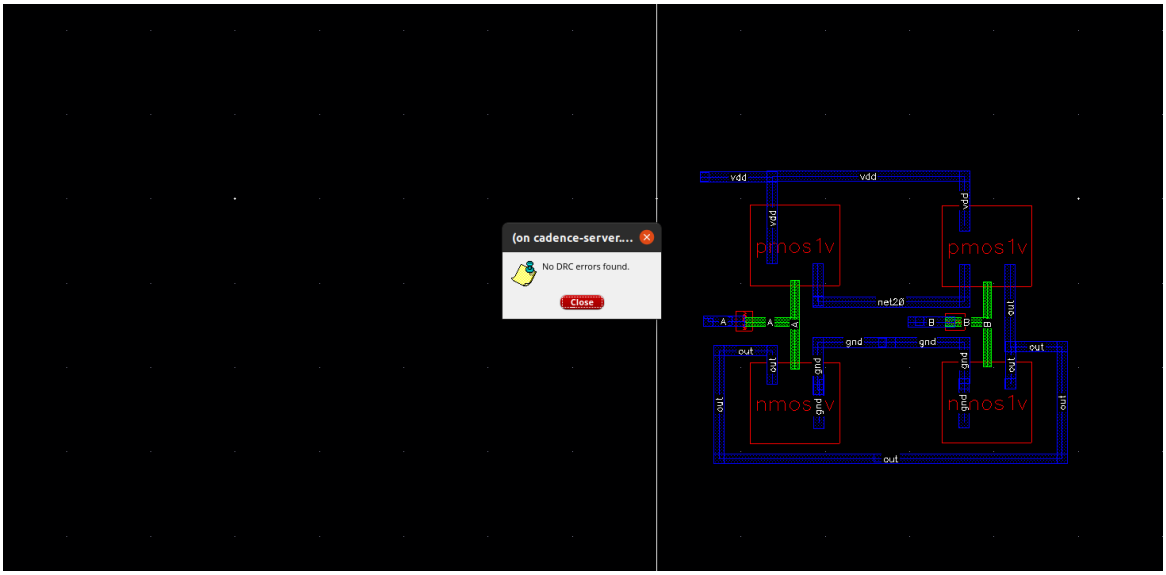


Layout of NOR Gate

2)Design Rule Check :

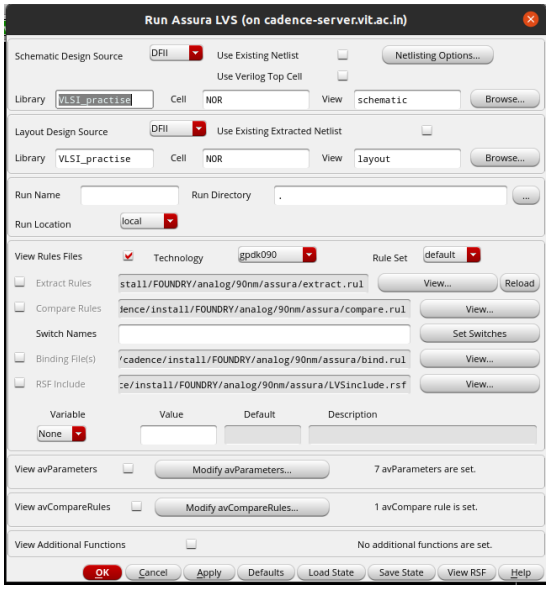


DRC Window

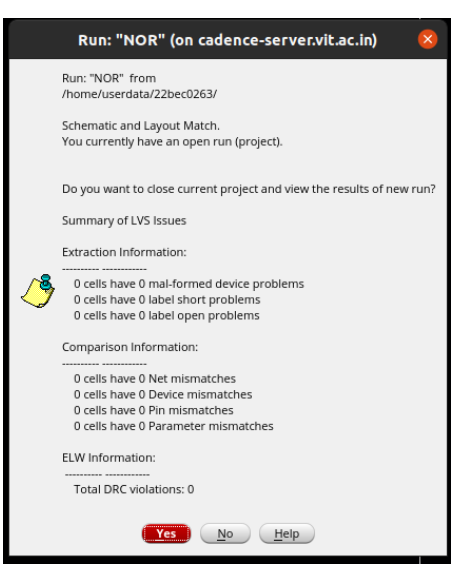


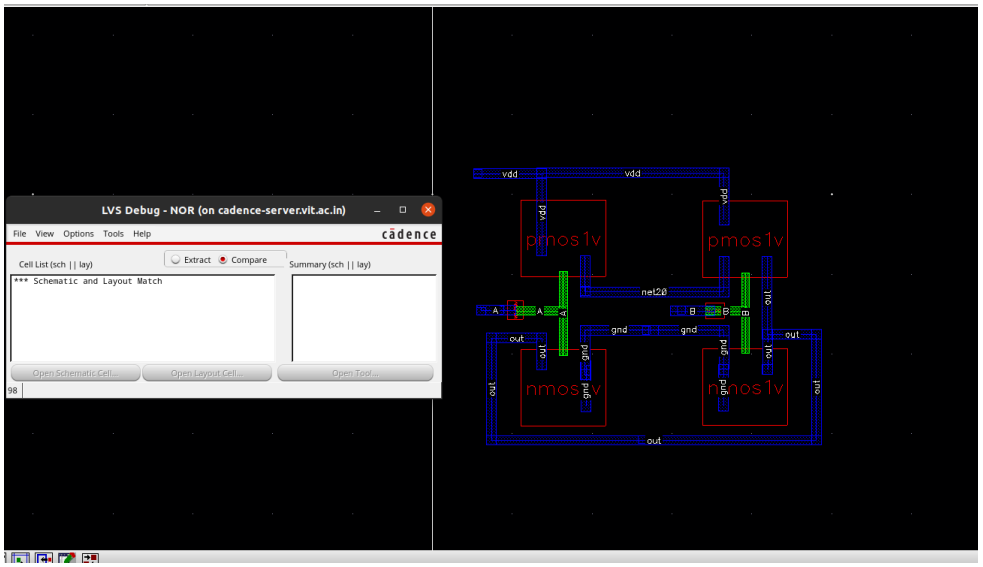
DRC Result Window

2)Layout vs Schematic :



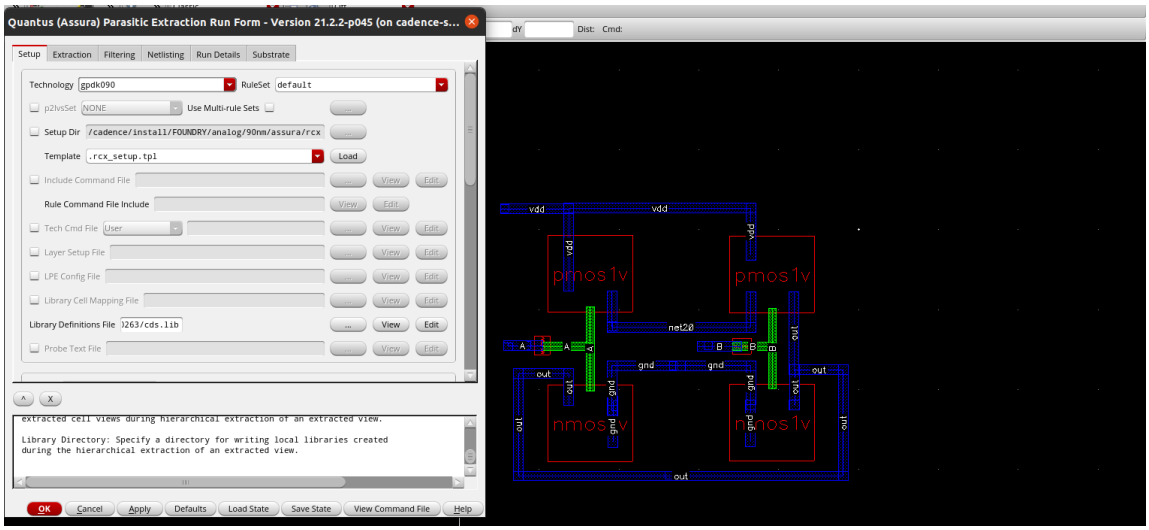
LVS Window



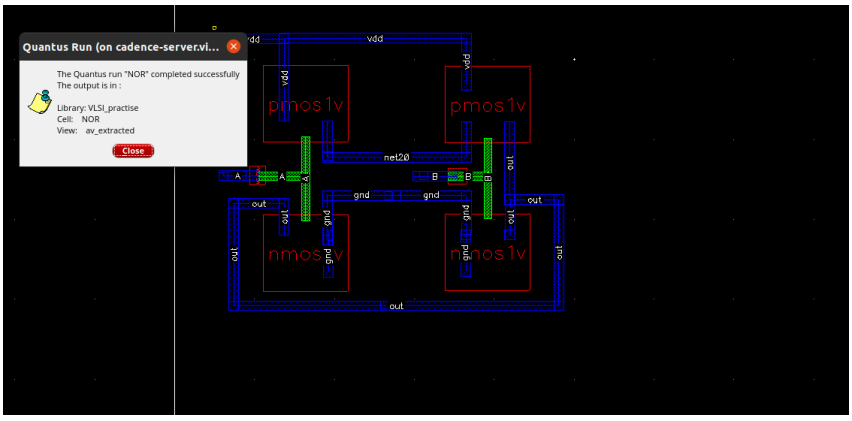


LVS Result Window **LVS Message**

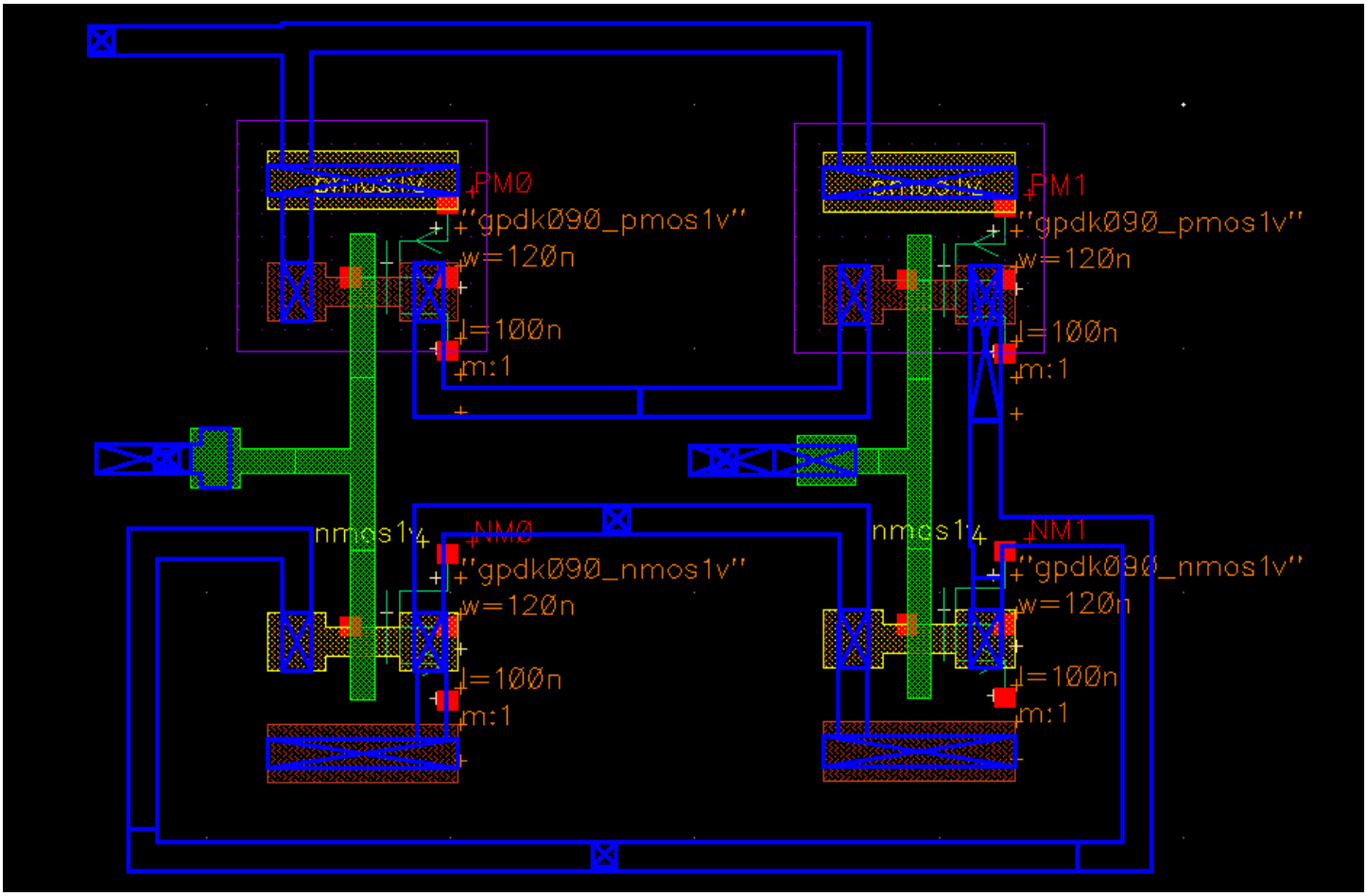
3)RC Extraction :



Run Quartus Window

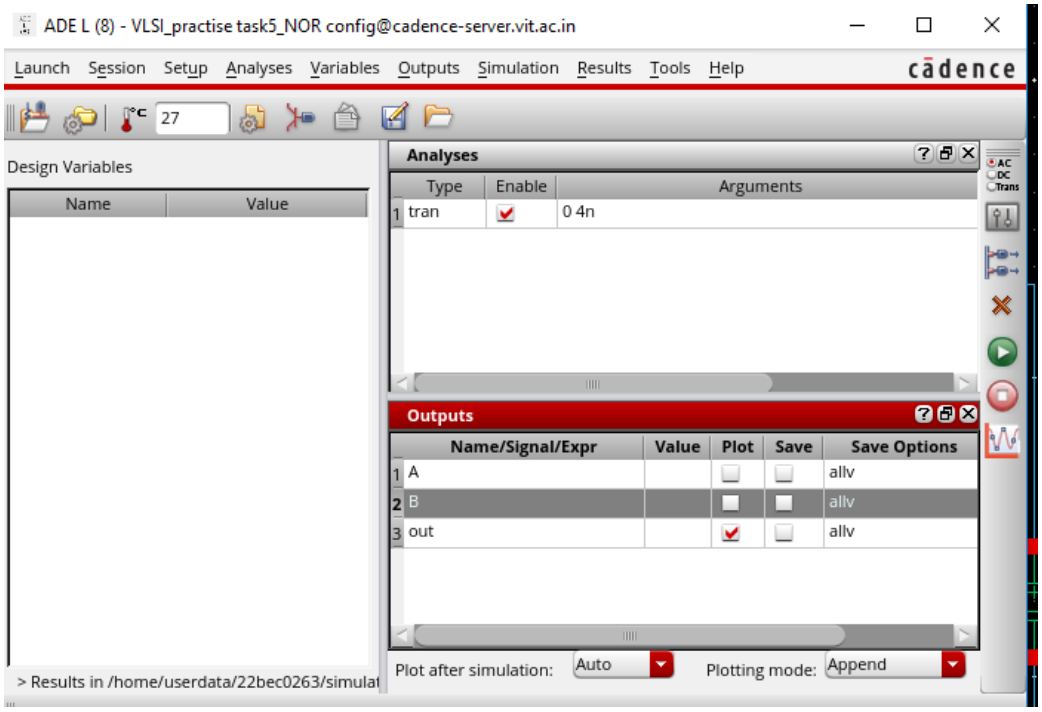


RC Extraction Success Popup

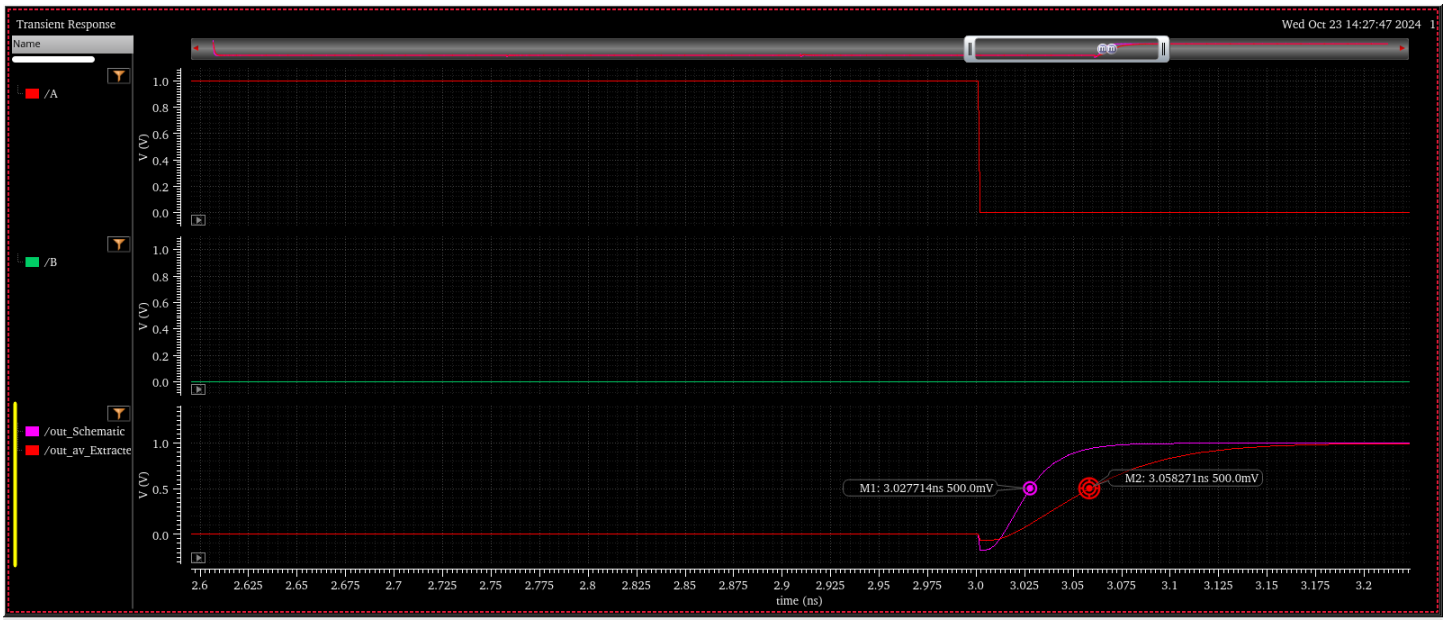


RC Extracted View

GRAPH:



ADEL Window



Layout Vs Schematic Waveform

Calculation:

Propagation Delay between Layout and Schematic= 30.556ps

Result and Inference:

The physical design and post-layout simulation of the NOR gate using Cadence Virtuoso demonstrated successful implementation of the circuit's functionality. The layout adhered to design rules and ensured correct transistor sizing and placement. Post-layout simulations verified the gate's timing characteristics, including propagation delays and rise/fall times, which were found to be within acceptable limits. The simulated output waveforms accurately matched the expected NOR gate behavior for various input combinations, confirming the design's correctness. Overall, the results indicate a well-designed and robust NOR gate implementation, ready for further integration into larger circuits.