

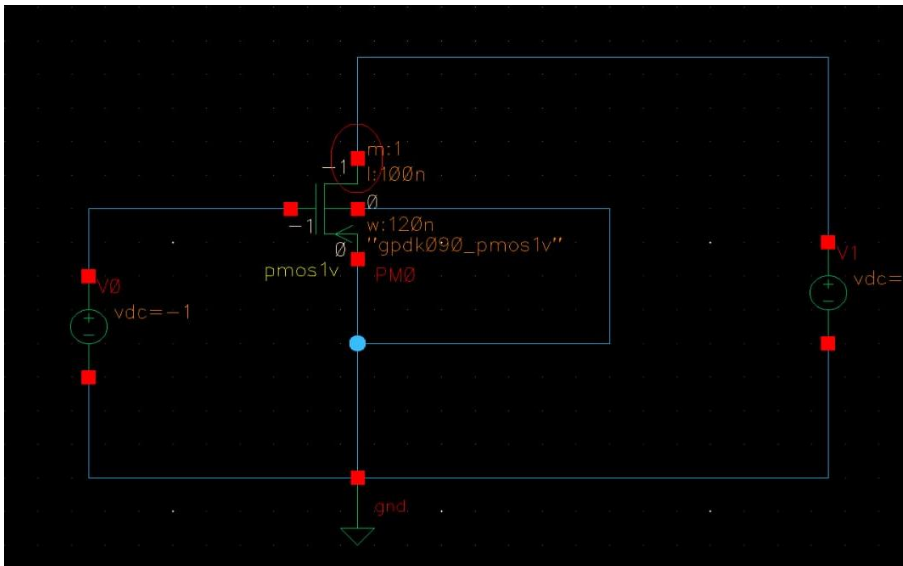
**AIM:** To plot V-I characteristics and calculate the Threshold and pinch off voltages of P-MOSFET.

**Software used:** Cadence Virtuoso

**Experimental Procedure:**

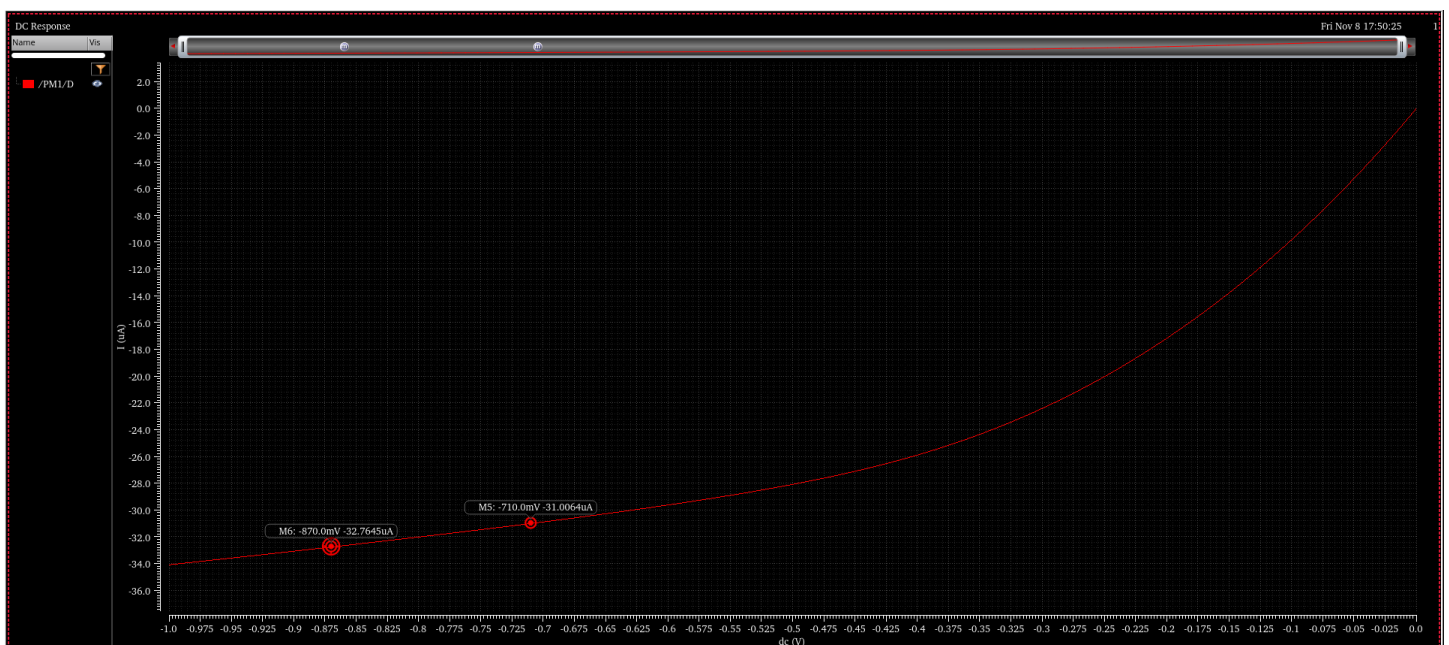
1. Invoke Cadence Virtuoso tool
2. Construct the schematic of P-MOSFET as Shown
3. Invoke ADEL tool for simulations. Perform DC analysis in order to plot transfer and Output characterizes.

**Circuit Diagrams:**

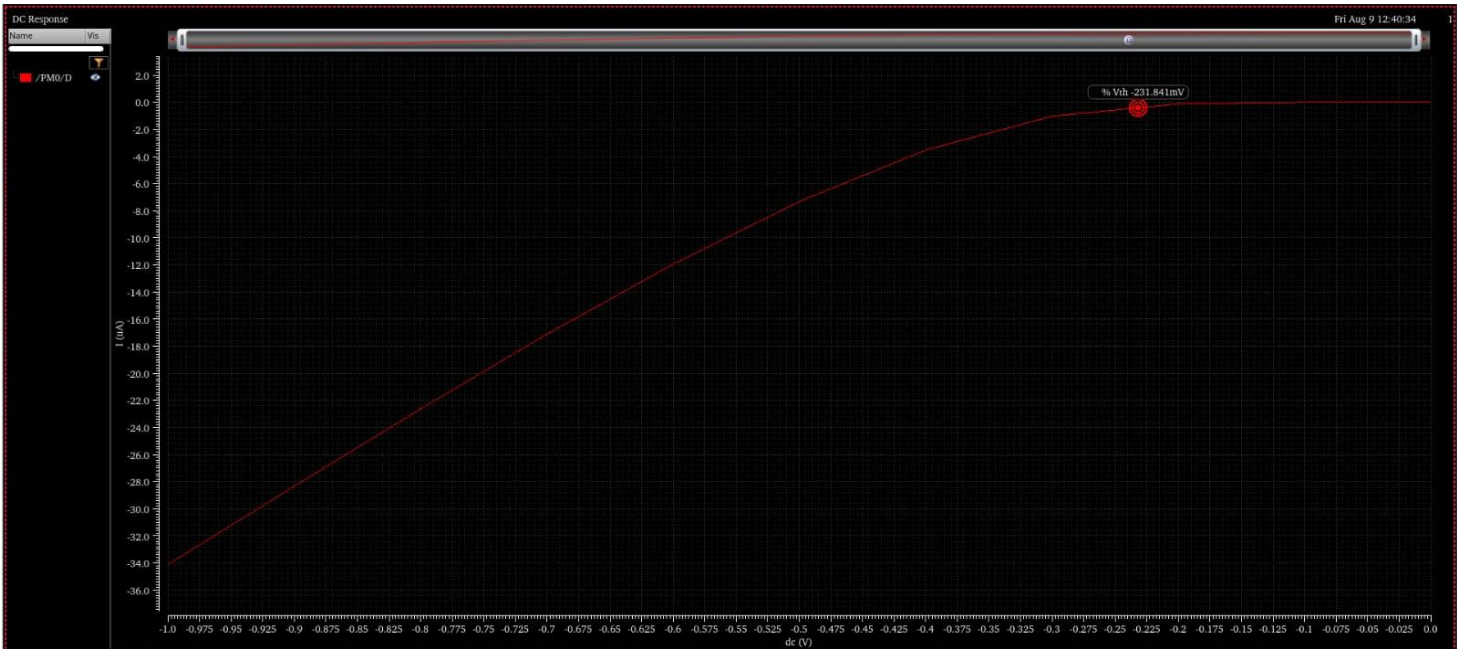


**GRAPHS:**

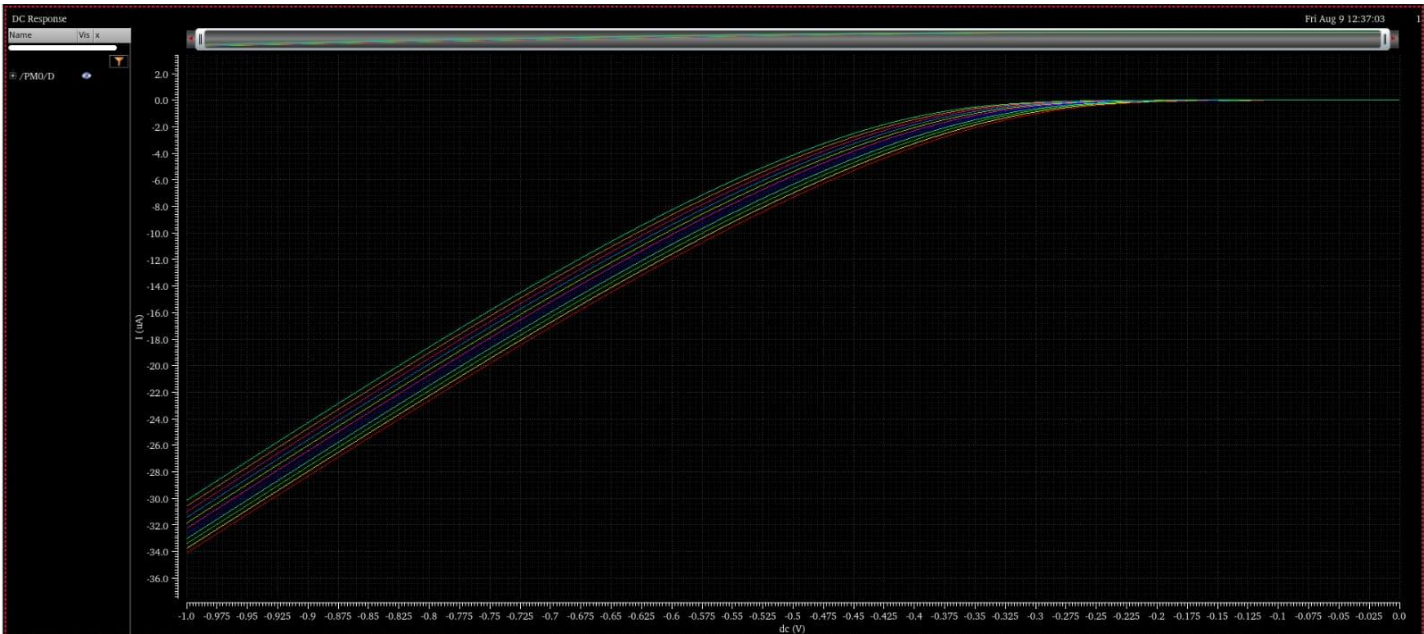
**a)  $I_d$  vs  $V_{ds}$ :**



2)Id vs Vgs:



3)Body Bias Effect:



OBSERVATIONS:

1)Vth :

Results Display Window (on cadence-server)		×
Window	Expressions	Info Help
		cadence
reversed	0	
ron	29.3325K	
rout	99.8308K	
sdint	2.14748G	
sdop	-1	
self_gain	5.78063	
tau1	NaN	
tk	NaN	
trise	NaN	
ueff	8.69274m	
vbs	0	
vdb	-1	
vds	-1	
vdsat	-464.779m	
vdsat_marg	NaN	
vdss	-464.779m	
vearly	3.40342	
vfbeff	-790.378m	
vgb	-1	
vgd	0	
vgs	-1	
vgsteff	703.579m	
vgt	-768.159m	
vsat_marg	-535.221m	
vsb	-0	
vth	-231.841m	
vth0	NaN	
vth_drive	NaN	
		HelpAction

## 2)Vdsat :

Results Display Window (on cadence-server)		×
Window	Expressions	Info Help
		cadence
signal	OP("/PM0" "??")	
qgi	126.328a	
qinv	174.825u	
qsi	79.327a	
qsrco	40.5077a	
region	2	
reversed	0	
ron	29.3325K	
rout	99.8308K	
sdint	2.14748G	
sdop	-1	
self_gain	5.78063	
tau1	NaN	
tk	NaN	
trise	NaN	
ueff	8.69274m	
vbs	0	
vdb	-1	
vds	-1	
vdsat	-464.779m	
vdsat_marg	NaN	
vdss	-464.779m	
vearly	3.40342	
vfbeff	-790.378m	
vgb	-1	
vgd	0	
vgs	-1	
vgsteff	703.579m	
vgt	-768.159m	
vsat_marg	-535.221m	
vsb	-0	
vth	-231.841m	
vth0	NaN	
vth_drive	NaN	

## 4) Channel Length Modulation Coefficient ( $\lambda$ ):

## Task

We calculate the channel width modulation coefficient ( $\lambda$ ) using  $I_{DS}$  vs.  $V_{DS}$  graph,

$$\begin{array}{l|l} V_{DS1} = -710 \text{ mV} & I_{D1} = -31.0064 \mu\text{A} \\ V_{DS2} = -870 \text{ mV} & I_{D2} = -32.7645 \mu\text{A} \end{array}$$

$$\frac{I_{DS1}}{I_{DS2}} = \frac{1 + \lambda V_{DS1}}{1 + \lambda V_{DS2}}$$

Solving this,  $\lambda = \cancel{0.473} - 0.47353 \text{ V}^{-1}$

### 3) Overall Results:

Results Display Window (on cadence-server)																
cadence																
Window	Expressions	Info	Help													
OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")	OP("PMOS")
gateoff	mbus	vds	rs	vthoff	vdsat	vth	vds	vds	vth	vds	vth	vds	vth	vds	vth	trise
190.201u	3.27047u	10.0169u	57.9043u	-790.378m	-464.779m	-231.841m	0	-1	-1	0	-1	-1	-1	-15.7446f	-34.0919u	NaN
190.281u	3.46825u	10.0459u	58.0712u	-789.895m	-466.011m	-241.24m	0	-1.1	-1.1	100n	-1	-1	-1	-15.0843f	-33.7943u	NaN
190.385u	3.63419u	10.0688u	58.2164u	-789.462m	-466.834m	-250.483m	0	-1.2	-1.2	200n	-1	-1	-1	-14.5999f	-33.3987u	NaN
190.509u	3.77684u	10.0864u	58.3429u	-789.07m	-467.316m	-259.61m	0	-1.3	-1.3	300n	-1	-1	-1	-14.2522f	-33.0277u	NaN
190.65u	3.90164u	10.0993u	58.4524u	-788.715m	-467.506m	-268.652m	0	-1.4	-1.4	400n	-1	-1	-1	-14.0144f	-32.6435u	NaN
190.805u	4.01219u	10.1079u	58.5467u	-788.391m	-467.443m	-277.631m	0	-1.5	-1.5	500n	-1	-1	-1	-13.8681f	-32.2475u	NaN
190.974u	4.11101u	10.1126u	58.6269u	-788.095m	-467.154m	-286.561m	0	-1.6	-1.6	600n	-1	-1	-1	-13.8003f	-31.8411u	NaN
191.155u	4.19987u	10.1136u	58.694u	-787.823m	-466.66m	-295.456m	0	-1.7	-1.7	700n	-1	-1	-1	-13.8017f	-31.4254u	NaN
191.346u	4.28009u	10.1113u	58.7488u	-787.572m	-465.981m	-304.322m	0	-1.8	-1.8	800n	-1	-1	-1	-13.8656f	-31.0012u	NaN
191.549u	4.35266u	10.1057u	58.7919u	-787.34m	-465.129m	-313.168m	0	-1.9	-1.9	900n	-1	-1	-1	-13.9873f	-30.5694u	NaN
191.761u	4.41834u	10.0971u	58.8238u	-787.125m	-464.117m	-321.997m	0	-2	-2	1	-1	-1	-1	-14.1634f	-30.1308u	NaN

### Calculations:

1. Channel Length Modulation Coefficient ( $\lambda$ ) for PMOS=-0.47353

### Result and Inference:

In this experiment using Cadence Virtuoso, the PMOS transistor was tested to observe the relationship between its drain current ( $I_D$ ) and drain-to-source voltage ( $V_{DS}$ ) across different gate-to-source voltages ( $V_{GS}$ ). The setup involved applying varying  $V_{DS}$  values while keeping  $V_{GS}$  constant for each sweep. Transient analysis produced output plots showing  $I_D$  versus  $V_{DS}$ , revealing characteristic PMOS behavior: as  $V_{DS}$  increases,  $I_D$  initially rises and then saturates, with higher  $V_{GS}$  values (more negative) leading to increased current due to stronger inversion. This experiment confirmed the expected PMOS operation, highlighting its current control based on  $V_{GS}$  and illustrating key principles of PMOS behavior essential for analog and digital circuit design.