

AIM OF THE PROJECT

Implementation of linear equation solver on FPGA using VHDL . An $N \times N$ matrix can be implemented successfully without much delay .

MOTIVATION

Big linear equations with multiple variable are too difficult for a human being to solve manually. These equations are way too complex to be solved in generic calculators. So we planned to design a FPGA based linear equation solver which can solve equations containing upto 8 variables.

Almost all computer graphics are plagued (for lack of a better word) with applications of linear algebra. For video games, you have to cope with 3D transformation matrices as well as some losses but fast image compression/display methods. In the latter case, the bitmap of an image is taken and take the Singular Value Decomposition of the matrix, and preserve only the values of the Singular Value Decomposition. Now the matrix generated for this purpose generally reaches an order of >5 .

Linear algebra helps in solving Markov chains, a very useful probabilistic tool that is used in all sorts of areas, from biological population dynamics models to economics predictions to traffic flow models to incompressible fluid flow dynamics.

Modern web search engines use many techniques to estimate the relevance of pages. An important one is link analysis based on the concept of eigenvector centrality, which comes from linear algebra.

Apart from the above mentioned applications, there are a lot of areas where complex linear programming is used. Thus a FPGA based linear equation solver solves them all.

INTRODUCTION

The Linear Equation Solver designed used LU Decomposition method, for the solving a set 8 linear equations having 8 unknown variables.

LU DECOMPOSITION METHOD:-

Suppose we have the system of equations $AX = B$.

The motivation for an LU decomposition is based on the observation that systems of equations involving triangular coefficient matrices are easier to deal with. Indeed, the whole point of Gaussian elimination is to replace the coefficient matrix with one that is triangular. The LU decomposition is another approach designed to exploit triangular systems.

We suppose that we can write $A = LU$ where L is a lower triangular matrix and U is an upper triangular matrix. Our aim is to find L and U and once we have done so we have found an LU decomposition of A .

Explicitly,

$$\begin{pmatrix} a_{11} & a_{12} & a_{13} & \dots & a_{1n} \\ a_{21} & a_{22} & a_{23} & \dots & a_{2n} \\ \dots & \dots & \dots & \dots & \dots \\ a_{n1} & a_{n2} & a_{n3} & \dots & a_{nn} \end{pmatrix} = \begin{pmatrix} l_{11} & 0 & 0 & \dots & 0 \\ l_{21} & l_{22} & 0 & \dots & 0 \\ \dots & \dots & \dots & \dots & \dots \\ l_{n1} & l_{n2} & l_{n3} & \dots & l_{nn} \end{pmatrix} \begin{pmatrix} 1 & u_{12} & u_{13} & \dots & u_{1n} \\ 0 & 1 & u_{23} & \dots & u_{2n} \\ \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & 1 \end{pmatrix}$$

Therefore, by LU-decomposition, the system of linear equations $Ax=B$ can be solved in three steps:

- I. Construct the lower triangular matrix L and upper triangular matrix U .
- II. Using forward substitution, solve $Ly=B$.
- III. Solve $Ux=y$, backward substitution.

Algorithm for LU Decomposition:-

Pseudo-code for a simple LU factorization of N x N A matrix:-

```
for k = 1 to N-1 do {for each diagonal element}
  for i = k + 1 to N do {for each element below it}
     $a_{i,k} \leftarrow a_{i,k}/a_{k,k}$  {normalize}
  end for
  for j = k + 1 to N do {for each column right of current diagonal element}
    for l = k + 1 to N do {for each element below it}
       $a_{l,j} \leftarrow a_{l,j} - a_{l,k} \times a_{k,j}$ 
    end for
  end for
end for
```

Algorithm for Forward Substitution:-

Forward substitution to solve $Ly=B$

```
x(1)=b(1)
for i = 2 : n
  s=0
  for j = 1 : i-1
     $s = s + a(i,j) \times x(j)$ 
  end for
   $x(i) = b(i) - s$ 
end for
```

Algorithm for Backward Substitution:-

back substitution to solve $Uy=B$:-

```
x(n) = x(n) / a(n, n)
for i = n-1 : -1 : 1
  s=0
  for j = i+1 to n
     $s = s + a(i, j) \times x(j)$ 
  end for
   $x(i) = (x(i) - s)/a(i,i)$ 
end for
```

Reasons for choosing LU Decomposition:-

LU Decomposition is computationally more efficient than Gaussian elimination when we are solving several sets of equations with the same coefficient matrix but different right hand sides.

For large n , for LU Decomposition, the computational time is proportional to $\frac{4n^3}{3}$, while for Gaussian Elimination, the computational time is proportional to $\frac{n^4}{3}$. So for large n , the ratio of the computational time for Gaussian elimination to computational for LU Decomposition is $\frac{n^4/3}{4n^3/3} = \frac{n}{4}$.

As an example, to find the inverse of a 2000×2000 coefficient matrix by Gaussian Elimination would take $n/4 = 2000/4 = 500$ times the time it would take to find the inverse by LU Decomposition.

FLOWCHARTS:-

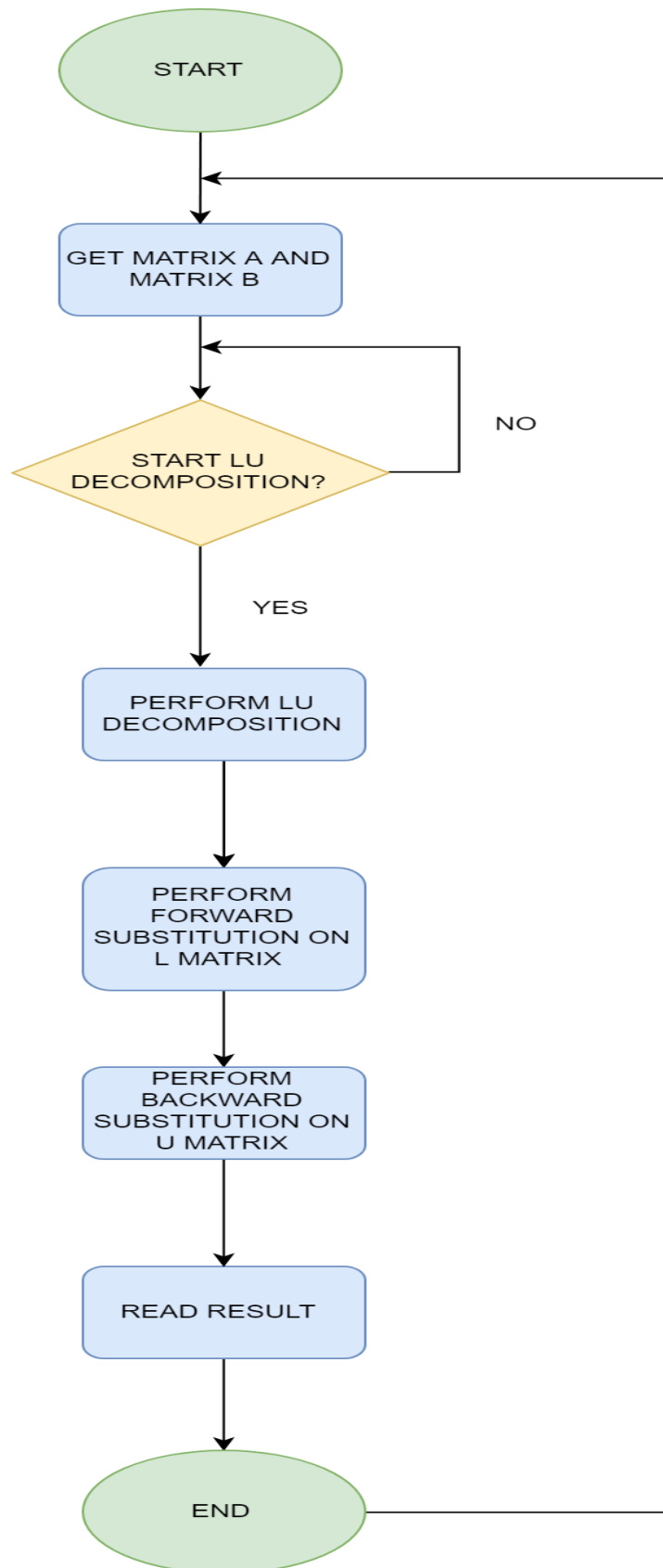


Figure 1 Top level flowchart of linear equation solver

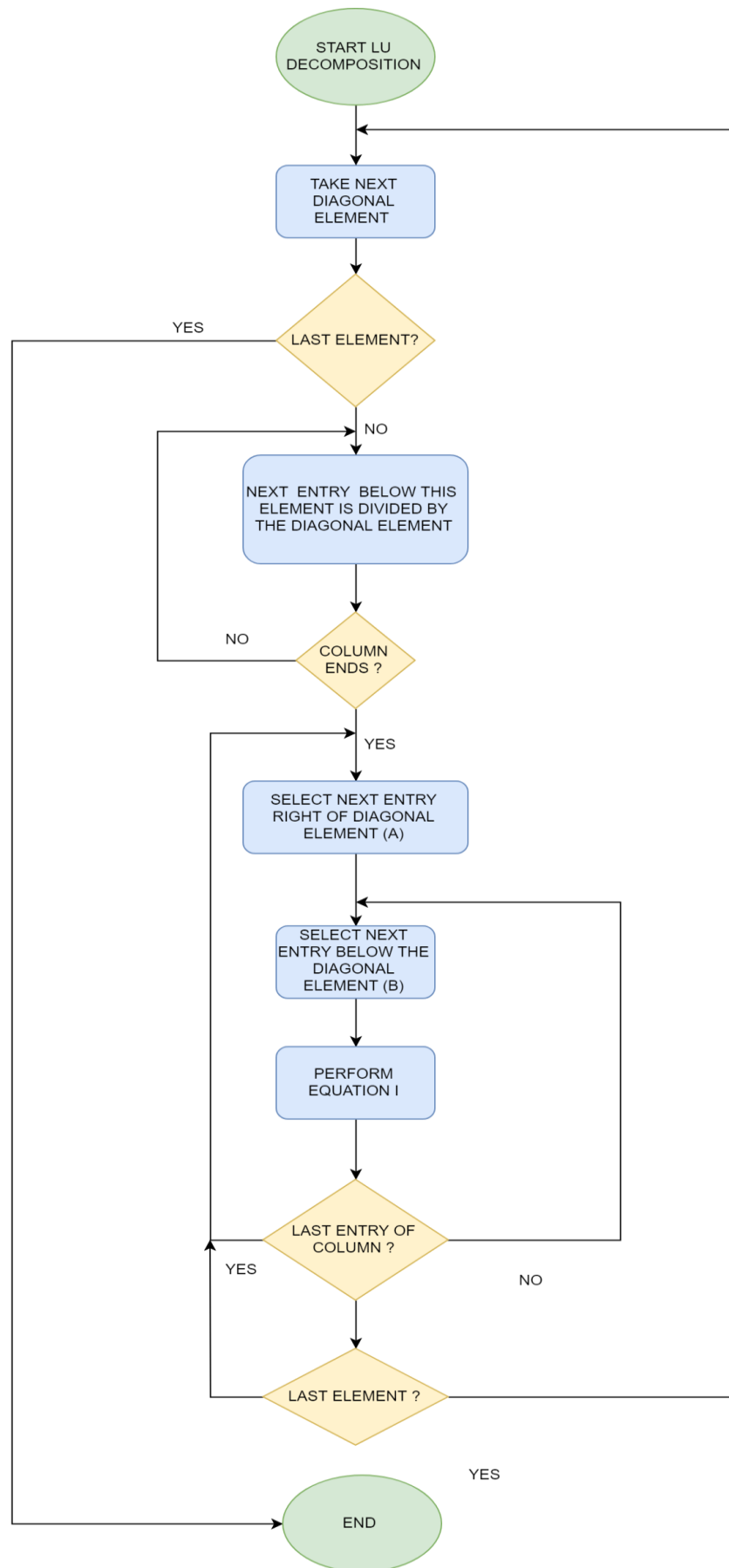


Figure 2 LU Decomposition

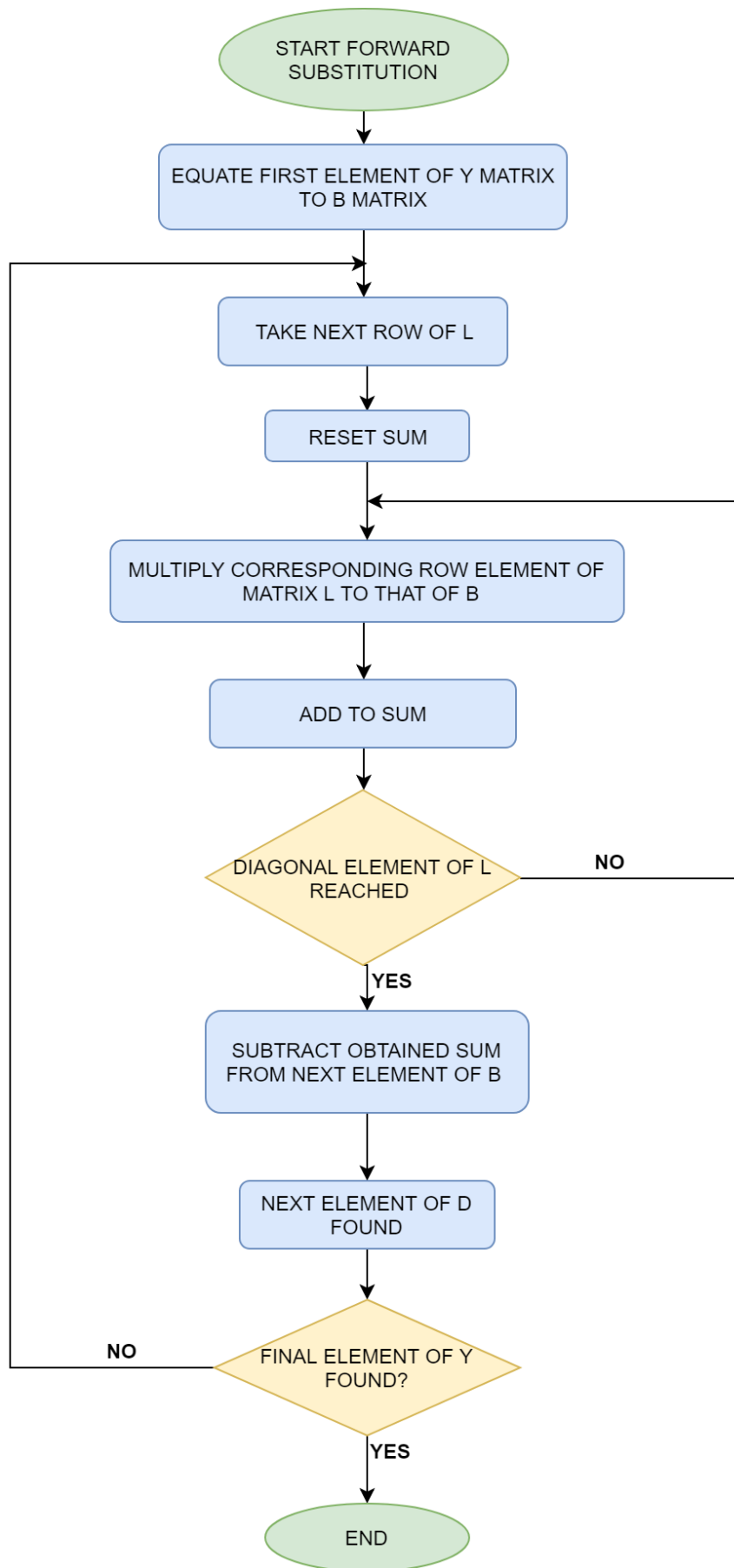


Figure 3 Solving $Ly=B$

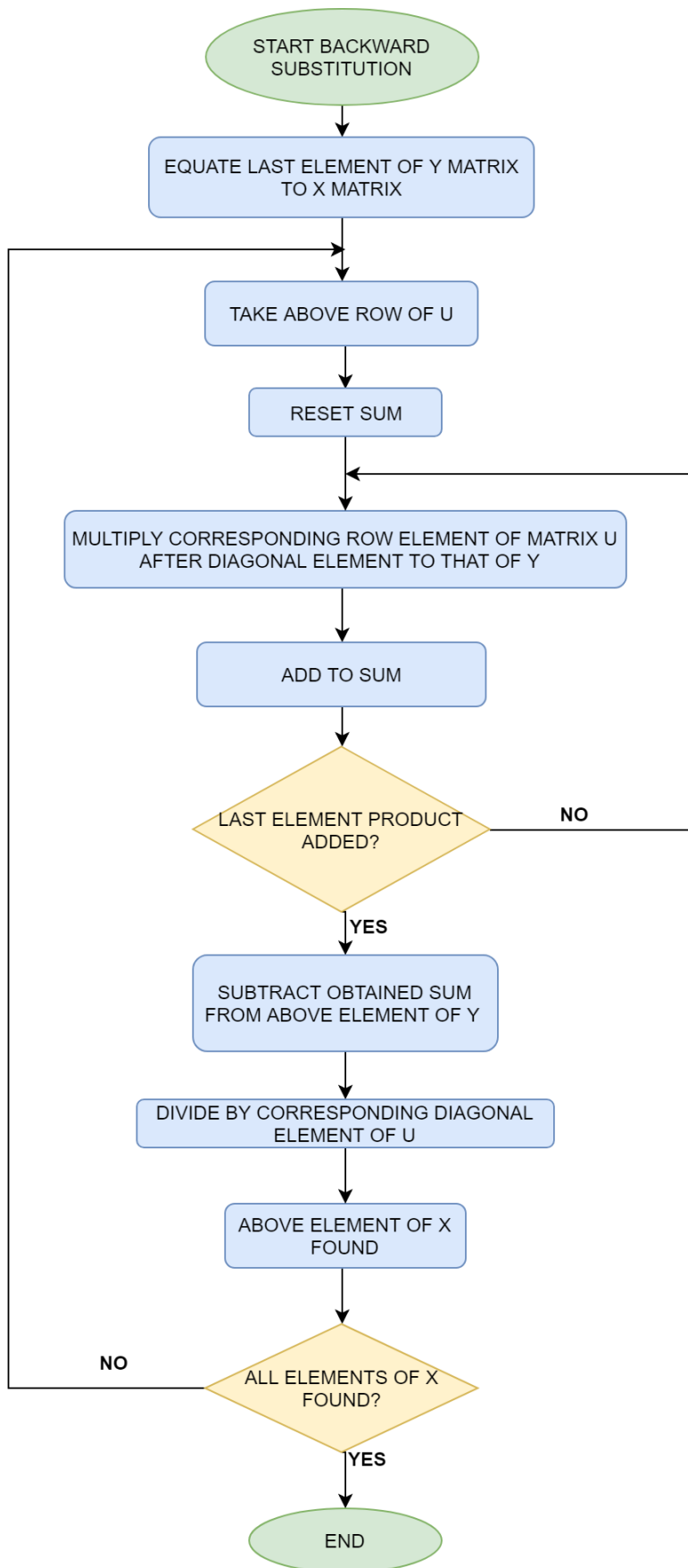


Figure 4 Solving $Ux=Y$

GUIDELINES TO BUILD PROJECT IN NIOS II

HARDWARE

- 1 Open Project File
- 2 Add all files --> <Project Directory>\LU_Linear_Equation_Solver\synthesis\submodules
- 3 Add file "LU_Linear_Equation_Solver.vhd"<Project Directory > \LU_Linear_Equation_Solver\synthesis
- 4 Set "LU_Linear_Equation_Solver.vhd" as top level entity
- 5 Compile Design
- 6 Program the Deo – Nano FPGA
- 7 Tools -> NIOS II Software Build Tools for Eclipse
- 8 Make a new workspace directory.
- 9 File -> New -> Nios II Application BSP from template.
- 10 Select the sopcinfo file inside GS_nios1 folder (<Project Directory>\LU_Linear_Equation_Solver.sopcinfo).
- 11 Open hello_world_small.c from <Project Directory>\software
- 12 Copy the contents from above file to hello_world_small.c in the project .
- 13 Build the project.
- 14 Run as Nios II hardware .

RTL MODELSIM SIMULATION

1. Open Project
2. Add file "LU_Componants.vhd" from <Project Directory> \LU_Components
3. Add files "Float_32_Add.vhd" , "Float_32_Div.vhd" and "Float_32_Mult.vhd" from <Project Directory>\IP_Componants.
4. Go to Hierarchy , right click on LU_Controller , Select settings , goto General , enter LU_Controller as top level entity
5. Run Analysis & Synthesis. (Don't Compile)
6. Run RTL Simulation
7. Run Vsim RTL simulation "LU_Controller_8x8_models.txt.txt" <Project Directory> \Testbenches.

AN EXAMPLE

$$\begin{bmatrix} 6 & 4 & 1 & -3 & -2 & -3 & 5 & 8 \\ -1 & 10 & 2 & 4 & 3 & 1 & 9 & 2 \\ 4 & 2 & 9 & 5 & -1 & 2 & -5 & -3 \\ 5 & -4 & -3 & 9 & 4 & 7 & 8 & 6 \\ 3 & 2 & 8 & 7 & 10 & 6 & 5 & 1 \\ -5 & 5 & 4 & 3 & 1 & 7 & 5 & 8 \\ 2 & 1 & 5 & 6 & -8 & 5 & 11 & 6 \\ 2 & 4 & 5 & 7 & -5 & 6 & 4 & 2 \end{bmatrix} \times \begin{bmatrix} x1 \\ x2 \\ x3 \\ x4 \\ x5 \\ x6 \\ x7 \\ x8 \end{bmatrix} = \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ 8 \end{bmatrix}$$

Y MATRIX FOUND FROM LY=B

1.000
2.166
2.469
5.34
1.6
5.96
1.97
1.437

RESULTANT X MATRIX FOUND

0.49
0.3256
0.0602
-0.657
-0.23
1.454
0.1723
-0.282

TIMING ANALYSIS

FOR SLOW 1200MILIVOLTS 85C MODEL

SUMMARY

The screenshot shows the Timing Analyzer Summary report for the Slow 1200mV 85C Model. The left pane displays the Table of Contents, with the Timing Analyzer section expanded. The main pane shows a table with the following data:

	Fmax	Restricted Fmax	Clock Name	Note
1	160.98 MHz	160.98 MHz	altera_reserved_tck	

Below the table, a note states: "This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such

SETUP SUMMARY

The screenshot shows the Timing Analyzer Setup Summary report for the Slow 1200mV 85C Model. The left pane displays the Table of Contents, with the Timing Analyzer section expanded. The main pane shows a table with the following data:

	Clock	Slack	End Point TNS
1	altera_reserved_tck	46.894	0.000

HOLD SUMMARY

Slow 1200mV 85C Model Hold Summary			
<<Filter>>			
	Clock	Slack	End Point TNS
1	altera_reserved_tck	0.358	0.000

FOR SLOW 1200 MILIVOLTS OC MODEL

SUMMARY

Slow 1200mV OC Model Fmax Summary				
<<Filter>>				
	Fmax	Restricted Fmax	Clock Name	Note
1	166.94 MHz	166.94 MHz	altera_reserved_tck	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including

SETUP SUMMARY

Compilation Report - Linear_Equation_Solver

Table of Contents

- > Analysis & Synthesis
- > Fitter
- > Assembler
- ▼ Timing Analyzer
 - Summary
 - Parallel Compilation
 - Clocks
 - > Slow 1200mV 85C Model
 - ▼ Slow 1200mV 0C Model
 - Fmax Summary
 - Setup Summary
 - Hold Summary
 - Recovery Summary
 - Removal Summary
 - Minimum Pulse Width Summary

Slow 1200mV 0C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	altera_reserved_tck	47.005	0.000

HOLD SUMMARY

Compilation Report - Linear_Equation_Solver

Table of Contents

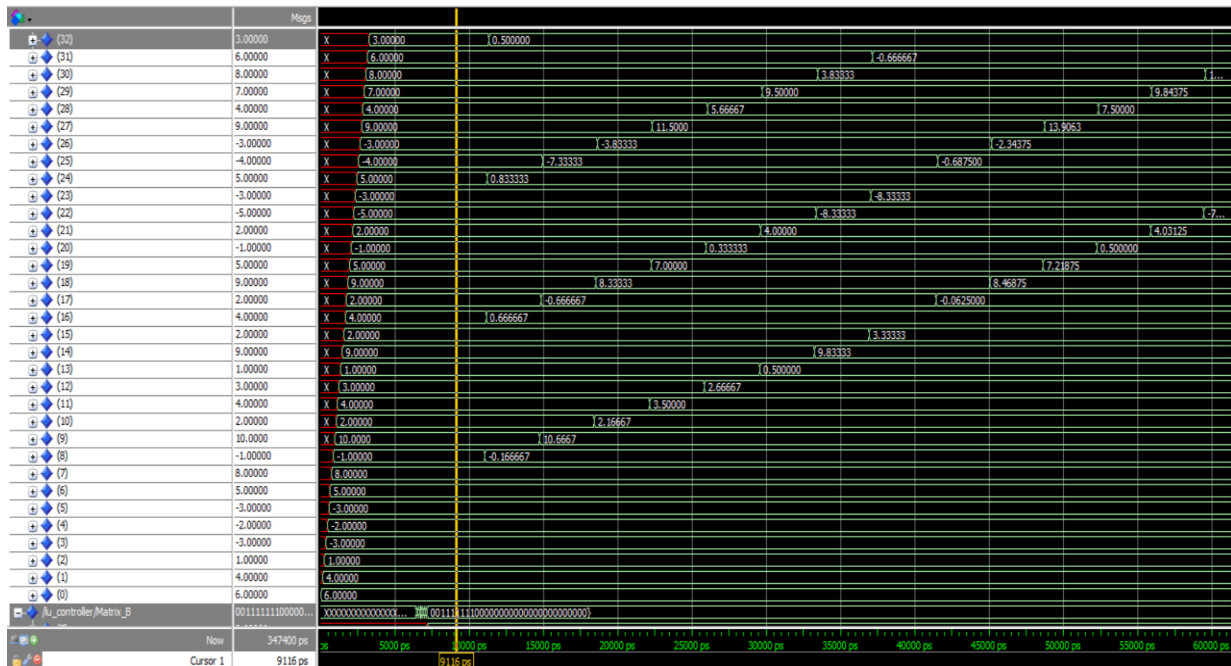
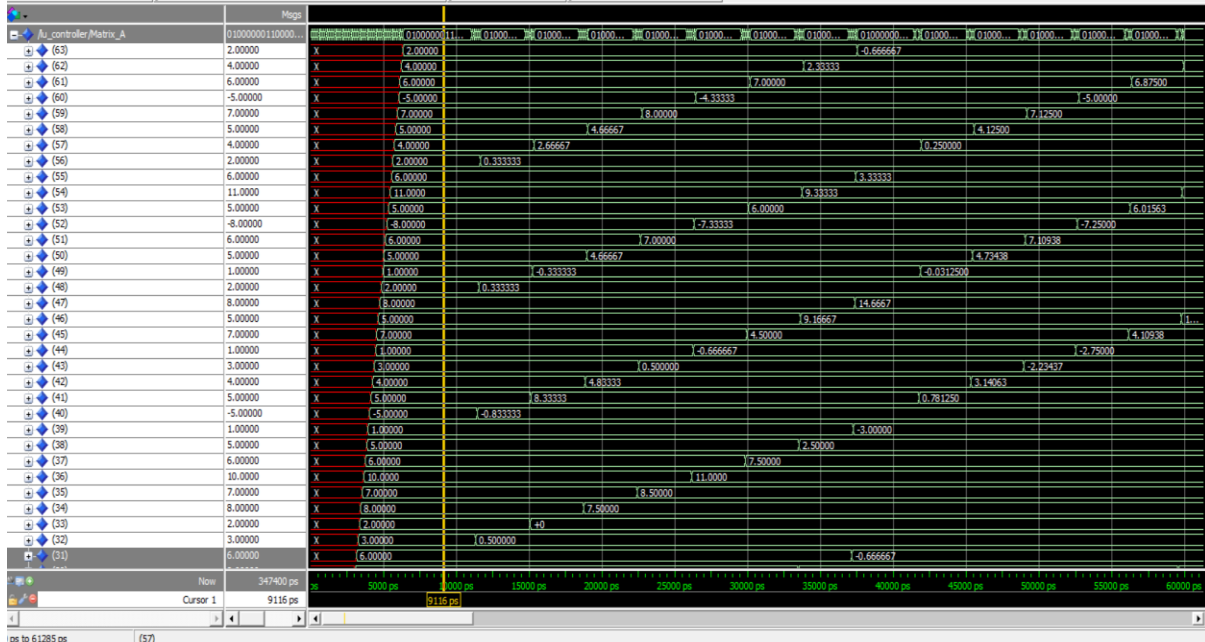
- > Analysis & Synthesis
- > Fitter
- > Assembler
- ▼ Timing Analyzer
 - Summary
 - Parallel Compilation
 - Clocks
 - > Slow 1200mV 85C Model
 - ▼ Slow 1200mV 0C Model
 - Fmax Summary
 - Setup Summary
 - Hold Summary
 - Recovery Summary
 - Removal Summary
 - Minimum Pulse Width Summary

Slow 1200mV 0C Model Hold Summary

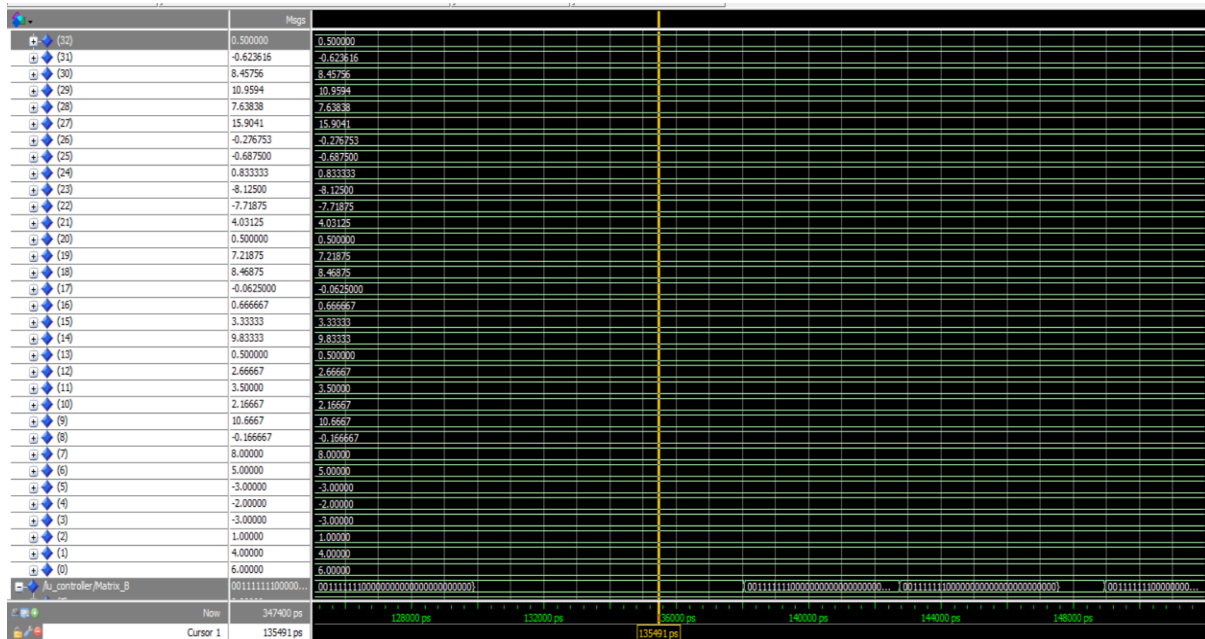
<<Filter>>

	Clock	Slack	End Point TNS
1	altera_reserved_tck	0.311	0.000

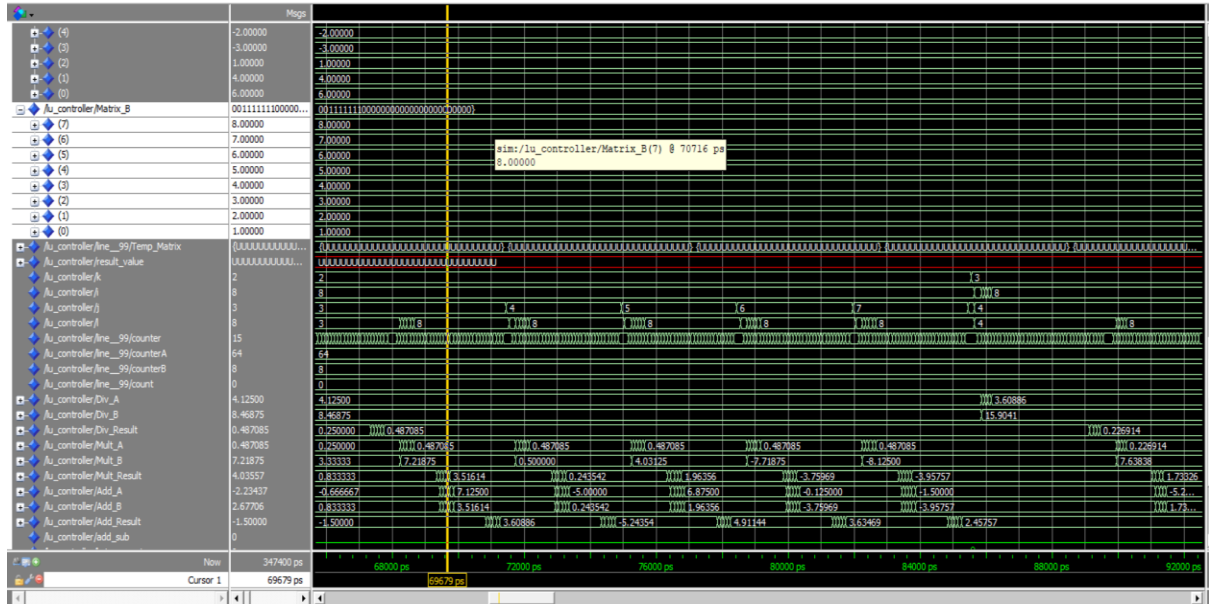
A MATRIX BEFORE LU DECOMPOSITION



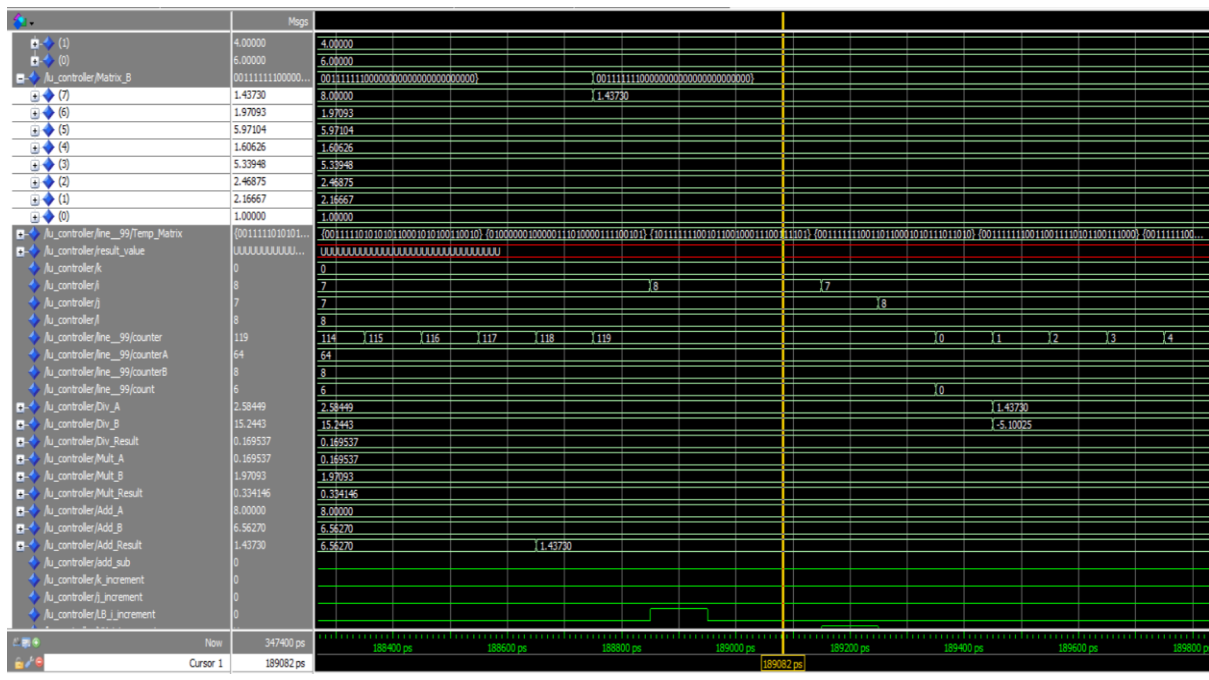
A MATRIX AFTER LU DECOMPOSITION



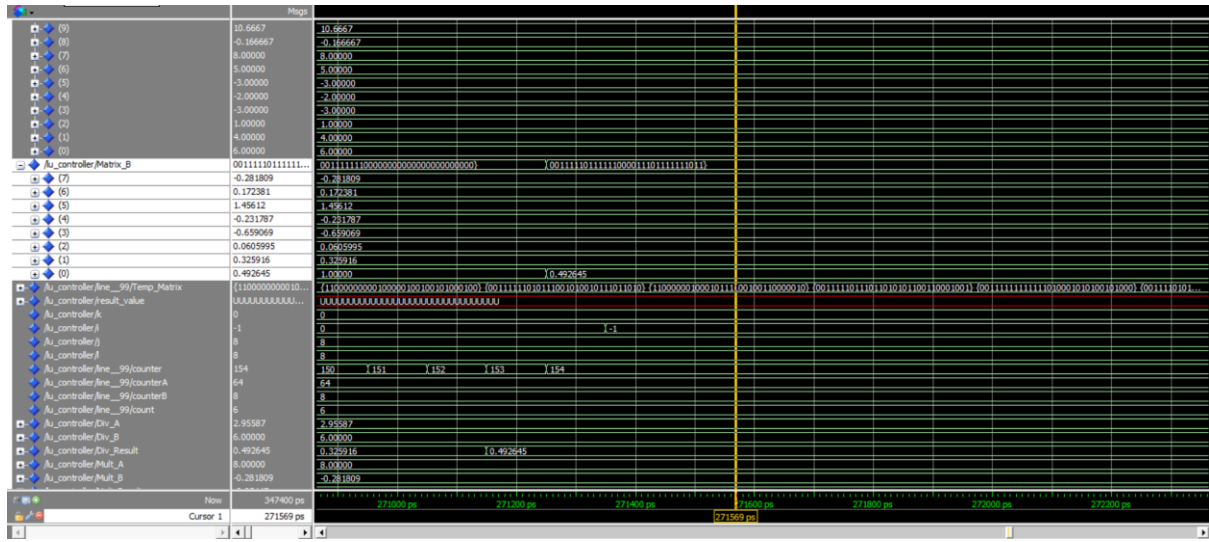
B MATRIX



Y MATRIX AFTER EXECUTING LY=B



FINAL SOLUTION AFTER $UX=Y$



OUTPUT FROM NIOS II

```
Nios II - Eclipse
File Edit Source Refactor Navigate Search Project Run Nios II Window Help

Project Explorer
  LU_Matrix_Solver_1
  LU_Matrix_Solver_1_bsp [LU_Linear_Equation_Solver]

hello_world_small.c
2 * "Small Hello World" example.
80
81 #include "sys/alt_stdio.h"
82 #include "system.h"
83 #include "io.h"
84 #include <stdio.h>
<

Problems Tasks Console Nios II Console Properties
LU_Matrix_Solver_1 New Nios II Hardware configuration - cable: USB blaster on localhost [328-0] device ID: 1 instance ID: 0 name: /log_uart_0.log

Hello from Nios II!
Matrix A is
40e00000 40800000 3f800000 c0400000 c0000000 c0400000 40a00000 41000000
bf800000 41200000 40000000 40800000 40400000 3f800000 41100000 40000000
40800000 40000000 41100000 40a00000 bf800000 40000000 c0a00000 c0400000
40a00000 c0800000 c0400000 41100000 40800000 40e00000 41000000 40000000
40400000 40000000 41000000 40e00000 41200000 40c00000 40a00000 3f800000
c0a00000 40a00000 40800000 40400000 3f800000 40e00000 40a00000 41000000
40000000 3f800000 40a00000 40000000 41000000 40a00000 41300000 40000000
40000000 40800000 40a00000 40e00000 40c00000 40c00000 40800000 40000000

Matrix B is
3f800000 40000000 40400000 40800000 40e00000 40c00000 40e00000 41000000
Writing 0x1 to control/status register to trigger the operation.

Answer is
3efc0bfb 3e6d6d0f 3d737329 bf22b0c5 be6d5959 3fde2202 3e30f4ee be914944
```

FITTER ANALYSIS

Table of Contents		Flow Summary	
<ul style="list-style-type: none">Flow SummaryFlow SettingsFlow Non-Default Global SettingsFlow Elapsed TimeFlow OS SummaryFlow LogAnalysis & SynthesisFitter<ul style="list-style-type: none">Flow MessagesFlow Suppressed Messages		<<Filter>>	
		Flow Status	Successful - Fri May 03 03:36:49 2019
		Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
		Revision Name	Linear_Equation_Solver
		Top-level Entity Name	LU_Controller
		Family	Cyclone IV E
		Device	EP4CE22F17C6
		Timing Models	Final
		Total logic elements	19,725 / 22,320 (88 %)
		Total registers	5707
		Total pins	70 / 154 (45 %)
		Total virtual pins	0
		Total memory bits	1,300 / 608,256 (< 1 %)
		Embedded Multiplier 9-bit elements	7 / 132 (5 %)
		Total PLLs	0 / 4 (0 %)

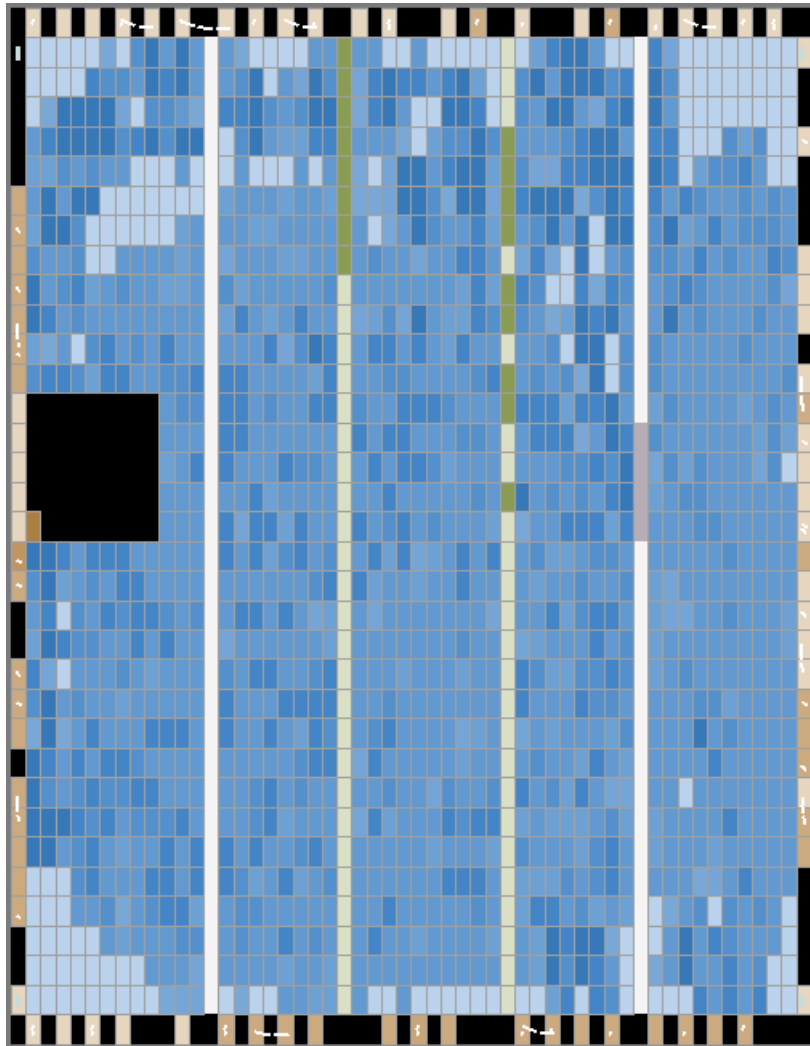
LOGIC ELEMENTS USED- 19725/22320 (95%)

TOTAL PINS – 70/154

THE DESIGN , IS FITTED PROPERLY INTO THE DE0-NANO FGPA , AS LONG AS FPGA HAS ENOUGH MEMORY .

THE DESIGN SUCCESSFULLY IMPLEMENTS A N×N MATRIX AND THUS A N×N LINEAR EQUATION SOLVER

CHIP-PLANNER



FUTURE SCOPE

- 1 It is assumed that the matrix entered is already pivoted.
- 2 The design encounters difficulties if diagonal elements are zero.

REFERENCES

1 Portable and Scalable FPGA-Based Acceleration of a Direct Linear System Solver by Wei Zhang , 2008, Department of Electrical and Computer Engineering University of Toronto.

2 Steven Chapra and Raymond Canale, Numerical Methods for Engineers, Fourth Edition, McGrawHill, 2002 (see Sections 10.1-10.2)

3 http://csep10.phys.utk.edu/guidry/phys594/lectures/linear_algebra/