Digital Logic Recap

ECSE 324: Computer Organization

Fall 2023 - Tutorial 1

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Outline

- Boolean Algebra
- Combinational Circuits
- Sequential Circuits

Boolean Algebra

- Operations: OR $(+)$;

  AND $(\times)$ (omit $\times$ for saving space);

  NOT ($'$ or $\bar{\ }$).

- Laws: Commutative $(a + b = b + a, ab = ba)$;

  Distributed $(a \times (b + c) = ab + ac, a + bc = (a + b)(a + c))$;

  Associative $(a + (b + c) = (a + b) + c, a(bc) = (ab)c)$;

  Identity $(a + 0 = a, a \times 1 = a)$;

  Complement $(a + a' = 1, a \times a' = 0)$.

Boolean Algebra

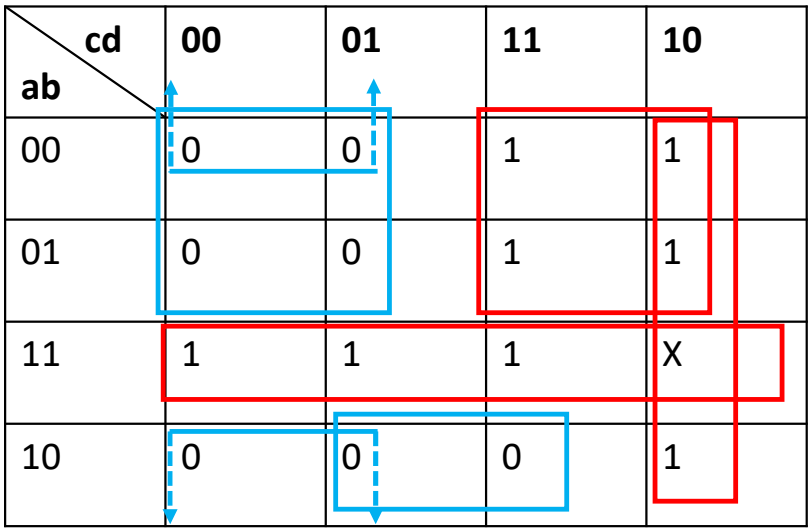
- DeMorgan's Laws: $(a + b + c + \cdots)' = a' \times b' \times c'$ …;
  $(a \times b \times c \times \cdots)' = a' + b' + c' + \cdots.$

- Sum of Product (SOP): $(a \times b) + (c \times d)$.

- Product of Sum (POS): $(a + b) \times (c + d)$.

Boolean Algebra

- K-Map



SOP

$$f = ca' + ab + cd'$$

POS

$$f = (a + c)(b + c)(a' + b + d')$$

Boolean Algebra

ab \ cd	00	01	11	10
00	1	1	1	1
01	1			
11	1			
10	1			

Why SOP? Why POS?

Simplify the logical expression!

$$f = a'b'c'd' + a'b'c'd + a'b'cd + a'b'cd' + a'bc'd' + abc'd' + ab'c'd'$$

$$f = a'b' + c'd'$$

Boolean Algebra

Q1

Simplify the following expression:

$f = (a' + b' + c + d) \times (a' + b' + c + d') \times (a' + b' + c' + d') \times (a + b' + c' + d') \times (a + b + c' + d') \times (a + b + c' + d) \times (a + b' + c' + d) \times (a' + b + c' + d)$

Combinational Circuits

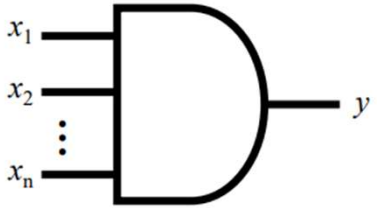
Logic gates:

NOT gate: $y = x'$

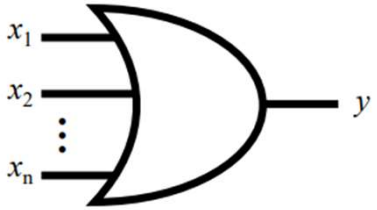
AND gate: $y = x_1 \times x_2$

OR gate: $y = x_1 + x_2$

n inputs AND gates: $y = x_1 \times x_2 \times \cdots$

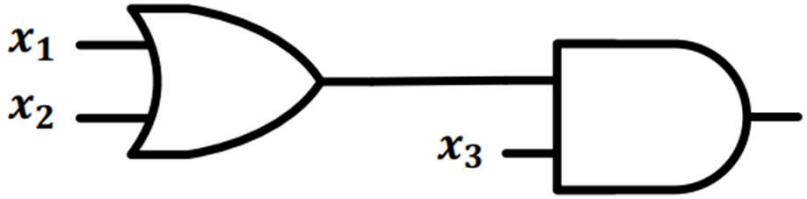


n inputs OR gates: $y = x_1 + x_2 + \cdots$

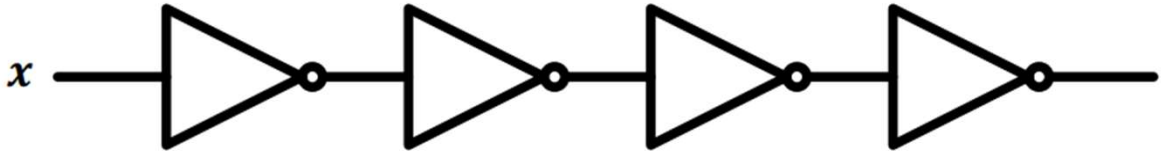


Combinational Circuits

$(x1 + x2) \times x3$:



$(((x')')')'$:



Combinational Circuits

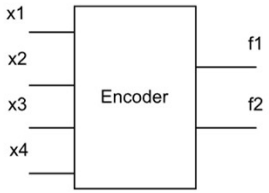
Q2

What is the difference between a demultiplexer and a decoder?

Combinational Circuits

Q3

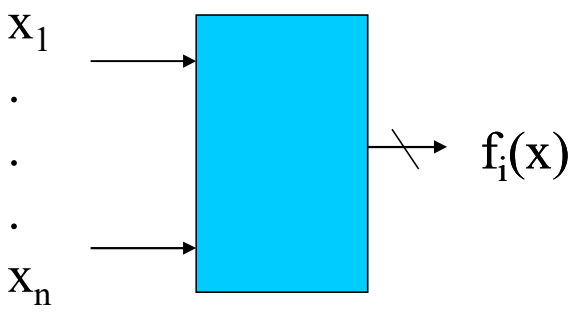
Design a combinational circuit for the following one-hot encoder:

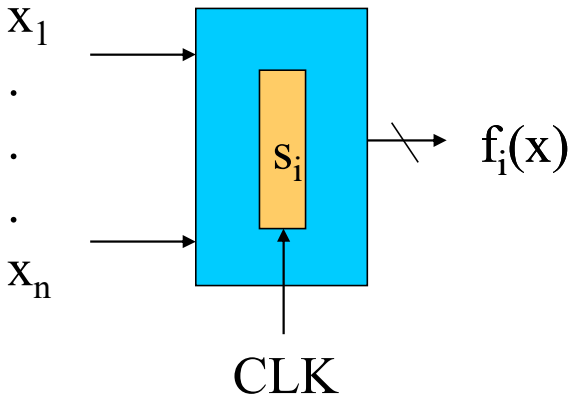


x1	x2	x3	x4	f1	f2
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Sequential Circuits

Combinatorial vs Sequential:





Combinational: $y_i = f_i(x_1,..,x_n)$

Sequential: 1) Memory 2) Time Steps (Clock)

$y_i^t = f_i(x_1^t,\ldots,x_n^t, s_1^t, \ldots,s_m^t)$

$S_i^{t+1} = g_i(x_1^t,\ldots,x_n^t, s_1^t,\ldots,s_m^t)$

Sequential Circuits

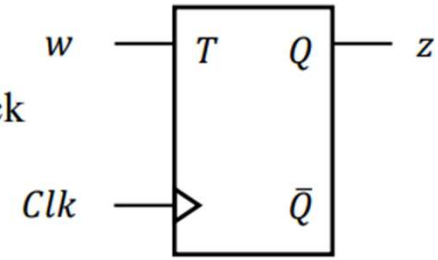
Q4 What is the difference between a latch and a flip-flop?

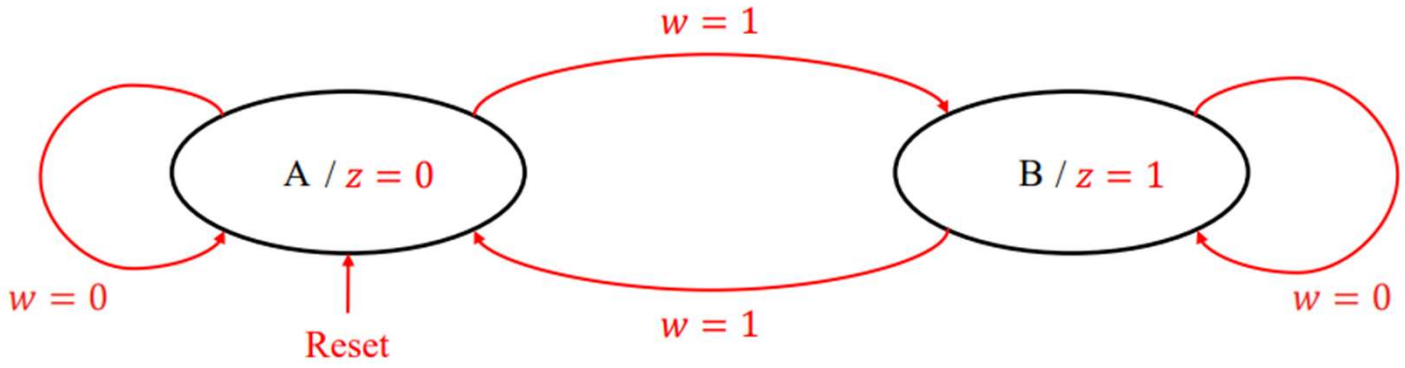
Sequential Circuits

Q5 What is the difference between different designs (Mealy and Moore Machine) of a finite state machine (FSM)?

Sequential Circuits

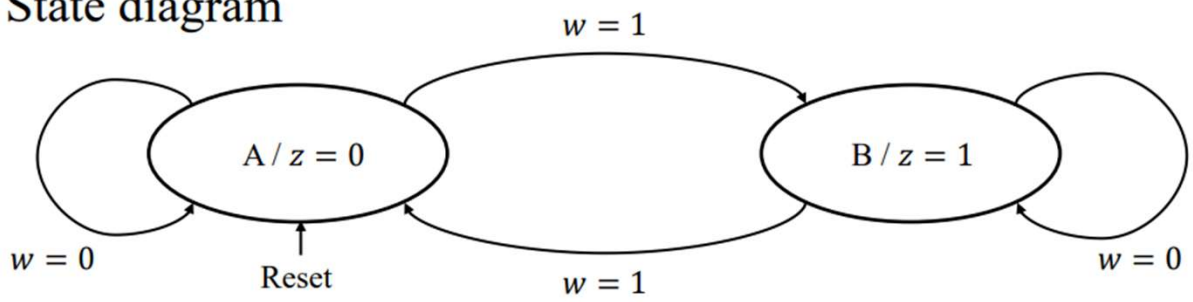
- The FSM (TFF) can be in one of two states
  - State A: $Q = 0$
  - State B: $Q = 1$
- Depending on the input, the FSM may change states at each positive edge of the clock
  - When $w = 0$ the state does not change
  - When $w = 1$ the state toggles
- The output z depends on the state only → Moore FSM
- Initial state: the state at which the FSM "starts"





State Diagram and Table

State diagram



State table

Present state	Next state		Output z
	$w = 0$	$w = 1$	
A	A	B	0
B	B	A	1

Sequential Circuits

Q6

Write down a state transition diagram for a sequence detector that detects two consecutive bit 1s in the input data stream. 1 bit arrives at the input per clock cycle. For example, a bit 0 arrives at the clock period 1, a bit 1 arrives at the clock period 2, a bit 1 arrives at the clock period 3, and the detector outputs the signal for successfully detecting two consecutive bit 1s. If the next incoming bit is 1 once two consecutive bit 1s are detected, the detector still outputs the signal for successfully detecting two consecutive bit 1s.