

**Nirma University Institute of Technology**

**Minor in Electronics and Communication Engineering**

**Semester – V(ODD 2024)**

**3EC101IC24 – Electronic Circuit Design using CMOS**

**SPECIAL ASSIGNMENT**

**22BCE296**

**4:1 MULTIPLEXER**

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# Introduction to multiplexer

Multiplexer is a combinational circuit. It has *2n*inputs line and one output line. In other word the multiplexer is a multiple inputs and one output. The binary information is place on the input line and directed to output line. The output line selection depends upon on the select line. Generally the number of input lines depends on the power of two such as 2, 4, 8, 16, etc. some of the most commonly usable multiplexer is 2 to 1, 4 to 1, 8 to 1 and 16 to 1 multiplexers. Multiplexer is also available in IC forms various input and select line configurations. Some multiplexer ICs are listed below.

* 1. 74157 = Quad 2-to-1 multiplexer
  2. 8158 = Quad 2-to-1 multiplexer
  3. 74153 = 4-to-1 multiplexer
  4. 74152 = 8-to-1 multiplexer
  5. 74150 = 16-to-1 multiplexer.

Multiplexers are also used in digital communications for signal processing.There are several types of multiplexing techniques used in digital communication systems, including:

1. Time Division Multiplexing (TDM): TDM is a technique where multiple signals are transmitted one after the other over a single channel. Each signal is assigned a time slot or time interval, and the channel is shared among the signals in a cyclical manner.
2. Frequency Division Multiplexing (FDM): FDM is a technique where multiple signals are transmitted simultaneously over a single channel by dividing the frequency spectrum of the channel into multiple frequency bands, each band carrying a different signal.

# 4:1 Multiplexer

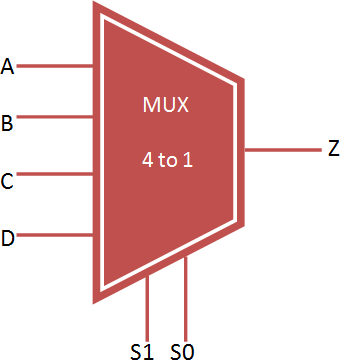
A 4 to 1 [MUX](https://www.knowelectronic.com/multiplexer/) contains “FOUR” input lines and these are A,B,C and D two selected lines S0 and S1 and one output Z-line. Selected lines S0 and S1 select one of the four input lines to connect the outgoing line. The figure below shows a 4 to 1 MUX block diagram where, the multiplexer determines the input by the selected line.Following is the block

diagram for 4x1 MUX.Configuration of selection lines(S1,S0) will determine the output of the MUX.

The following is figure of a 4:1 representation.

# Truth table:

For input lines S1 and S0,following is the truth table:

|  |  |  |
| --- | --- | --- |
| **S1** | **S0** | **Output** |
| 0 | 0 | A |
| 0 | 1 | B |
| 1 | 0 | C |
| 1 | 1 | D |

# Question and answers:

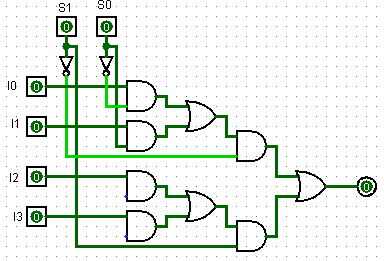
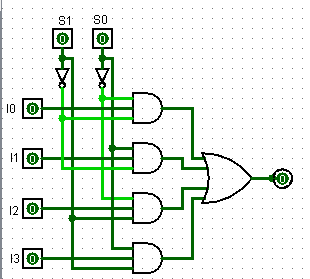
3.1) Find out the optimized Boolean equation for 4:1 MUX?

Ans. From the truth table provided in introduction,we can derive the Boolean equation:

Y = I0S0‘S1’+ I1S0S1‘ + I2S0’S1 + I3S0S1

       = S1 ( I0S0‘ + I1S0 ) + S1( I2S0‘ + I3S0 )

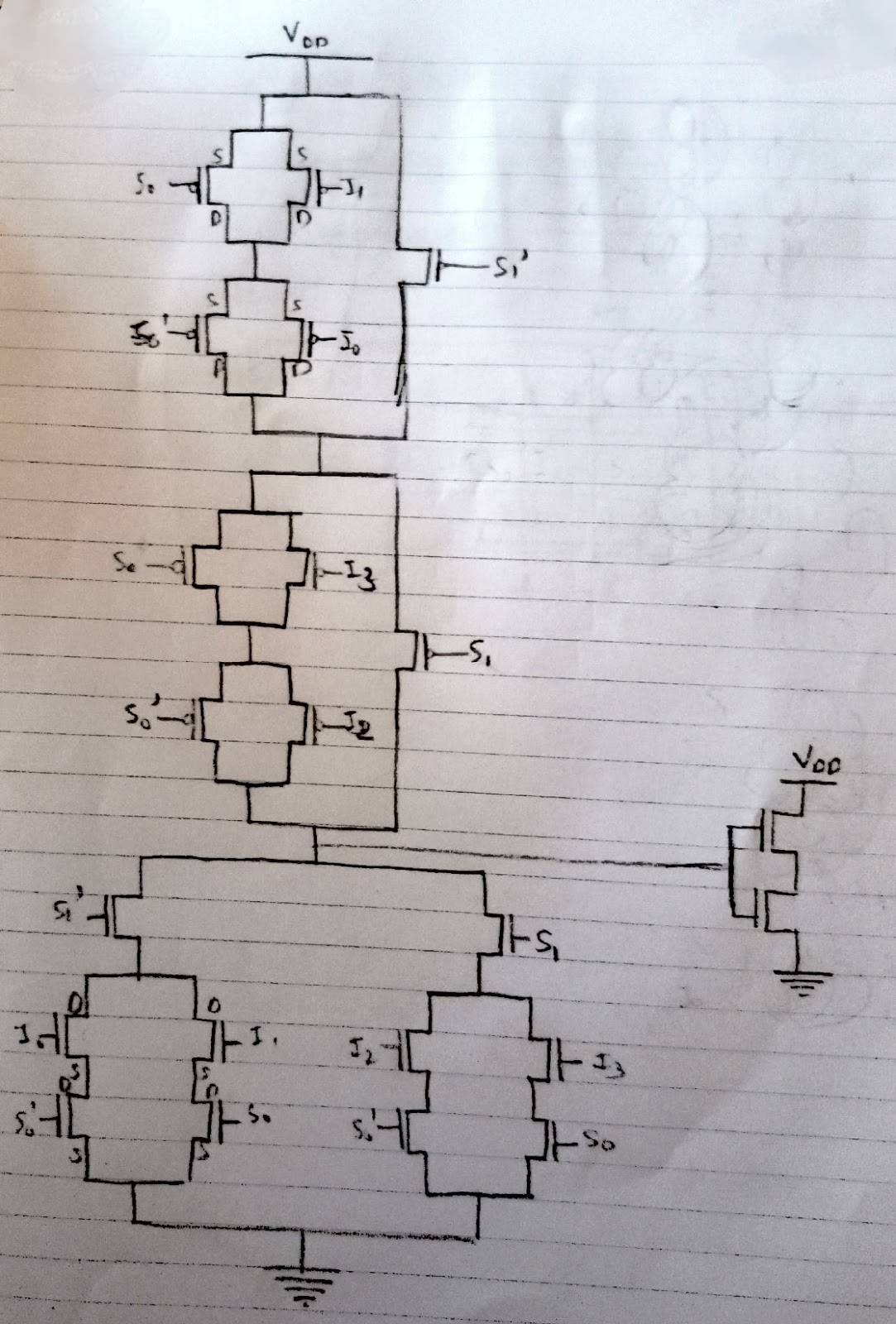
3.2) Draw the optimized gate level circuit diagram. Ans.Following is the logical circuit for 4:1 MUX:



Y = I0S0‘S1’+ I1S0S1‘ + I2S0’S1 + I3S0S1 Y = S1 ( I0S0‘ + I1S0 ) + S1(I2S0‘ + I3S0)

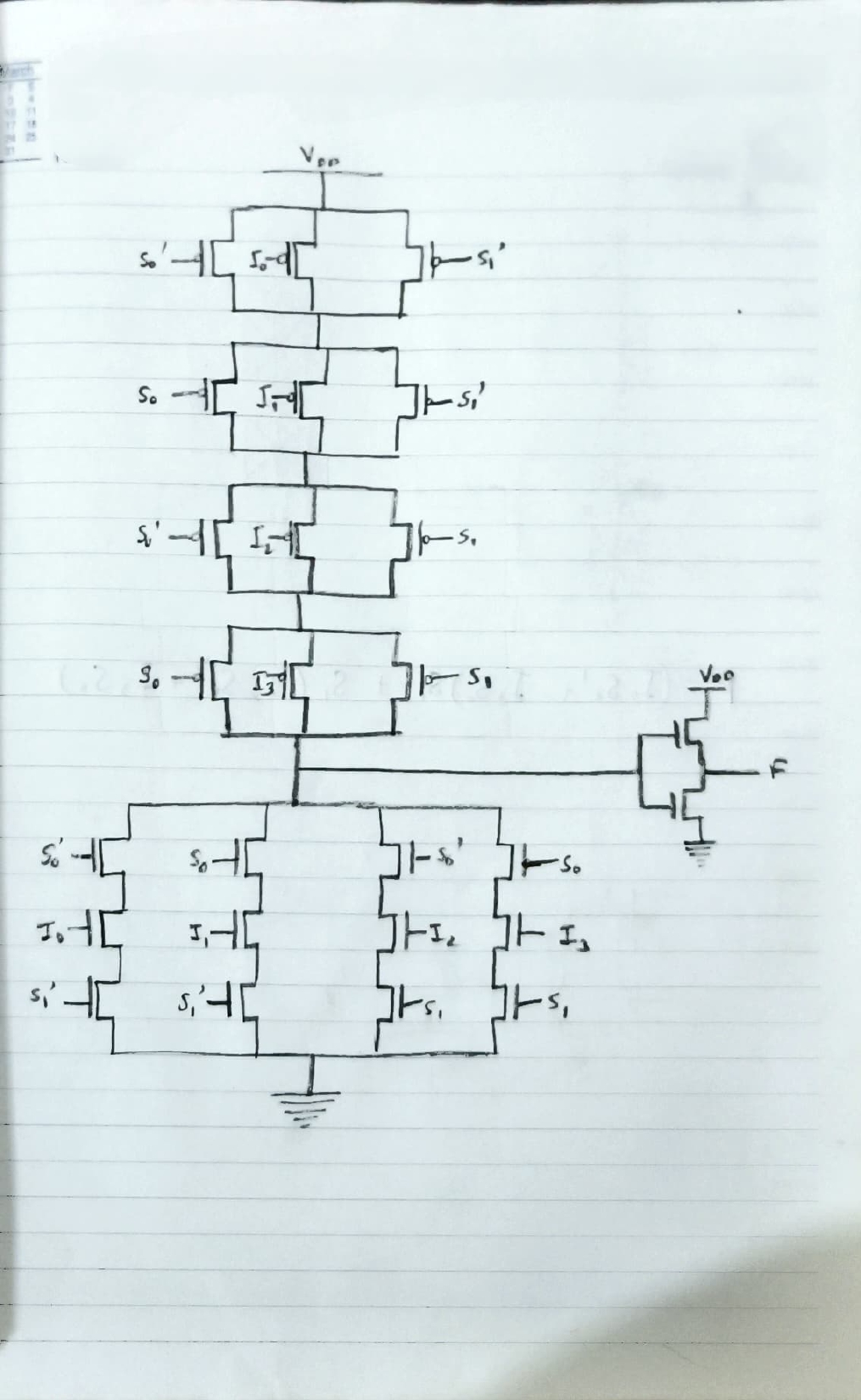
3.3) Draw the transistor level schematic for CMOS/MOS implementation

Ans.



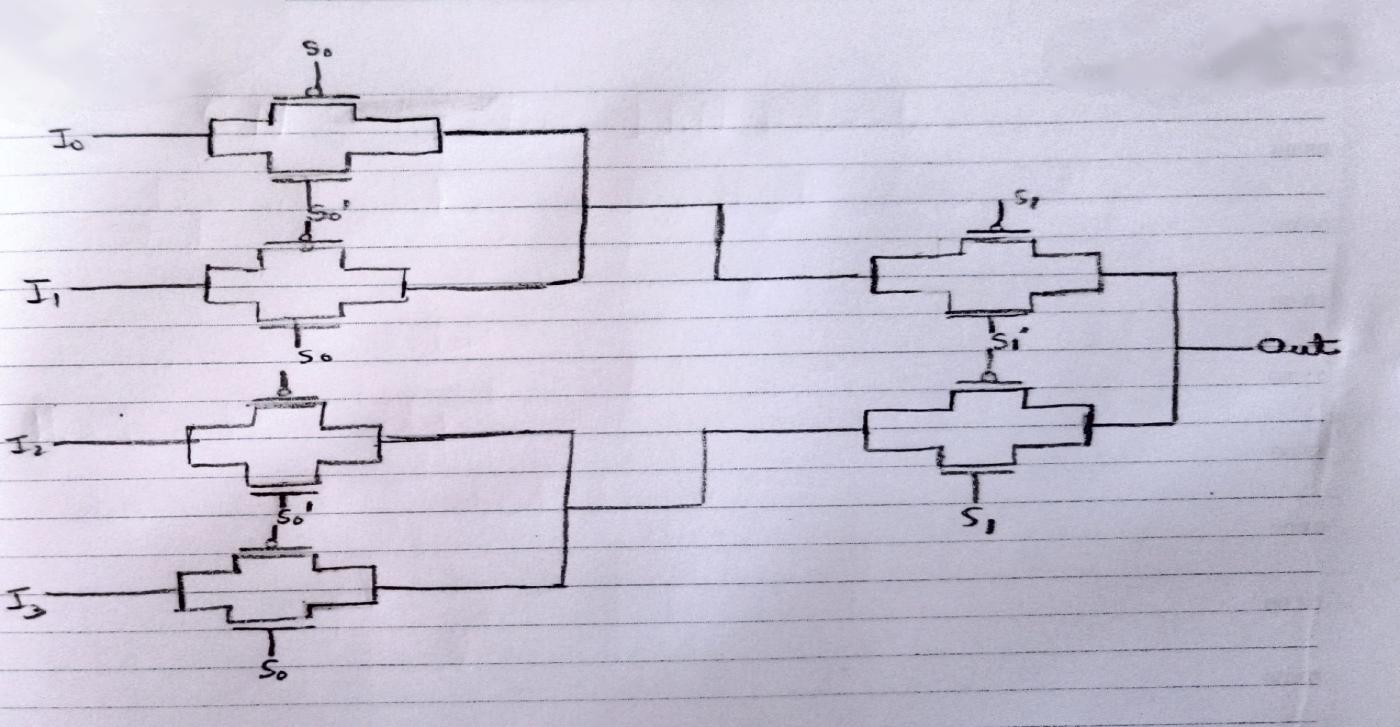
Y = I0S0‘S1’+ I1S0S1‘ + I2S0’S1 + I3S0S1

CMOS Implementation



Y = S1 ( I0S0‘ + I1S0 ) + S1(I2S0‘ + I3S0)

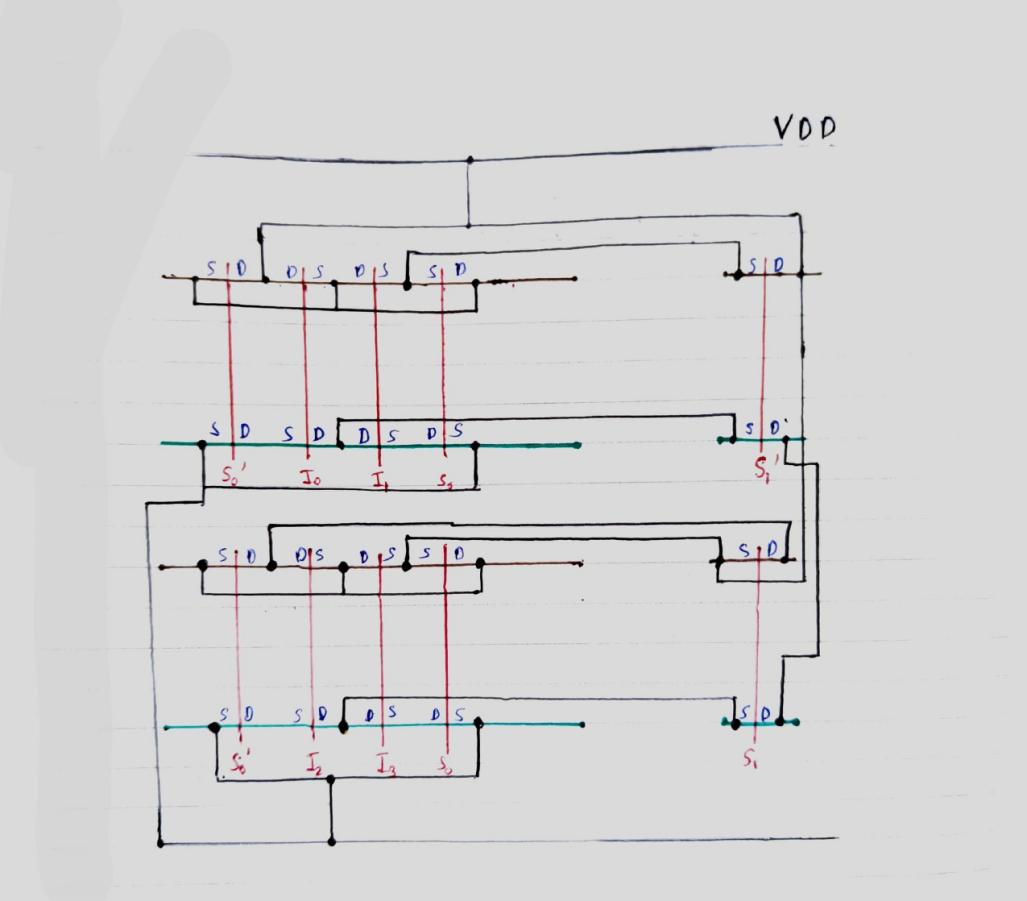
CMOS Implementation



Pass Gate Implementation

3.4) Draw stick diagram for above implementation level using proper color code.

Ans.



3.5) State the various level of VOL corresponding to various transistor statuses considering non CMOS implantation.

Ans: In this circuit various values of VOL is not possible as only one of the path would be enable i.e. only one line would be enabled at any instance.

3.6) Find an equivalent CMOS inverter circuit.

Ans. For the optimized CMOS circuit thee equivalent W/L of PMOS net be W/L. Also the W/L for NMOS net the equivalent W/L would be the same.

3.7) For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value of that resistance?

Ans. At any instance only one path would be on for getting the output low. In a multiplexer the input line I needs to be low for the output to be low hence NMOS would be on whereas PMOS would be off. There are 3 transistors in series for the NMOS circuit as only one of the path would be on at any instance. Therefore the equivalent resistance would be

Req = R + R + R

Given, R=20K ohm

Therefore, Req = 20 + 20 + 20 = 60K ohm

3.8) For CMOS/MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the value of that resistance?

Ans. Ans. At any instance only one path would be on for getting the output high. In a multiplexer the input line I needs to be low for the output to be low hence PMOS would be on whereas NMOS would be off. There are 3 transistors in parallel for the PMOS circuit as only one of the path would be on at any instance. Therefore the equivalent resistance would be

1/Req = 1/R + 1/R + 1/R

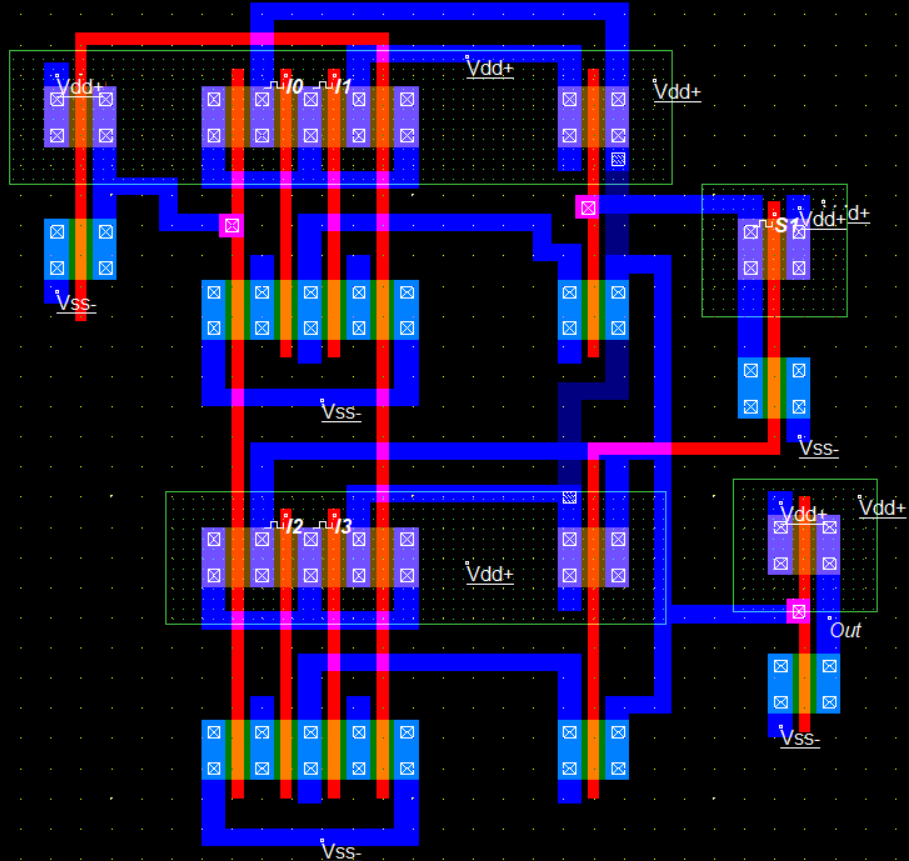
Given, R=20K ohm

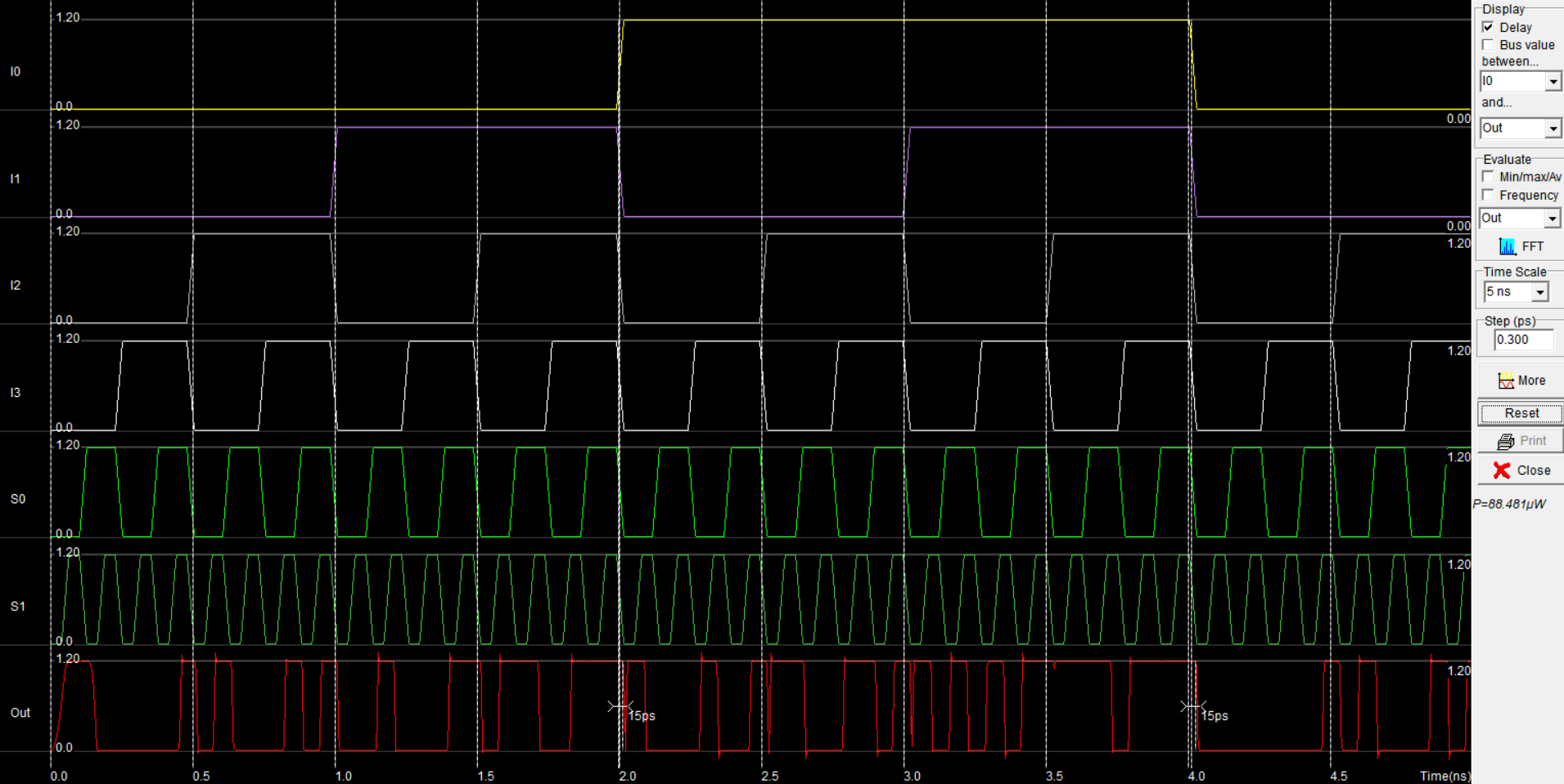
Therefore, 1/Req = 1/20 + 1/20 + 1/20

Req = 20/3 = 6.6667K ohm

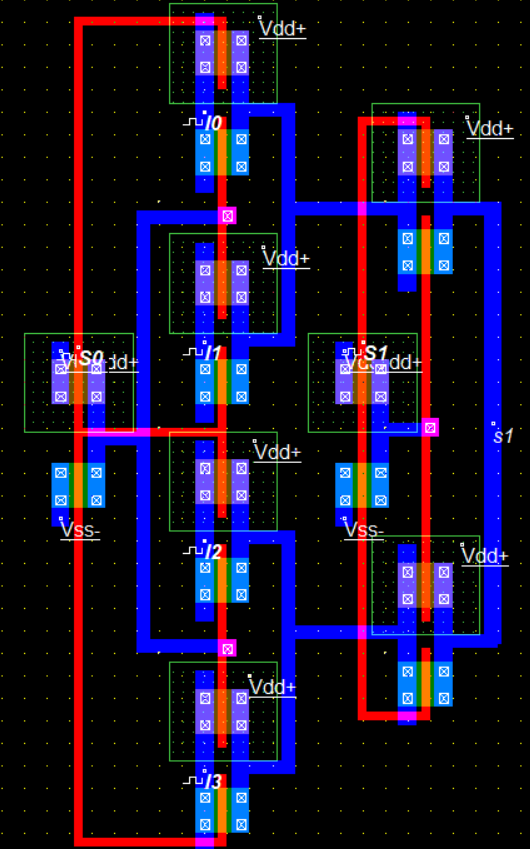
3.9) Prepare a detailed report with proper plots and theory including the answers of the above given questions. Also include the concluding remarks.

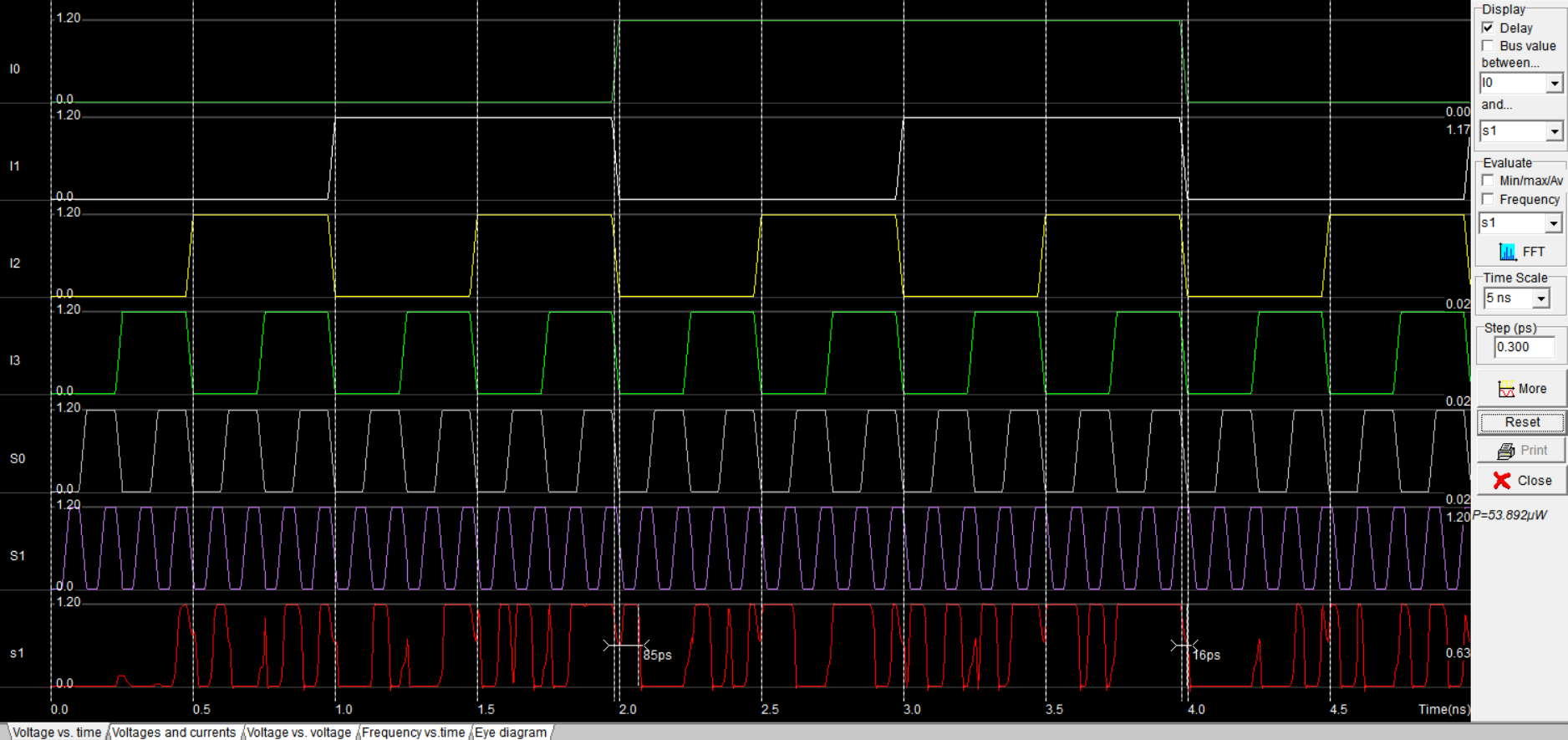
Ans. The following is the CMOS implementation for 4x1 MUX followed by the simulation results.





The following is the transmission gate implementation of 4x1 MUX followed by the simulation results.





1. **Conclusion**

The power of the transmission gate implementation is 53.892μW whereas the power of CMOS implementation is 88.481μW. Also transmission gate implementation requires only 16 transistors whereas the CMOS implementation requires 26 transistors. Hence the area of the transmission gate implementation would be lesser and more optimized. This aspects would result to higher noise. The delay of CMOS implementation is lesser than the delay of transmission gate implementation.

**From above observations, it can be observed that MUX using transmission gate implementation gives better output upon comparison of output among CMOS implementation.**

**\*\*END\*\***