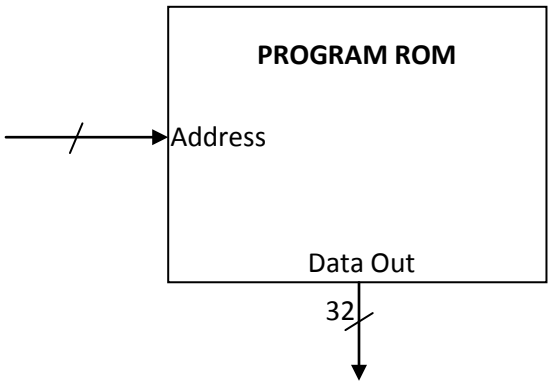
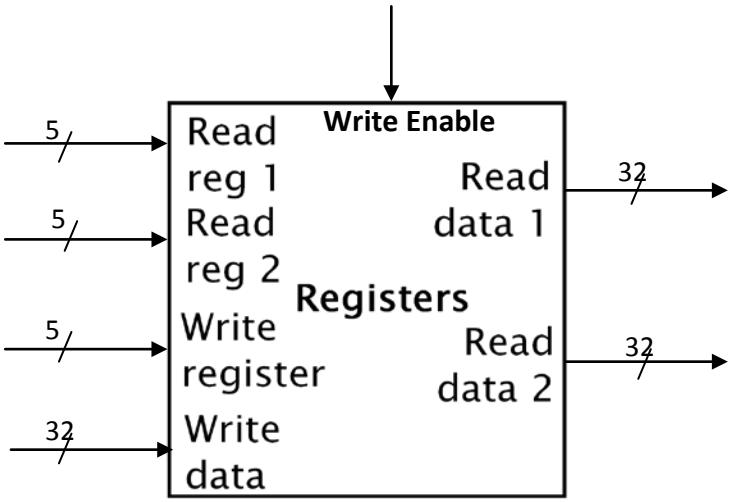
CSE 331 Computer Organization MIPS Processor Design
Project 3: PROGRAM ROM & REGISTER DESIGN
Due Date: 23:59 December 6 (Friday), 2013 (Later submissions will not be accepted)

In this Project you will design two memory elements that will be used in MIPS CPU design:

1. **Program Memory:** It will be a memory which will store the instructions. Fort hat it requires an address input and a data output. The memory size will be 512 MB and the data output will be 32 bits wide as each instruction is 32 bits wide. The figure is shown below. Compute the width of the address input by yourself.



2. **Register:** A register block that contains 32 registers each of which is 32-bits as used in MIPS datapath. It will be able to read two different registers and it will be able to write to a register at the same time.



RULES:

1. Submit a single zip file to Moodle containing all of your Xilinx ALU project files such that your TA could be able to open your project and simulate in Xilinx ISE.

2. Name your zip file as "YourID_Name_Surname_Project3.zip" otherwise you will lose 5 points.

3. You not onlyperform the design but also have to simulate it with Xilinx ISE. The simulation files should also be included in the zip file of course.

4. You will put a txt file named "FunctionalReport.txt" into the zip file, in which you explain which functions work accurately and which ones wrongly or even do not work. Your TA will check your design and if the txt file and the simulation of TA matches with each other, you will get extra 10 points otherwise if the information you gave does not match with the reality you get -15 points.

5. Comment your Verilog files clearly (You may comment in Turkish). Otherwise you will lose 30 pts.

6. You will not get much partial credits. Submit fully working simulating designs for credit.