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Programmable interrupt controller

In computing, a **programmable interrupt controller** (**PIC**) is a device that is used to combine several sources of interrupt onto one or more CPU lines, while allowing priority levels to be assigned to its interrupt outputs. When the device has multiple interrupt outputs to assert, it asserts them in the order of their relative priority. Common modes of a PIC include hard priorities, rotating priorities, and cascading priorities. PICs often allow the cascading of their outputs to inputs between each other.

Contents

Common features

PICs typically have a common set of registers: Interrupt Request Register (IRR), In-Service Register (ISR), Interrupt Mask Register (IMR). The IRR specifies which interrupts are pending acknowledgement, and is typically a symbolic register which can not be directly accessed. The ISR register specifies which interrupts have been acknowledged, but are still waiting for an End Of Interrupt (EOI). The IMR specifies which interrupts are to be ignored and not acknowledged. A simple register schema such as this allows up to two distinct interrupt requests to be outstanding at one time, one waiting for acknowledgement, and one waiting for EOI.

There are a number of common priority schemas in PICs including hard priorities, specific priorities, and rotating priorities.

Interrupts may be either edge triggered or level triggered.

There are a number of common ways of acknowledging an interrupt has completed when an EOI is issued. These include specifying which interrupt completed, using an implied interrupt which has completed (usually the highest priority pending in the ISR), and treating interrupt acknowledgement as the EOI.

Well-known types

One of the best known PICs, the 8259A, was included in the x86 PC. In modern times, this is not included as a separate

chip in an x86 PC, but rather as part of the motherboard's southbridge chipset. In other cases, it has been replaced by the newer Advanced Programmable Interrupt Controllers which support more interrupt outputs and more flexible priority schemas.

See also

- Intel 8259
- Advanced Programmable Interrupt Controller (APIC)
- OpenPIC and IBM MPIC
- Inter-processor interrupt (IPI)
- Interrupt
- Interrupt handler
- Interrupt request (IRQ)
- Interrupt latency
- Non-maskable interrupt (NMI)

Further reading

More information on the Intel APIC can be found in the *IA-32 Intel Architecture Software Developer's Manual, Volume 3A: System Programming Guide, Part 1, Chapter 10*, freely available on the Intel website.

External links

- IA-32 Intel Architecture Software Developer's Manual, Volume 3A (http://www.intel.com/Assets/PDF/manual/253668.pdf)
- Interrupt controller and associated registers. (http://www.fullchipdesign.com/tyh/interrupt_controller_vic.htm)