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Bus mastering

In computing, **bus mastering** is a feature supported by many bus architectures that enables a device connected to the bus to initiate direct memory access (DMA) transactions. It is also referred to as **first-party DMA**, in contrast with third-party DMA where a system DMA controller actually does the transfer.

Some types of buses allow only one device (typically the CPU, or its proxy) to initiate transactions. Most modern bus architectures, such as PCI, allow multiple devices to bus master because it significantly improves performance for general-purpose operating systems. Some real-time operating systems prohibit peripherals from becoming bus masters, because the scheduler can no longer arbitrate for the bus and hence cannot provide deterministic latency.

While bus mastering theoretically allows one peripheral device to directly communicate with another, in practice almost all peripherals master the bus exclusively to perform DMA to main memory.

If multiple devices are able to master the bus, there needs to be a **bus arbitration** scheme to prevent multiple devices attempting to drive the bus simultaneously. A number of different schemes are used for this; for example SCSI has a fixed priority for each SCSI ID. PCI does not specify the algorithm to use, leaving it up to the implementation to set priorities.

See also

- Master/slave (technology)
- SCSI initiator and target

References

- How Bus Mastering Works (http://www.tweak3d.net/articles/howbusmaster/) - Tweak3D
- What is bus mastering? (https://web.archive.org/web/20120316232747/http://bugclub.org/beginners/hardware/BUSMastering.html)- Brevard User's Group

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