Krishna Ramdeep, Joseph Bess
CS 377P
Homework 1

L1 Cache Miss Rates (%)

	50	100	200	400	800	1200	1600	2000
i-j-k	0.712	12.16	12.83	51.73	49.03	51.2	48.7	49.2
j-i-k	0.424	5.406	6.886	52.16	49.9	48.4	45.5	49.9
j-k-i	0.193	5.454	4.57	45.43	52.1	56.4	52.8	59.6
k-j-i	0.320	5.487	4.072	45.35	52.1	55.8	53.1	59.5
i-k-j	0.309	6.703	7.433	7.346	7.36	6.78	6.73	7.1
k-i-j	0.509	7.530	7.054	6.673	6.57	6.3	6.12	6.3

L2 Cache Miss Rates (%)

	50	100	200	400	800	1200	1600	2000
i-j-k	21.65	1.294	63.92	23.7	43.3	24.2	99.7	55.9
j-i-k	10.43	0.195	8.267	0.85	26.2	3.56	92.7	63.1
j-k-i	0.223	0.071	53.9	6.26	36.4	32.5	99.8	64.3
k-j-i	0.134	0.150	49.5	6.09	37.8	33.1	99.8	65.2
i-k-j	0	0.093	2.362	3.24	3.06	6.2	7.8	9.9
k-i-j	0.102	0.107	22.069	27.34	24.9	10.2	13.04	13.4

Floating Point Instructions

	50	100	200	400	800	1200	1600	2000
i-j-k	125,100	1,000,580	8,004,234	64,024,325	512,074,979	1,729,994,637	4,100,425,513	8,010,103,930
j-i-k	250,007	2,000,038	16,003,572	131,019,098	1,047,961,960	3,530,480,315	8,485,699,477	16,573,786,542
j-k-i	250,087	2,000,963	16,006,092	137,411,481	1,078,098,703	3,529,963,955	8,477,376,470	16,432,601,500
k-j-i	250,965	2,004,192	16,054,262	138,560,255	1,074,064,867	3,543,164,286	8,516,560,690	16,548,529,305
i-k-j	125,031	1,000,077	8,001,444	64,011,521	512,069,783	1,729,942,398	4,098,834,150	8,005,449,372
k-i-j	125,000	1,000,036	8,014,552	64,147,340	512,853,633	1,737,169,454	4,122,122,083	8,044,333,820

Load-Store Instructions

	50	100	200	400	800	1200	1600	2000
i-j-k	128,307	1,010,871	8,041,807	64,164,177	512,646,973	1,729,451,627	4,098,577,413	8,004,023,613
j-i-k	268,088	2,071,088	16,282,096	129,124,156	1,028,490,628	3,466,094,368	8,209,942,116	16,028,031,180
j-k-i	465,892	3,471,694	26,883,302	211,526,944	1,678,097,282	5,647,703,685	13,368,358,357	26,088,047,112
k-j-i	465,894	3,471,694	26,883,302	211,528,226	1,678,097,420	5,647,705,139	13,368,358,889	26,088,052,211
i-k-j	205,785	1,571,489	12,043,487	96,166,903	768,653,877	2,593,461,737	6,146,589,517	12,004,038,915
k-i-j	90,633	1,511,183	12,042,287	96,164,505	768,651,069	2,593,455,117	6,146,584,967	12,004,030,925

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1) For the smallest matrix size, the L1 miss rate is almost constant between the loop variants, but the L2 miss rate is extremely high for i-j-k, a little lower for j-i-k, and near zero for the others.
   Looking at the larger matrix sizes, especially 400x400 and greater, the L1 miss rates for the first 4 loop variations are very high (> 40%), but for the last 2 variations remains under 10%. Look at the L2 miss rates for matrices 800x800 and larger, we easily exceed 20% miss rate (especially for 1600x1600, where we see nearly 100% miss rate for the first 4 loop variants).
   Why is this? Probably the cache size. With smaller matrices, the entire calculation can be stored in L1, causing extremely low miss rates, whereas larger data allocation will fill up this cache and cause high miss rates.

2) Using CLOCK_THREAD_CPUTIME_ID gets us very similar results to CLOCK_REALTIME, probably because we were the only user on the machine at the time and the code was the only major process we were running. Similarly, PAPI real time gets use similar results to PAPI process time. When we compare across the 2 methodologies, we see similar times (although when you go down to the nanosecond level, the differences are large).