Department of Electronics and Electrical Engineering

EE211 : Digital Circuits Laboratory

Experiment No. 5 : Stop Watch

Objective: To design a stop watch with the following specifications.

Specifications: 4 digit display showing seconds, and 1/100 second. E.g. a display of 23.78 will indicate time interval of 23.78 second. One push button switch to go through three states in cycle, viz. RESET, START, and STOP, sequentially.

State 1 (RESET): RESET condition shows display as 00.00, and the stop-watch is ready to start counting.

State 2 (START): The switch when pressed during RESET starts the watch and the display is updated every 1/100 second. The watch keeps counting till the switch is pressed again, and then goes to state 3.

State 3 (STOP): In state 3, counting stops and the display freezes. The watch remains in STOP condition till the switch is pressed once again. Pressing switch during STOP condition RESETs the display and the process repeats from State 1.

Procedure: Design a 4 digit (16 bit) fully synchronous BCD counter, a clock generator of 10 ms period using 555 timer, a debouncing circuit for the push button switch and associated logic circuit. Fully synchronous counters use carry-look-ahead throughout. The 4-bit presettable counters 74160, 74161, 74162, and 74163 can be cascaded to obtain fully synchronous 16 bit counter (clock inputs of all the counters are connected together and given a common clock). Read the datasheet of the counter IC to know how ENP and ENT pins are used to cascade several such counters to make a fully synchronous larger modulus counter. Implement and demonstrate the operation of the circuit. Use BCD to 7-segment decoder IC to drive the 7-segment LED display.

Demonstrate the clock generation circuit and switch debouncing circuit using LTSpice.

Preparation Study:

- Download the datasheet of 74160–74163 counters from website of Texas Instruments, http://www.ti.com/lit/ds/symlink/sn54ls161a-sp.pdf and understand the following parts in the datasheet.

  Page 1: Differences between the four counters. Difference between asynchronous clear and synchronous clear.

  Page 11: Timing diagram explaining counter function, use of $\overline{\text{CLR}}$ and $\overline{\text{LOAD}}$ inputs.

  Page 22: Connections for fully synchronous operation of cascaded counters. You may check the internal diagram on page 4 to understand how carry-look-ahead is generated.
- Download the datasheet of 555 timer from http://www.ti.com/lit/ds/symlink/lm555.pdf , study the schematic diagram on page 3, and understand astable multivibrator configuration on page 10.
- Study why switch debouncing is required and how to design a debouncing circuit given in the application notes at https://training.ti.com/debounce-switch