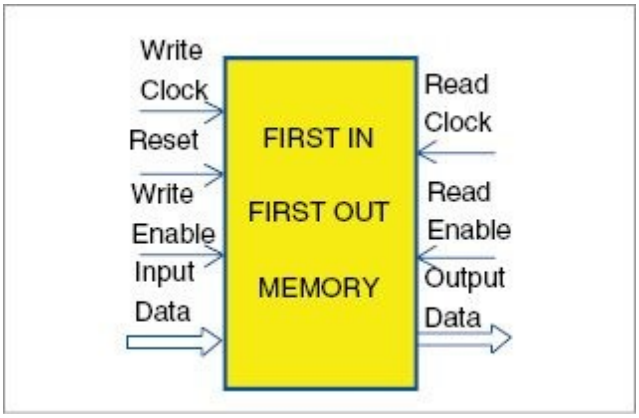
Synchronous FIFO verification

By **Bug Finder** - November 13, 2016



A synchronous First In First Out (commonly referred to as FIFO) or a queue is an array memory. Generally, it is used when the write and read side logic operate at the same clo frequency.

Use Case

- to buffer data when the burst write operation is larger than the burst read operation or vi versa
- read operation is delayed with respect to the write

Interfaces

A FIFO typically has the following set of signals –

- Clock and reset
- Write and Write data
- Read and Read data
- Read and Write enable
- Full and empty (outputs)

Scenarios to verify

FIFO is a commonly used logic in many designs. The major functional features which have to verified are –

- Single write and read operations as well as data correctness
- FIFO transitioning from empty to non-empty and vice versa
- The transition from non-empty to full and vice versa
- Burst read and burst write operations up to the maximum depth
- Empty to full and back to empty

Error conditions

- Write operation when full – The client should wait for the full signal to go low before issui more writes. Otherwise, the data in the FIFO could be overwritten or dropped.
- Read operation when empty – The client should wait for the empty signal to go low befo issuing a read. Otherwise, the data read will be garbage.

Bug Finder

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