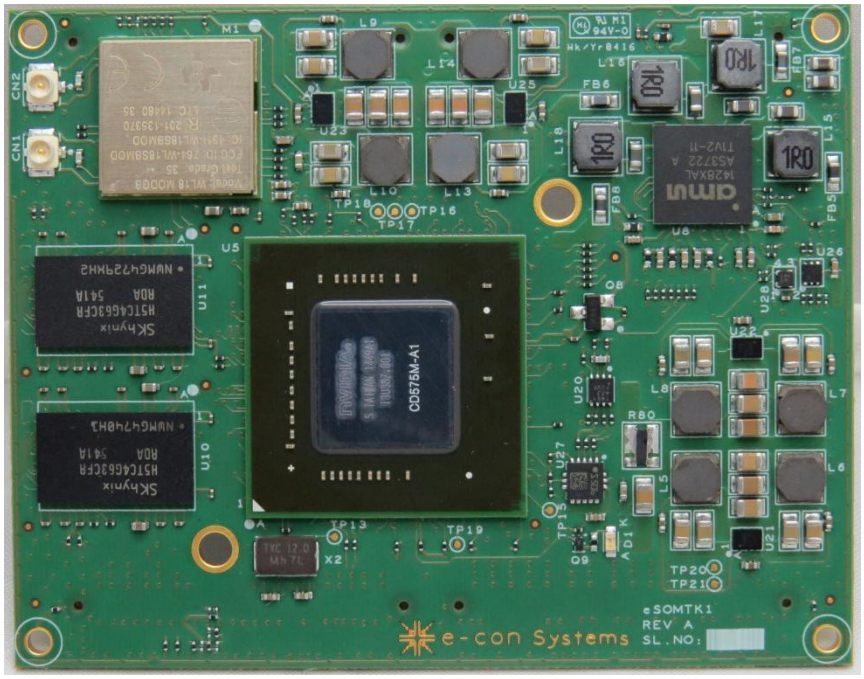
e-con Systems India Pvt Ltd.

eSOMTK1 Datasheet Rev1.7



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1 Introduction

e-con Systems has developed a Computer/System-on-Module eSOMTK1, based on NVIDIA Tegra® K1 CPU with the basic functionality in a compact form factor. The eSOMTK1 has NVIDIA Tegra® K1 CPU running up to 2.2GHz – 4Plus1 Core, DDR3L SDRAM configurable up to 4GB, eMMC configurable up to 32GB. The eSOMTK1 module also has Wireless LAN and Bluetooth module.

As part of the "Productized Services" program of e-con Systems, the eSOMTK1 is aimed at reducing the time-to-market for our customers by making use of the stabilized and ready-to-market eSOMTK1 modules in the customer applications. Being offered in a compact form factored module with various configurations and OS support, these modules will enable our customers to focus on their application design.

This eSOMTK1 is currently powered by Linux and Android. The SOM is targeted to customers to reduce the Time-to-Market, by not worrying about the CPU subsystem, but to focus on the application base board design. This enables customers to build variety of base boards targeting various applications with a host of peripherals and interfaces, but keeping the eSOMTK1 standard which would be the work-horse of the entire product.

The module delivers state of the art technology, targeting low power systems that still require high CPU Performance. It also offers all the interfaces needed in a modern embedded device. Besides the internal Flash Memory, there are several interfaces available for data storage such as SD memory card and SATA.

The CPU board also exposes the complete range of interfaces provided by the Tegra® K1 Processor through its connectors so that the customers can get the complete functionality, without going through the complex design requirements of the processor sub system including memory and power manager.

e-con has a base board "PROPUS" built around eSOMTK1 for evaluation. PROPUS board will be available for customers with complete source code and other design inputs such as schematics, DXF etc. The complete features of eSOMTK1 and a variety of add-on modules supported by e-con are available on our website www.e-consystems.com. Interested customers can also write to sales@e-consystems.com asking for specific details.

Software

e-con provides Linux kernel, with u-boot boot loader for the eSOMTK1. The eSOMTK1 come with pre-installed u-boot. E-con provides Linux kernel and root file system for this eSOMTK1. The source code along with configuration files for eSOMTK1 is provided to the customers.
Please contact e-con Systems for more information about the other Operating Systems supported

2 Ordering Information

Part Number Template: eSOMTK1-Fxxx-Rxx-WB-IM-IT

Feature	Options	P/N Code
CPU	NVIDIA Tegra® K1	TK1
eMMC Density	16GByte	F16G
	32GByte	F32G
	64GByte	F64G
DDR3L Density	2GByte	R2G
	4GByte	R4G
WIFI / BLUETOOTH	Present	WB
	Absent	
IMU	Present	IM
	Absent	
Temperature Grade	Commercial	
	Industrial	IT

3 Block Diagram

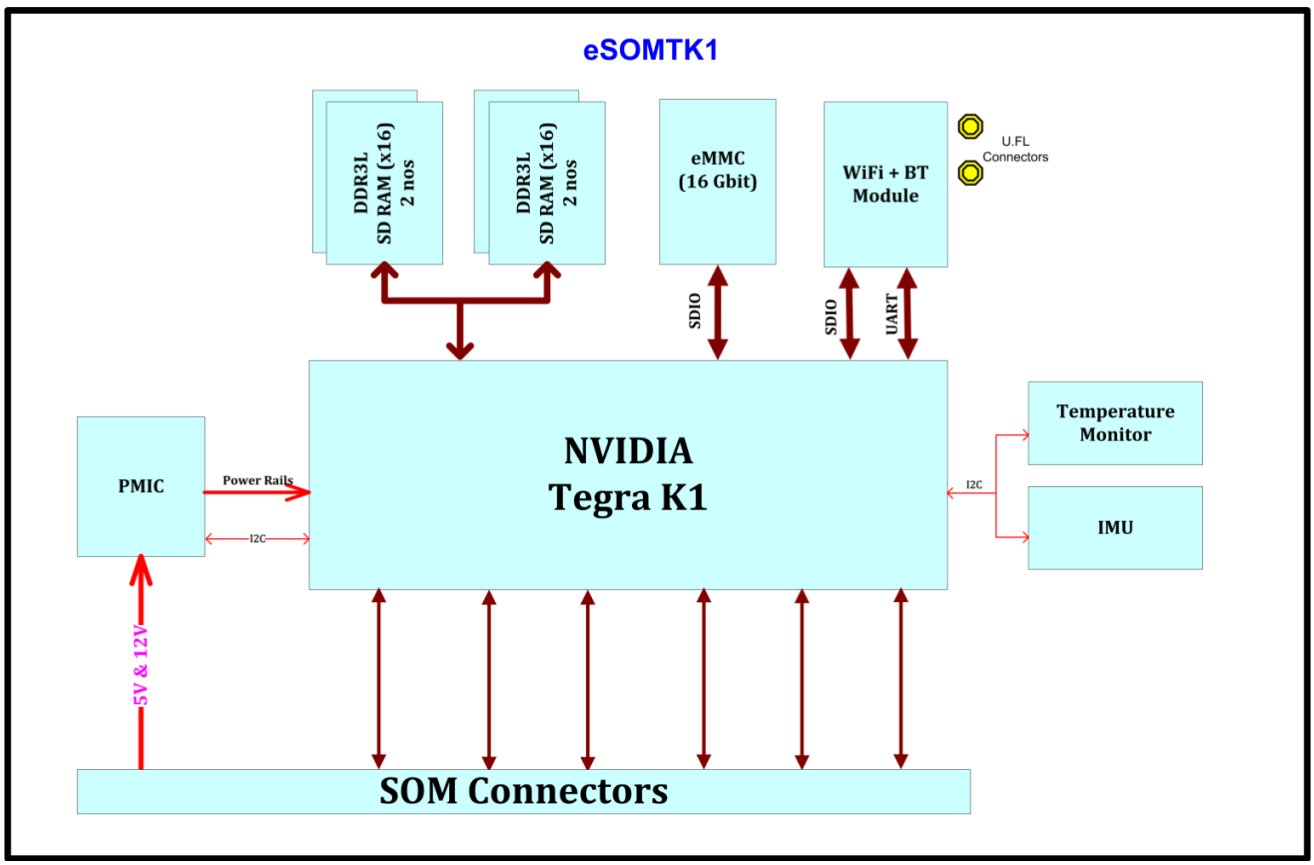


Figure 4-1: Block diagram of eSOMTK1

4 Features Summary

NVIDIA Tegra® K1 CPU

NVIDIA Tegra® K1 4-Plus-1 ARM® Cortex™ -A15 core with NEON Technology processor, capable of operating upto 2.2 GHz and integrated NVIDIA Kepler™ GPU with 192 NVIDIA CUDA® cores.

The Tegra® CPU features
- ARM® Cortex™ A15 MPCore (Quad Core) Processor with NEON Technology
- 2MB L2 cache (16-way) with 40way address banking
- 32KByte I-cache and 32KByte D-cache for each core
- CPU complex on a separate, independently controlled, power rail
- Ultra Low Power (ULP) single core CPU operating mode for low compute workloads (Companion core)

For further information about the features, please refer NVIDIA's Datasheet, User Manual, App notes.

On Board Memory

- **DDR3L SD RAM**
  eSOMTK1 supports a total on-board memory of up to 1/2/4 GB. Tegra® K1 memory controller interfaces up to 64-bits wide and operates upto 792 MHz clock.

- **eMMC – storage**
  eSOMTK1 is available with 16/32/64GB of eMMC memory. This memory can be used for porting OS image, user defined storage.

WIFI + Bluetooth Combo Module

Wi-Fi & Bluetooth connectivity is supported by eSOMTK1.
It can support
- IEEE STD 802.11a, 802.11b, 802.11g, and 802.11n
- Bluetooth 4.1 and CSA2 Support
- Dual-Mode Bluetooth and BLE

There are two on-Board UFL Connectors to which an external Antenna need to be connected.

Inertial Measurement Unit (IMU)

A 3D digital accelerometer and a 3D digital gyroscope (6 axis) is present on eSOMTK1

5 INTERFACES

5.1 BOARD TO BOARD CONNECTOR INTERFACES – 100 X 4 PINS

- PCIe Gen 2.0 (x2)
- SATA II (x1)
- USBOTG 2.0 (x1)
- USB Host 3.0 (x2)
- LVDS / eDP (x1)
- HDMI 1.4b (x1)
- SD/MMC (4-Bit x1, 8-Bit x1)
- I2C (x4)
- SPI (x2)
- PWM (x4)
- SPDIF IN & OUT (x1)
- MIPI-DSI (x1)
- MIPI CSI (x3)
- UART (with CTS & RTS) (x3)
- I2S (x3)
- HSIC (x2)
- GPIOs

5.2 SOM peripherals and their Interface

	Power Domains	Source	Voltage (V)	Interface
eMMC	VCCQ (IO)	PMIC DCDC 5	1.8	SDMMC4
	VCC	PMIC DCDC 3 Through Power switch EN Control is PMIC GPIO1	3.3	
IMU	VDD_IO	PMIC DCDC 5	1.8	GEN1_I2C
	VDD	PMIC DCDC 5	1.8	
WIFI	VIO	PMIC CDCD 5	1.8	WIFI -- SDMMC1 BT-- UART2 BT Audio -- DAP1
	VBAT	PMIC DCDC 3 Through Power switch EN Control is Processor GPIO PBB7	3.3	
LED	Yellow LED	Base Board 5V through MOSFET GPIO Control GPIO_PCC2	5	GPIO_PCC2

GENERAL SPECIFICATIONS

- Power Supply: 12V and 5V Input Voltage
- Form Factor: 70mm x 55mm x 1.6mm (Length X Width X Thickness)

6 Board Connector - Signal termination and Pin Mux

eSOMTK1 has 4 board to board connectors, 100pins each.

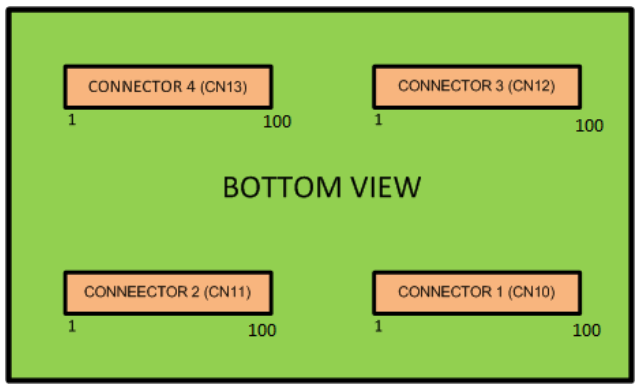
The recommended mating connector for interface is specified below
Manufacturer Part Number: **AXK500147YG**
Manufacturer: **Panasonic**
Mated Height: **3mm**

Tegra® Processor has pins that are multi-purpose digital I/O pads (MPIO). Though each MPIO has upto 5 functions, a given MPIO can act as only a single function at a given point in time.
There are 5 types of MPIO pads, as below

MPIO Pad Type	Input Buffer	Output Buffer	I/O Voltage Tolerance	Nominal Pull Strength
CZ	Schmitt & CMOS	push-pull	VDDIO	15kΩ
DD	Schmitt & CMOS	push-pull & open-drain	3.3V for OD, VDDIO otherwise	50kΩ
LV	Schmitt & CMOS	push-pull	VDDIO	15kΩ
OD	CMOS	open-drain	5V	100kΩ (down only)
ST	Schmitt & CMOS	push-pull	VDDIO	100kΩ

SOM connector pin-out

The below table will have the details of every pin coming out of eSOMTK1.



The following table describes the column heading of the below table.

Item on the Table	Description of the item
Pin Number	Pin number on the 100 pin board to board connector
Pin Name	This represents the signal name in the eSOMTK1 100-pin board to board connector. The signal name is abbreviation of the signal functionality.
Mux Capabilities	Mux options available for the particular pin
Voltage/Pad Type	Functional group of the pin and type of pad
POR	Power On reset state
Wake Capable	Can wake processor from deep sleep state

6.1 CONNECTOR 1

Pin No.	Pin Name	Mux Capabilities					Voltage /Pad Type	WAKE Capable	POR State
1	Ground								
2	Ground								
3	DP_HPD	GPIO3_PFF.00					3.3V,ST		Z
4	DP_AUX_CH0_N			I2C6_DAT					
5	VCC_3P3_LS_1								
6	DP_AUX_CH0_P			I2C6_CLK					
7	VCC_1P8_SD5								
8	Ground								
9	Ground								
10	Ground								
11	Ground								
12	GPIO_PK0					SOC_THERM_OC3_N	1.8V,CZ		PU
13	HDMI_TXCN								
14	PM3_PWM2	GPIO_PH2					1.8V,CZ		PD
15	HDMI_TXCP								PD
16	PM3_PWM1	GPIO_PH1					1.8V,CZ		PD
17	Ground								
18	GPIO_PJ2					SOC_THERM_OC4_N	1.8V,CZ	WAKE15	PU
19	HDMI_TXD0P								
20	GPIO_PI0						1.8V,CZ		
21	HDMI_TXD0N								
22	Ground								
23	Ground								
24	PM3_PWM0	GPIO_PH0		TRACE DATA2		DTV_VALID	1.8V,CZ		PD
25	HDMI_TXD1N								
26	PM3_PWM3	GPIO_PH3					1.8V,CZ		PD
27	HDMI_TXD1P								
28	GPIO_PU5						1.8V,ST	WAKE6	Z
29	Ground								
30	GPIO_PU4						1.8V,ST		Z
31	HDMI_TXD2P								
32	GPIO_PU6						1.8V,ST	WAKE7	Z
33	HDMI_TXD2N								
34	Ground								
35	Ground								

36	GPIO_PG0						1.8V,CZ		Z
37	DDC_SDA	GPIO3_PV.05	I2C4_DAT				3.3V,OD		Z
38	GPIO_PG3		TRACE DATA1				1.8V,CZ		Z
39	HDMI_INT	GPIO3_PN.07					3.3V,OD	WAKE4	PD
40	GPIO_PG2		TRACE DATA0				1.8V,CZ		Z
41	DDC_SCL	GPIO3_PV.04	I2C4_CLK				3.3V,OD		Z
42	GPIO_PG1						1.8V,CZ		Z
43	HDMI_CEC	GPIO3_PEE.03					3.3V,DD	WAKE52	Z
44	Ground								
45	Ground								
46	SDMMC2A_CLK	GPIO_PK1		TRACE CLK			1.8V,CZ		PD
47	CLK3_OUT	GPIO3_PEE.00	EXTPERIPH3_CLK				1.8V,ST		Z
48	SDMMC2A_DAT2	GPIO_PH5					1.8V,CZ		PD
49	CLK3_REQ	GPIO3_PEE.01					1.8V,ST		Z
50	SDMMC2A_DAT1	GPIO_PI5					1.8V,CZ	WAKE23	PU
51	CLK2_REQ	GPIO3_PCC.05					1.8V,ST		Z
52	SDMMC2A_DAT3	GPIO_PH6	TRACE DATA3		DTV_DATA		1.8V,CZ		PU
53	CLK2_OUT	GPIO3_PW.05	EXTPERIPH2_CLK				1.8V,ST		PD
54	SDMMC2A_DAT5	GPIO_PK4					1.8V,CZ		PU
55	Ground								
56	Ground								
57	SPI4C_SCK	GPIO_PG5					1.8V,CZ	WAKE 0	Z
58	SDMMC2A_DAT4	GPIO_PK3		TRACE CTL			1.8V,CZ		PU
59	SPI4C_CS3	GPIO_PG4					1.8V,CZ		Z
60	SDMMC2A_CMD	GPIO_PH7	TRACE DATA4		DTV_CLK		1.8V,CZ		PU
61	SPI4C_DIN	GPIO_PG7					1.8V,CZ		Z
62	SDMMC2A_DAT6	GPIO_PI2		TRACE DATA5			1.8V,CZ		PU
63	SPI4C_DOUT	GPIO_PG6					1.8V,CZ		Z
64	SDMMC2A_DAT7	GPIO_PI6					1.8V,CZ	WAKE35	PU
65	SPI4C_CS1	GPIO_PI4		TRACE DATA6			1.8V,CZ	WAKE32	PD
66	SDMMC2A_DAT0	GPIO_PH4					1.8V,CZ		PU
67	SPI4C_CS0	GPIO_PI3					1.8V,CZ		PU
68	Ground								
69	Ground								

70	UART3_CTS_N	GPIO3_PA.01					1.8V,ST	WAKE55	PU
71	UD3_RTS	GPIO_PK7					1.8V,CZ		Z
72	UART3_RTS_N	GPIO3_PC.00					1.8V,ST		PU
73	UD3_CTS	GPIO_PB1					1.8V,CZ		Z
74	UART3_RXD	GPIO3_PW.07					1.8V,ST		PU
75	UD3_TXD	GPIO_PJ7					1.8V,CZ		Z
76	UART3_TXD	GPIO3_PW.06					1.8V,ST		PU
77	UD3_RXD	GPIO_PB0					1.8V,CZ		Z
78	Ground								
79	Ground								
80	SDMMC3_CD_N	GPIO3_PV.02					1.8V,ST	WAKE56	PU
81	UA3_RXD	GPIO_PU1					1.8V,ST		PD
82	SDMMC3_DAT3	GPIO3_PB.04					3.3V,CZ		PU
83	UA3_TXD	GPIO_PU0					1.8V,ST		PD
84	SDMMC3_DAT0	GPIO3_PB.07					3.3V,CZ		PU
85	UA3_RTS	GPIO_PU3					1.8V,ST		Z
86	SDMMC3_DAT1	GPIO3_PB.06					3.3V,CZ	WAKE3	PU
87	UA3_CTS	GPIO_PU2					1.8V,ST		Z
88	SDMMC3_DAT2	GPIO3_PB.05					3.3V,CZ		PU
89	Ground								
90	SDMMC3_CMD	GPIO3_PA.07					3.3V,CZ		PU
91	DAP4_SCLK	GPIO3_PP.07					1.8V,ST		PD
92	SDMMC3_CLK	GPIO3_PA.06					3.3V,CZ		PD
93	DAP4_FS	GPIO3_PP.04					1.8V,ST		PD
94	Ground								
95	DAP4_DIN	GPIO3_PP.05					1.8V,ST		PD
96	SDMMC3_CLK_LB_IN	GPIO3_PEE.05					3.3V,CZ		PD
97	DAP4_DOUT	GPIO3_PP.06					1.8V,ST		PD
98	SDMMC3_CLK_LB_OUT	GPIO3_PEE.04					3.3V,CZ		Z
99	Ground								
100	Ground								

6.2 CONNECTOR 2

Pin No	Pin Name	Mux Capabilities					Voltage /Pad Type	WAKE Capable	POR State
1	Ground								
2	Ground								
3	DSI_A_CLK_N								
4	Ground								
5	DSI_A_CLK_P								
6	VCC_3P3_LDO2								
7	Ground								
8	VCC_LDO6								
9	DSI_A_D2_P								
10	VCC_LDO10								
11	DSI_A_D2_N								
12	Ground								
13	Ground								
14	CAM_MCLK	GPIO3_PCC.00			vimclk_alt3		1.8V,ST		PU
15	DSI_A_D3_N								
16	Ground								
17	DSI_A_D3_P								
18	GPIO_PCC1						1.8V,ST		PU
19	Ground								
20	GPIO_PBB0	GPIO3_PBB.00				vimclk2_alt3	1.8V,ST		PD
21	DSI_A_D0_N								
22	Ground								
23	DSI_A_D0_P								
24	Ground								
25	Ground								
26	DSI_B_D0_P								
27	DSI_A_D1_P								
28	DSI_B_D0_N								
29	DSI_A_D1_N								
30	Ground								
31	Ground								
32	DSI_B_CLK_N								
33	Ground								
34	DSI_B_CLK_P								
35	CAM_I2C_SCL	GPIO3_PBB.01					1.8V,DD	WAKE53	Z
36	Ground								

37	CAM_I2C_SDA	GPIO3_PBB.02					1.8V,DD	WAKE48	Z
38	DSI_B_D2_P								
39	Ground								
40	DSI_B_D2_N								
41	Ground								
42	Ground								
43	CSI_A_D0_P								
44	DSI_B_D1_N								
45	CSI_A_D0_N								
46	DSI_B_D1_P								
47	Ground								
48	Ground								
49	CSI_A_CLK_N								
50	DSI_B_D3_P								
51	CSI_A_CLK_P								
52	DSI_B_D3_N								
53	Ground								
54	Ground								
55	CSI_A_D1_N								
56	Ground								
57	CSI_A_D1_P								
58	CSI_B_D0_P								
59	Ground								
60	CSI_B_D0_N								
61	CSI_E_D0_P								
62	Ground								
63	CSI_E_D0_N								
64	CSI_B_D1_N								
65	Ground								
66	CSI_B_D1_P								
67	CSI_E_CLK_N								
68	Ground								
69	CSI_E_CLK_P								
70	Ground								
71	Ground								
72	LVDS0_TXD2P								
73	Ground								
74	LVDS0_TXD2N								
75	Ground								
76	Ground								

77	SPDIF_IN	GPIO3_PK.06					3.3V,ST	WAKE57	PD
78	LVDS0_TXD1P								
79	SPDIF_OUT	GPIO3_PK.05					3.3V,ST		PU
80	LVDS0_TXD1N								
81	Ground								
82	Ground								
83	GPIO_PI1						1.8V,CZ		PU
84	LVDS0_TXD0N								
85	OWR								Z
86	LVDS0_TXD0P								
87	USB_VBUS_EN1	GPIO3_PN.05					3.3V,DD		0
88	Ground								
89	USB_VBUS_EN0	GPIO3_PN.04					3.3V,DD		0
90	LVDS0_TXD3N								
91	Ground								
92	LVDS0_TXD3P								
93	GEN2_I2C_SCL	GPIO3_PT.05					1.8V,DD		Z
94	Ground								
95	GEN2_I2C_SDA	GPIO3_PT.06					1.8V,DD	WAKE47	Z
96	LVDS0_TXD4N								
97	Ground								
98	LVDS0_TXD4P								
99	Ground								
100	Ground								

6.3 CONNECTOR 3

Pin No	Pin Name	Mux Capabilities					Voltage /Pad Type	WAKE Capable	POR State
1	Ground								
2	USB_VBUS_EN2	GPIO3_PFF.01					3.3V,DD		0
3	PEX_RX3N								
4	GPIO_PFF2		SATA_DA				3.3V,DD	WAKE59	Z
5	PEX_RX3P								
6	USB0_VBUS								
7	Ground								
8	Ground								
9	PEX_TX3N								

10	KB_COL0	GPIO3_PQ.00					1.8,ST	WAKE51	PU
11	PEX_TX3P								
12	KB_COL3	GPIO3_PQ.03					1.8V,ST		PU
13	Ground								
14	KB_COL4	GPIO3_PQ.04			SDMMC3_WP_N		1.8V,ST		PU
15	PEX_REFCLKN								
16	KB_COL6	GPIO3_PQ.06					1.8V,ST		PU
17	PEX_REFCLKP								
18	KB_COL2	GPIO3_PQ.02					1.8V,ST		PU
19	Ground								
20	KB_COL7	GPIO3_PQ.07					1.8V,ST		PU
21	Ground								
22	KB_COL1	GPIO3_PQ.01					1.8V,ST		PU
23	PEX_CLK2P								
24	KB_COL5	GPIO3_PQ.05					1.8V,ST	WAKE54	PU
25	PEX_CLK2N								
26	Ground								
27	Ground								
28	SATA_L0_TXN								
29	PEX_L1_CLKREQ_N	GPIO3_PDD.06					3.3V,ST		Z
30	SATA_L0_TXP								
31	PEX_L0_CLKREQ_N	GPIO3_PDD.02					3.3V,ST		Z
32	Ground								
33	PEX_WAKE_N	GPIO3_PDD.03					3.3V,ST	WAKE14	Z
34	SATA_L0_RXP								
35	PEX_L1_RST_N	GPIO3_PDD.05					3.3V,ST		Z
36	SATA_L0_RXN								
37	PEX_L0_RST_N	GPIO3_PDD.01					3.3V,ST		Z
38	Ground								
39	Ground								
40	SATA_TESTCLKP								
41	Ground								
42	SATA_TESTCLKN								
43	EN5V						2.5V		
44	Ground								
45	AC_OK						5V (max.)		
46	RESET_OUT_N								
47	Ground								

48	Ground								
49	GPIO_PV1						1.8V,ST	WAKE 1	Z
50	DAP3_DOUT	GPIO3_PP.02					1.8V,ST		PD
51	GPIO_PV0						1.8V,ST	WAKE24	Z
52	DAP3_DIN	GPIO3_PP.01					1.8V,ST		PD
53	Ground								
54	DAP3_FS	GPIO3_PP.00					1.8V,ST		PD
55	HSIC1_DATA								
56	DAP3_SCLK	GPIO3_PP.03					1.8V,ST		PD
57	HSIC1_STROBE								
58	Ground								
59	Ground								
60	Ground								
61	HSIC2_STROBE								
62	GPIO_X5_AUD	GPIO3_PX.05					1.8V,ST		PU
63	HSIC2_DATA								
64	GPIO_X1_AUD	GPIO3_PX.01					1.8V,ST		PD
65	Ground								
66	GPIO_X6_AUD	GPIO3_PX.06					1.8V,ST		PD
67	DAP2_SCLK	GPIO3_PA.03					1.8V,ST		PD
68	Ground								
69	DAP2_FS	GPIO3_PA.02					1.8V,ST		PD
70	Ground								
71	DAP2_DOUT	GPIO3_PA.05					1.8V,ST		PD
72	DAP_MCLK1	GPIO3_PW.04	EXTPERIPH1_CLK				1.8V,ST		PD
73	DAP2_DIN	GPIO3_PA.04					1.8V,ST		PD
74	GPIO_W2_AUD	GPIO3_PW.02					1.8V,ST	WAKE12	PU
75	Ground								
76	GPIO_X3_AUD	GPIO3_PX.03					1.8V,ST		PU
77	KB_ROW2	GPIO3_PS.02				UA3_RXD	1.8V,ST		PD
78	GPIO_W3_AUD	GPIO3_PW.03					1.8V,ST	WAKE11	PU
79	KB_ROW13	GPIO3_PR.05					1.8V,ST	WAKE26	PD
80	DAP_MCLK1_REQ	GPIO3_PEE.02			SATA_DEV_SLP		1.8V,ST		PD
81	Ground								
82	Ground								
83	KB_ROW17	GPIO3_PT.01					1.8V,ST		PD
84	KB_ROW3	GPIO3_PR.03			SYS_CLK_REQ		1.8V,ST		1
85	KB_ROW10	GPIO3_PS.02		UA3_RXD			1.8V,ST	WAKE9	PD
86	KB_ROW14	GPIO3_PS.06					1.8V,ST	WAKE28	PD

87	KB_ROW9	GPIO3_PS.01		UA3_TXD			1.8V,ST		PD
88	KB_ROW7	GPIO3_PR.07					1.8V,ST	WAKE49	PD
89	KB_ROW6	GPIO3_PR.06			DCA_LSPII		1.8V,ST		PD
90	KB_ROW5	GPIO3_PR.05					1.8V,ST		PD
91	KB_ROW16	GPIO3_PT.00					1.8V,ST		PD
92	KB_ROW12	GPIO3_PS.04					1.8V,ST	WAKE25	PD
93	KB_ROW0	GPIO3_PR.00					1.8V,ST		PD
94	KB_ROW11	GPIO3_PS.03					1.8V,ST		PD
95	KB_ROW8	GPIO3_PS.00					1.8V,ST	WAKE27	PD
96	KB_ROW1	GPIO3_PR.01					1.8V,ST		PD
97	KB_ROW4	GPIO3_PR.04					1.8V,ST	WAKE50	PD
98	KB_ROW15	GPIO3_PS.07			soc_therm_oc1_n		1.8V,ST	WAKE29	PD
99	Ground								
100	Ground								

6.4 CONNECTOR 4

Pin No.	Pin Name	Mux Capabilities					Voltage /Pad Type	WAKE Capable	POR State
1	VCC_5								
2	VCC_12								
3	VCC_5								
4	VCC_12								
5	VCC_5								
6	VCC_12								
7	VCC_5								
8	VCC_12								
9	VCC_5								
10	VCC_12								
11	VCC_5								
12	VCC_12								
13	VCC_5								
14	VCC_12								
15	VCC_5								
16	VCC_12								
17	Ground								
18	VCC_12								
19	Ground								
20	VCC_12								
21	Ground								

22	VCC_12								
23	Ground								
24	VCC_12								
25	VCC_LDO9								
26	Ground								
27	Ground								
28	Ground								
29	LID						5V (max.)		
30	Ground								
31	GPIO6_PMIC						5V/1.8V		
32	Ground								
33	GPIO4_PMIC						5V/1.8V		
34	VBAT_BKUP						2.5V-3.6V		
35	GPIO5_PMIC						5V/1.8V		
36	VCC_2P5						2.5V		
37	Ground								
38	XRES_IN								
39	Ground								
40	Ground								
41	PWM_CLK2_ADC1						5V (max.)		
42	Ground								
43	PWM_DAT2_ADC2						5V (max.)		
44	USB2_DP								
45	Ground								
46	USB2_DN								
47	ONKEY						2.5V		
48	Ground								
49	USB0_ID								
50	USB1_DN								
51	Ground								
52	USB1_DP								
53	SPI1A_SCK	GPIO3_PY.02	ULPI_NXT				1.8V,ST		Z
54	Ground								
55	GPIO3_PO.04		ULPI_DATA3				1.8V,ST		PU
56	USB0_DN								
57	GPIO3_PO.01		ULPI_DATA0				1.8V,ST		PU
58	USB0_DP								
59	GPIO3_PO.02		ULPI_DATA1				1.8V,ST		PU
60	Ground								
61	Ground								

62	Ground								
63	GPIO3_PO.06		ULPI_DATA5				1.8V,ST		PU
64	USB3_RX0P								
65	GPIO3_PO.03		ULPI_DATA2				1.8V,ST		PU
66	USB3_RX0N								
67	SPI1A_CS0	GPIO3_PY.03	ULPI_STP				1.8V,ST		Z
68	Ground								
69	GPIO3_PO.00		ULPI_DATA7				1.8V,ST		PU
70	USB3_TX0P								
71	Ground								
72	USB3_TX0N								
73	GPIO3_PO.07		ULPI_DATA6				1.8V,ST		PU
74	Ground								
75	SPI1A_DIN	GPIO3_PY.01	ULPI_DIR				1.8V,ST		Z
76	Ground								
77	GPIO3_PO.05		ULPI_DATA4				1.8V,ST		PU
78	PEX_USB3_TX1N								
79	SPI1A_DOUT	GPIO3_PY.00	ULPI_CLK				1.8V,ST		Z
80	PEX_USB3_TX1P								
81	Ground								
82	Ground								
83	PEX_CLK1N								
84	PEX_USB3_RX1N								
85	PEX_CLK1P								
86	PEX_USB3_RX1P								
87	Ground								
88	Ground								
89	PEX_RX4P								
90	PEX_TX2N								
91	PEX_RX4N								
92	PEX_TX2P								
93	Ground								
94	Ground								
95	PEX_TX4P								
96	PEX_RX2N								
97	PEX_TX4N								
98	PEX_RX2P								
99	Ground								
100	Ground								

7 Peripheral interfaces

This chapter discuss in detail the various interfaces terminated in the four 100pin connectors by referring to the default pin names. However, additional interfaces are available when different mux options are selected. The following section explains the notation used in the tables below.

Item on the Table	Description of the item
Pin Number	Pin number on the 100 pin board to board connector
Pin Name	This item represents the Signal Name of the eSOMTK1 100 pin connector. The Signal Name is abbreviation of the signal functionality.
Connector Number	Connector in which the pin is terminated
Description	Pin functionality description

7.1 Display Subsystem

The eSOMTK1 supports the following display interfaces

- Two MIPI/DSI ports
- One HDMI port (ver. 1.4b)
- 1 LVDS/eDP channel

7.1.1 MIPI DSI

Tegra® K1 MIPI DSI interface is compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.0.1. Tegra® K1 has two MIPI DSI controllers - A and B. Controller B can also be used as MIPI CSI interface in case an additional CSI interface is desired. Please refer the TRM for more information.
The DSI interface supports up to 1x4 or 2x4 D-PHY Data Lanes. Max. Video Mode resolution is 16:9 aspect ratio upto and including 3200x2000 at 60fps, 24bpp

DSI A

Connector No	Pin Number	Pin Name	Description
2	3	DSI_A_CLK_N	Output Clock Negative for interface A
	5	DSI_A_CLK_P	Output Clock Positive for interface A
	21	DSI_A_D0_N	Data Lane 0 Negative
	23	DSI_A_D0_P	Data Lane 0 Positive
	29	DSI_A_D1_N	Data Lane 1 Negative
	27	DSI_A_D1_P	Data Lane 1 Positive
	11	DSI_A_D2_N	Data Lane 2 Negative
	9	DSI_A_D2_P	Data Lane 2 Positive
	15	DSI_A_D3_N	Data Lane 3 Negative
	17	DSI_A_D3_P	Data Lane 3 Positive

DSI B

Connector No.	Pin Number	Pin Name	Description
2	32	DSI_B_CLK_N	Output Clock Negative for interface B
	34	DSI_B_CLK_P	Output Clock Positive for interface B
	28	DSI_B_D0_N	Data Lane 0 Negative
	26	DSI_B_D0_P	Data Lane 0 Positive
	44	DSI_B_D1_N	Data Lane 1 Negative
	46	DSI_B_D1_P	Data Lane 1 Positive
	40	DSI_B_D2_N	Data Lane 2 Negative
	38	DSI_B_D2_P	Data Lane 2 Positive
	52	DSI_B_D3_N	Data Lane 3 Negative
	50	DSI_B_D3_P	Data Lane 3 Positive

7.1.2 HDMI

The High Definition Multimedia Interface (HDMI) is a wired digital interconnect that replaces the analog TV out or VGA out. The HDMI module provides an HDMI standard interface port to an HDMI 1.4b compliant display.

Connector No.	Pin Number	Pin Name	Description
1	43	HDMI_CEC	Consumer Electronics Control (CEC) one-wire serial bus
	41	DDC_SCL	Serial Clock, this pin is 5V tolerant
	37	DDC_SDA	Serial Data, this pin is 5V tolerant
	39	HDMI_INT	Interrupt. Used for Hot Plug detection
	13	HDMI_TXCN	Transmit Clock Negative
	15	HDMI_TXCP	Transmit Clock Positive
	21	HDMI_TXD0N	Data Lane 0 Negative
	19	HDMI_TXD0P	Data Lane 0 Positive
	25	HDMI_TXD1N	Data Lane 1 Negative
	27	HDMI_TXD1P	Data Lane 1 Positive
	33	HDMI_TXD2N	Data Lane 2 Negative
	31	HDMI_TXD2P	Data Lane 2 Positive

7.1.3 eDP/LVDS Interface

Connector No.	Pin Number	Pin Name	Description
2	84	LVDS0_TXD0N	Data Lane 0 Negative
	86	LVDS0_TXD0P	Data Lane 0 Positive
	80	LVDS0_TXD1N	Data Lane 1 Negative
	78	LVDS0_TXD1P	Data Lane 1 Positive
	74	LVDS0_TXD2N	Data Lane 2 Negative
	72	LVDS0_TXD2P	Data Lane 2 Positive
	90	LVDS0_TXD3N	Data Lane 3 Negative
	92	LVDS0_TXD3P	Data Lane 3 Positive
	96	LVDS0_TXD4N	Data Lane 4 Negative
	98	LVDS0_TXD4P	Data Lane 4 Positive
1	3	DP_HPD	Hot Plug detect
	4	DP_AUX_CH0_N	Auxiliary Negative
	6	DP_AUX_CH0_P	Auxiliary Positive

See LVDS/eDP Pin Assignment Options table below for pin assignments for each interface in the table below.

Pin Name	LVDS (3-lane)	LVDS (4 lane)	eDP
LVDS0_TXD0N	LVDS lane 0	LVDS lane 0	eDP lane 2
LVDS0_TXD0P			
LVDS0_TXD1N	LVDS lane 1	LVDS lane 1	eDP lane 1
LVDS0_TXD1P			
LVDS0_TXD2N	LVDS lane 2	LVDS lane 2	eDP lane 0
LVDS0_TXD2P			
LVDS0_TXD3N	N/A	LVDS lane 3	N/A
LVDS0_TXD3P			
LVDS0_TXD4N	LVDS clock lane	LVDS clock lane	eDP lane 3
LVDS0_TXD4P			

7.2 Camera Subsystem

Upto 3 camera inputs that can be connected to Tegra® K1 (any 2 can be active at the same time)

- 1 x4 (single camera with 4 lane sensor)
- 1 x4 + 1 x1 (one high resolution camera and another one lane camera)
- 2 x4 (dual cameras for stereo with 4 lanes for each camera)

Connector No.	Pin Number	Pin Name	Description
2	49	CSI_A_CLK_N	CSI A Clock Negative
	51	CSI_A_CLK_P	CSI A Clock Positive
	45	CSI_A_D0_N	CSI A Data 0 Negative
	43	CSI_A_D0_P	CSI A Data 0 Positive
	55	CSI_A_D1_N	CSI A Data 1 Negative
	57	CSI_A_D1_P	CSI A Data 1 Positive
	60	CSI_B_D0_N	CSI B Data 0 Negative
	58	CSI_B_D0_P	CSI B Data 0 Positive
	64	CSI_B_D1_N	CSI B Data 1 Negative
	66	CSI_B_D1_P	CSI B Data 1 Positive
	67	CSI_E_CLK_N	CSI E Clock Negative
	69	CSI_E_CLK_P	CSI E Clock Positive

7.3 SDMMC

Tegra® K1's SecureDigital (SD)/Embedded MultiMediaCard (eMMC) controller is capable of interfacing to SD/eSD, SDIO cards, and eMMC devices. SD/eMMC controller supports 2 different bus protocols - SD and eMMC bus protocol for eMMC.

It supports the following features

- SD Host Controller Standard Specification Version 4.0
- eMMC Specification version 4.51 including HS200 at 200MHz
- SD Physical Layer Specification Version 4.0
- SDIO Physical Layer Specification Version 4.0 (up to UHS1, not UHS2)
- One 4 bit and another 8bit interfaces are available.

Connector No.	Pin Number	Pin Name	Description
1	46	SDMMC2A_CLK	SD/SDIO/MMC 2A Clock
	60	SDMMC2A_CMD	SD/SDIO/MMC 2A Command
	66	SDMMC2A_DAT0	SD/SDIO/MMC 2A Data 0
	50	SDMMC2A_DAT1	SD/SDIO/MMC 2A Data 1
	48	SDMMC2A_DAT2	SD/SDIO/MMC 2A Data 2
	52	SDMMC2A_DAT3	SD/SDIO/MMC 2A Data 3
	58	SDMMC2A_DAT4	SD/SDIO/MMC 2A Data 4
	54	SDMMC2A_DAT5	SD/SDIO/MMC 2A Data 5
	62	SDMMC2A_DAT6	SD/SDIO/MMC 2A Data 6

	64	SDMMC2A_DAT7	SD/SDIO/MMC 2A Data 7
	92	SDMMC3_CLK	SD/SDIO/MMC 3 Clock
	90	SDMMC3_CMD	SD/SDIO/MMC 3 Command
	84	SDMMC3_DAT0	SD/SDIO/MMC 3 Data 0
	86	SDMMC3_DAT1	SD/SDIO/MMC 3 Data 1
	88	SDMMC3_DAT2	SD/SDIO/MMC 3 Data 2
	82	SDMMC3_DAT3	SD/SDIO/MMC 3 Data 3
	80	SDMMC3_CD_N	SD/SDIO/MMC 3 Card Detect
	96	SDMMC3_CLK_LB_IN	Clock Loop Back input
	98	SDMMC3_CLK_LB_OUT	Clock Loop Back output

Note: SDMMC3_CLK_LB_IN connects to SDMMC_CLK_LB_OUT. Total trace length is the length of a round trip, from Tegra® to connector and back. SDMMC_CLK_LB_OUT trace should go till the connector and back to SDMMC3_CLK_LB_IN.

7.4 SATA

Tegra® K1 supports SATA specification Rev 3.1 and AHCI specification Rev 1.3.1

Connector No.	Pin Number	Pin Name	Description
3	28	SATA_L0_TXN	Transmit Data Negative
	30	SATA_L0_TXP	Transmit Data Positive
	36	SATA_L0_RXN	Receive Data Negative
	34	SATA_L0_RXP	Receive Data Positive
	42	SATA_TESTCLKN	Test Clock Negative
	40	SATA_TESTCLKP	Test Clock Positive

7.5 USB

The USB complex consists of a single USB 3.0 controller and three USB 2.0 controllers. The USB 3.0 controller supports up to 2 regular USB 3.0 ports and their companion regular USB 2.0 ports. The USB 2.0 controllers support up to: 2x regular USB ports, 2x HSIC interfaces.

Features supported are

- Universal Serial Bus Specification Revision 3.0
- Universal Serial Bus Specification Revision 2.0, plus the following
  - USB Battery Charging Specification, version 1.0; including Data Contact Detect protocol
  - Modes: Host and Device
  - Speeds: Low, Full, and High
- Enhanced Host Controller Interface Specification for Universal Serial Bus revision 1.0

Connector No.	Pin Number	Pin Name	Description
4	49	USB0_ID	ID Pin
4	56	USB0_DN	USB 0 Data Negative
4	58	USB0_DP	USB 0 Data Positive
3	6	USB0_VBUS	Detects presence of VBUS
2	89	USB_VBUS_EN0	VBUS Enable 0
4	50	USB1_DN	USB 1 Data Negative
4	52	USB1_DP	USB 1 Data Positive
4	46	USB2_DN	USB 2 Data Negative
4	44	USB2_DP	USB 2 Data Positive
4	66	USB3_RX0N	USB 3 Receive Data Negative
4	64	USB3_RX0P	USB 3 Receive Data Positive
4	72	USB3_TX0N	USB 3 Transmit Data Negative
4	70	USB3_TX0P	USB 3 Transmit Data Positive
4	87	USB_VBUS_EN1	VBUS Enable 1
3	2	USB_VBUS_EN2	VBUS Enable 2

7.6 HSIC

Connector No.	Pin Number	Pin Name	Description
3	55	HSIC1_DATA	Serial Data 1
	57	HSIC1_STROBE	Strobe 1
	63	HSIC2_DATA	Serial Data 2
	61	HSIC2_STROBE	Strobe 2

7.7 PCI Express (PCIe)

Tegra® K1 supports PCI Express Base Specification Revision 2.0. K1 series processors integrate an x4 lane PCIe bridge to enable a control path from the Tegra® chip to external PCIe devices. Two PCIe Gen2 controllers (one with a maximum width of x4 and the other with a maximum width of x1) support connections to one or two endpoints.

Connector No.	Pin Number	Pin Name	Description
4	83	PEX_CLK1N	Clock 1 Negative
4	85	PEX_CLK1P	Clock 1 Positive
3	25	PEX_CLK2N	Clock 2 Negative
3	23	PEX_CLK2P	Clock 2 Positive
4	84	PEX_USB3_RX1N	Receive Data 1 Negative
4	86	PEX_USB3_RX1P	Receive Data 1 Positive
4	78	PEX_USB3_TX1N	Transmit Data 1 Negative
4	80	PEX_USB3_TX1P	Transmit Data 1 Positive

4	96	PEX_RX2N	Receive Data 2 Negative
4	98	PEX_RX2P	Receive Data 2 Positive
4	90	PEX_TX2N	Transmit Data 2 Negative
4	92	PEX_TX2P	Transmit Data 2 Positive
3	3	PEX_RX3N	Receive Data 3 Negative
3	5	PEX_RX3P	Receive Data 3 Positive
3	9	PEX_TX3N	Transmit Data 3 Negative
3	11	PEX_TX3P	Transmit Data 3 Positive
4	91	PEX_RX4N	Receive Data 4 Negative
4	89	PEX_RX4P	Receive Data 4 Positive
4	97	PEX_TX4N	Transmit Data 4 Negative
4	95	PEX_TX4P	Transmit Data 4 Positive
3	15	PEX_REFCLKN	Reference Clock Negative
3	17	PEX_REFCLKP	Reference Clock Positive
3	31	PEX_L0_CLKREQ_N	Reference Clock Request 0
3	29	PEX_L1_CLKREQ_N	Reference Clock Request 1
3	33	PEX_WAKE_N	Wake
3	37	PEX_L0_RST_N	Reset 0
3	35	PEX_L1_RST_N	Reset 1

Various configurations of PCIe, USB3.0 and SATA exist as per the table below

#	USB 3.0	PCIe	SATA	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	SATA
				USB3_TX0 USB3_RX0	PEX_USB3_TX1 PEX_USB3_RX1	PEX_TX2 PEX_RX2	PEX_TX3 PEX_RX3	PEX_TX4 PEX_RX4	SATA_TX SATA_RX
1	2	1 x1 & 1x2	1	USB_SS#0	USB_SS#1	PCIe#1_0	PCIe#0_1	PCIe#0_0	SATA
2	1	1 x4	1	USB_SS#0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	SATA
3	0	1 x1 & 1x4	1	PCIe#1_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	SATA
4	1	1 x1 & 1x4	0	PCIe#1_0	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#1

7.8 SPI

SPI controller supports both master (up to 65MHz) and slave (up to 45MHz) operation. It allows a duplex, synchronous, serial communication between the controller and external peripheral devices.

Connector No.	Pin Number	Pin Name	Description
4	53	SPI1A_SCK	SPI 1A Clock
4	75	SPI1A_DIN	SPI 1A Data IN
4	79	SPI1A_DOUT	SPI 1A Data Out
4	67	SPI1A_CS0	SPI 1A CS0
1	57	SPI4C_SCK	SPI 4C Clock

1	61	SPI4C_DIN	SPI 4C Data IN
1	63	SPI4C_DOUT	SPI 4C Data Out
1	67	SPI4C_CS0	SPI 4C CS0
1	65	SPI4C_CS1	SPI 4C CS1
1	59	SPI4C_CS3	SPI 4C CS3

7.9 I2C

Tegra® K1's I2C interface adheres to NXP Inter-IC Bus specification. The I2C controller supports multiple masters and slaves in: Standard-mode (up to 100Kbit/s), Fast-mode (up to 400 Kbit/s), Fast-mode plus (Fm+, up to 1Mbit/s) and High-speed mode (up to 3.4Mbit/s) of operations.

Connector No.	Pin Number	Pin Name	Description
2	35	CAM_I2C_SCL	CAM I2C Clock
2	37	CAM_I2C_SDA	CAM I2C Data
2	93	GEN2_I2C_SCL	GEN2 I2C Clock
2	95	GEN2_I2C_SDA	GEN2 I2C Data
1	4	DP_AUX_CH0_N	I2C6_DAT, Muxed
1	6	DP_AUX_CH0_P	I2C6_CLK, Muxed
1	41	DDC_SCL	I2C4_DAT, Muxed
1	37	DDC_SDA	I2C4_CLK, Muxed

7.10 UART

UART controller provides serial data synchronization and data conversion (parallel-to-serial and serial-to-parallel) for both receiver and transmitter sections.
The controller supports both 16450 and 16550 compatible modes. Default mode is 16450.
Device clock upto 200MHz, at a Baud rate of 12.5Mbits/second
Flow control support on RTS and CTS

Connector No.	Pin Number	Pin Name	Description
1	70	UART3_CTS_N	UART 3 Clear to send
	72	UART3_RTS_N	UART 3 Request to send
	74	UART3_RXD	UART 3 Receive
	76	UART3_TXD	UART 3 Transmit
	71	UD3_RTS	UD 3 Request to send
	73	UD3_CTS	UD 3 Clear to send
	75	UD3_TXD	UD 3 Transmit
	77	UD3_RXD	UD 3 Receive
	87	UA3_CTS	UA 3 Clear to send
	85	UA3_RTS	UA 3 Request to send
	81	UA3_RXD	UA 3 Receive
	83	UA3_TXD	UA 3 Transmit

7.11 AUDIO INTERFACES

Tegra® K1 supports I2S and Sony/Philips Digital Interface Format (S/PDIF).

7.11.1 I2S

The controller supports I2S format, Left-justified Mode format, Right-justified Mode format, and DSP mode format, as defined in the Philips inter-IC-sound (I2S) bus specification.

- The I2S and PCM (master and slave modes) interfaces support clock rates up to 24.5760MHz.
- Basic I2S modes to be supported (I2S, RJM, LJM and DSP) in both Master and Slave modes
- PCM mode with short (one-bit-clock wide) and long-fsync (two bit-clocks wide) in both master and slave modes.
- TDM mode with flexibility in number of slots and slot(s) selection
- Support for u-Law and A-Law compression/decompression

Connector No.	Pin Number	Pin Name	Description
3	67	DAP2_SCLK	DAP 2 Serial Clock/Bit Clock
3	69	DAP2_FS	DAP 2 Frame Sync/Word Select
3	71	DAP2_DOUT	DAP 2 Data Out
3	73	DAP2_DIN	DAP 2 Data In
3	56	DAP3_SCLK	DAP 3 Serial Clock/Bit Clock
3	54	DAP3_FS	DAP 3Frame Sync/Word Select
3	52	DAP3_DIN	DAP 3 Data In
3	50	DAP3_DOUT	DAP 3 Data Out
1	91	DAP4_SCLK	DAP 4 Serial Clock/Bit Clock
1	93	DAP4_FS	DAP 4 Frame Sync/Word Select
1	95	DAP4_DIN	DAP 4 Data In
1	97	DAP4_DOUT	DAP 4 Data Out

7.11.2 SPDIF

Its features include

- Five data formats: 16-bit, 20-bit, 24-bit, Raw, 16-bit packed
- Supported sample rates: 32, 44.1, 48, 88.2, 96, 176.4 and 192 kHz

Connector No.	Pin Number	Pin Name	Description
2	77	SPDIF_IN	Data IN
	79	SPDIF_OUT	Data OUT

7.12 GPIO

The following table lists the available GPIOs

Connector No.	Pin No	Pin Name
1	12	GPIO_PK0
	18	GPIO_PJ2
	20	GPIO_PI0
	28	GPIO_PU5
	30	GPIO_PU4
	32	GPIO_PU6
	36	GPIO_PG0
	38	GPIO_PG3
	40	GPIO_PG2
	42	GPIO_PG1
2	18	GPIO_PCC1
	20	GPIO_PBB0
	83	GPIO_PI1
3	4	GPIO_PFF2
	49	GPIO_PV1
	51	GPIO_PV0
	62	GPIO_X5_AUD
	64	GPIO_X1_AUD
	66	GPIO_X6_AUD
	74	GPIO_W2_AUD
	76	GPIO_X3_AUD
	78	GPIO_W3_AUD
	10	KB_COL0
	12	KB_COL3
	14	KB_COL4
	16	KB_COL6
	18	KB_COL2
	20	KB_COL7
	22	KB_COL1
	24	KB_COL5
	83	KB_ROW17
	84	KB_ROW3
	85	KB_ROW10
	86	KB_ROW14
	87	KB_ROW9
	88	KB_ROW7

	89	KB_ROW6
	90	KB_ROW5
	91	KB_ROW16
	92	KB_ROW12
	93	KB_ROW0
	94	KB_ROW11
	95	KB_ROW8
	96	KB_ROW1
	97	KB_ROW4
	98	KB_ROW15
	99	KB_ROW4
4	31	GPIO6_PMIC
	33	GPIO4_PMIC
	35	GPIO5_PMIC
	55	GPIO3_PO.04
	57	GPIO3_PO.01
	59	GPIO3_PO.02
	63	GPIO3_PO.06
	65	GPIO3_PO.03
	69	GPIO3_PO.00
	73	GPIO3_PO.07
	77	GPIO3_PO.05

8 Wireless module

e-con Systems has re-certified Texas Instrument's wireless module with the FCC ID: 2ALXI-SOMWB1, for re-use into e-con Systems' SOM. This module is called as eSOMWB1. The FCC Certification for eSOMWB1 grants single modular certification, as per FCC part 15C requirements.

e-con Systems' customers can re-use this wireless certification to save cost and time in the product design by following the integration instructions given below.

8.1 Host End products requirements for re-using the FCC ID

The Host using the SOM with eSOMWB1 module do not require any additional testing as an intentional radiator as long as

- The following antennas or antennas of same type and equal or lesser gain is used in the final product

Manufacturer	Part Number	Type	Gain
LSR	001-0012	Dipole	2dBi
Laird	CAF94505	PCB	2dBi

- Any restrictions found in the grants are followed in the usage of the module
    - This device is to be used only for mobile and fixed applications
        - The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons.
    - The antenna / transmitter must not transmit simultaneously with any other antenna or transmitter.
    - The antenna(s) used for this transmitter must not exceed a maximum gain of 2dBi
- The host end product can use the FCC ID of the certified Wireless transmitter module as its FCC ID (since every wireless product should have an FCC ID)
- A label displaying the FCC ID of the certified Wireless Transmitter module should be placed on a visible location in the end product with the following text “Contains FCC ID: 2ALXI-SOMWB1”

8.2 Product Regulatory Information

8.2.1 FCC Declaration of Conformity

The product contains the following FCC ID: 2ALXI-SOMWB1. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (i.) this device may not cause harmful interference and (ii.) this device must accept any interference received, including interference that may cause undesired operation (FCC 15.19)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult an authorized dealer or service representative for help.

Only peripherals (computer input/output devices, terminals, printers, etc.) certified to comply with the Class B limits may be attached to this device. Operation with non-certified peripherals is likely to result in interference to radio and TV reception.

9 Control, Boot options and Reset

Connector No.	Pin Number	Pin Name	Direction	Description
3	43	EN5V	Output	Enable signal from PMIC to enable 5V supply to SOM. Power-on state is pulled Low by PMIC
3	45	AC_OK	Input	Input to PMIC, indicates all supplies are good, should be low for PMIC to start PU to VCC_2P5 via 75K resistor
3	46	RESET_OUT_N	Output	Reset OUT from Processor PU to VCC_1P8_SD5 via 1M
4	38	XRES_IN	Input	Reset input to PMIC PU to VCC_2P5 via 75K resistor
4	29	LID	Input	PMIC starts only if this pin is low, PD via 75K resistor.
4	36	VCC_2P5	Output	Always On supply from PMIC, derived from 12V Not to be loaded
1	5	VCC_3P3_LS_1	Output	Last of the Power-on sequence supplies Not to be loaded (only for enable Base Board Power Supply).
3	6	USB0_VBUS	Input	This pin detects presence of USB HOST
1	36 42 40 38	GPIO_PG0 GPIO_PG1 GPIO_PG2 GPIO_PG3	I/O	Power-on State decides Boot source. 1000 [3:0] => Boot from SPI 1011 [3:0] => Boot from eMMC Configured for eMMC boot in eSOMTK1

10 Electrical Specification

10.1 Input Power Supply & Ground pins

Connector No.	Pin Number	Direction	Pin Name	Description
4	1,3,5,7,9,11,13,15	Input	VCC_5	5V input supply
4	2,4,6,8,10,12,14,16,18,20,22,24	Input	VCC_12	12V input supply
1	8,9,10,11,17,22,23,29,34,35,44,45,55,56,68,69,78,7989,94,99,100		Ground	Digital Ground
2	1,2,4,712,13,16,19,22,24,25,30,31,33,36,39,41,42,47,48,53,54,56,59,62,65,68,70,71,73,75,76,81,82,91,92,94,97,98,99,100		Ground	Digital Ground
3	1,7,8,13,19,21,26,27,32,39,41,44,47,48,53, 58,59,60,65,68,70,75,81,82,99,100		Ground	Digital Ground
4	17,19,21,23,26,27,28,30,32,37,39,40,42, 45,48,51,54,60,61,62,68,71,74,76,81,82, 87,88,93,94,99,100		Ground	Digital Ground

10.2 Output Power Supply

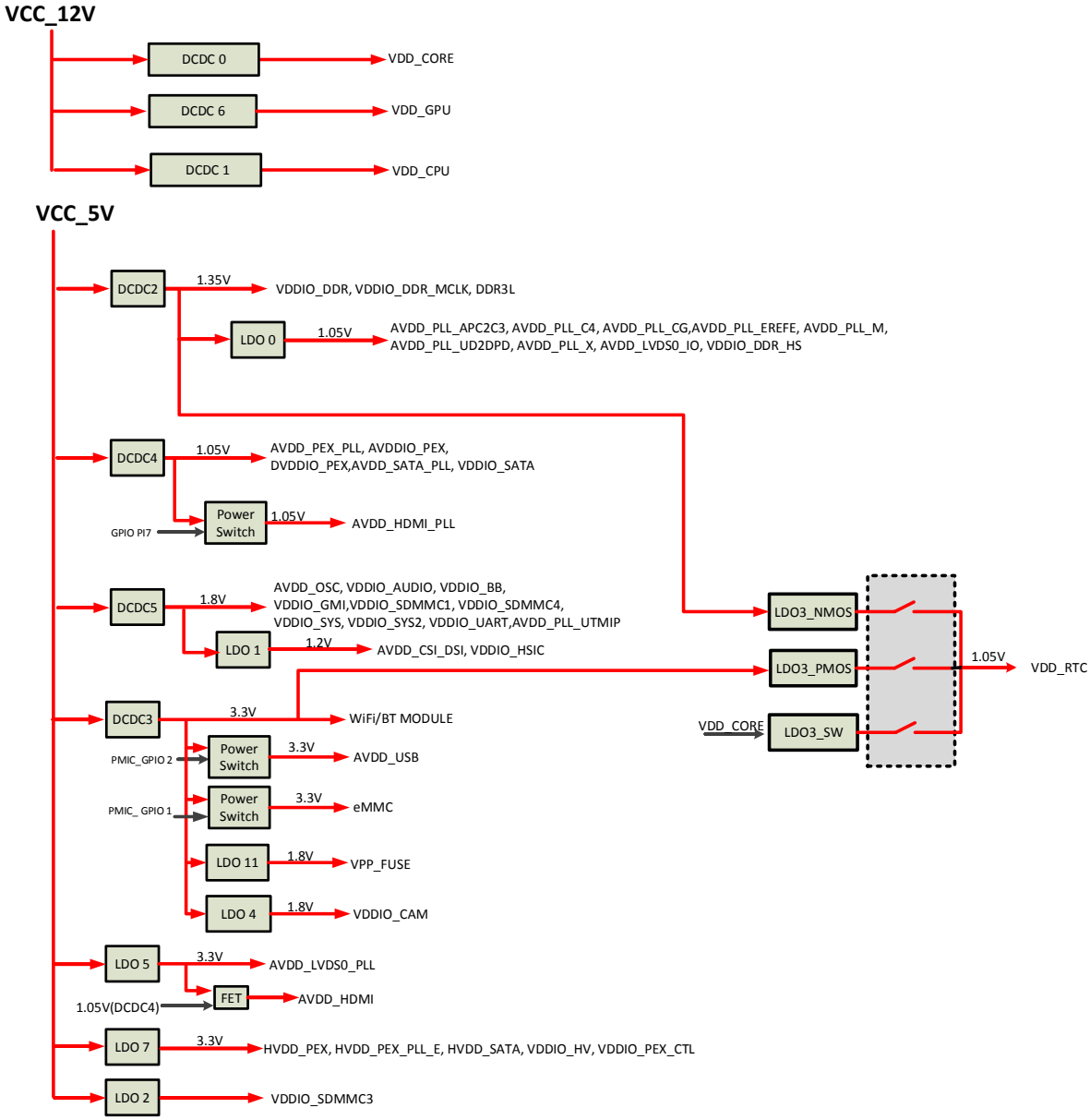
Connector No.	Pin Number	Direction	Pin Name	Default Voltage (V)	Configurable Voltage Range (V)	Maximum Current (mA)	Description
1	7	Output	VCC_1P8_SD5	1.8V	Not Applicable	50	1.8V O/P from SD5
2	6	Output	VCC_3P3_LDO2	OFF	0.825 to 3.3	300	3.3V O/P from LDO2 (For SD Card IO only)
2	8	Output	VCC_LDO6	OFF	0.825 to 1.5	300	LDO6 Output
2	10	Output	VCC_LDO10	OFF	0.825 to 3.3	300	LDO10 Output
4	25	Output	VCC_LDO9	OFF	0.825 to 3.3	300	LDO9 Output

10.3 Processor Power Domains

Domain	Power PIN	Source	Voltage (V)
RTC	VDD_RTC	PMIC LDO 3	1.1
CORE CLOCKS	AVDD_OSC	PMIC DCDC 5	1.8
	AVDD_PLL_APC2C3	PMIC LDO 0	1.05
	AVDD_PLL_C4	PMIC LDO 0	1.05
	AVDD_PLL_CG	PMIC LDO 0	1.05
	AVDD_PLL_EREFE	PMIC LDO 0	1.05
	AVDD_PLL_M	PMIC LDO 0	1.05
	AVDD_PLL_UD2DPD	PMIC LDO 0	1.05
	AVDD_PLL_UTMIP	PMIC DCDC 5	1.8
	AVDD_PLL_X	PMIC LDO 0	1.05
DIGITAL, I/O	VDDIO_AUDIO	PMIC DCDC 5	1.8
	VDDIO_BB	PMIC DCDC 5	1.8
	VDDIO_CAM	PMIC LDO 4	1.8
	VDDIO_GMI	PMIC DCDC 5	1.8
	VDDIO_HV	PMIC LDO 7	3.3
	VDDIO_SDMMC1	PMIC DCDC 5	1.8
	VDDIO_SDMMC3	PMIC LDO 2	
	VDDIO_SDMMC4	PMIC DCDC 5	1.8
	VDDIO_SYS	PMIC DCDC 5	1.8
	VDDIO_SYS_2	PMIC DCDC 5	1.8

	VDDIO_UART	PMIC DCDC 5	1.8
DISPLAY / CAMERA	AVDD_CSI_DSI	PMIC LDO 1	1.2
	AVDD_HDMI	PMIC LDO 5 Through Power switch EN Control is PMIC DCDC 4	3.3
	AVDD_HDMI_PLL	PMIC DCDC 4 Through Power switch EN Control Processor GPIO PI7	1.05
	AVDD_LVDS0_IO	PMIC LDO 0	1.05
	AVDD_LVDS0_PLL	PMIC LDO 5	3.3
USB 2.0 / HSIC	AVDD_USB	PMIC DCDC 3 Through Power switch EN Control is PMIC GPIO2	3.3
	VDDIO_HSIC	PMIC LDO 1	1.2
USB 3.0 + PCIe	AVDDIO_PEX	PMIC DCDC 4	1.05
	DVDDIO_PEX	PMIC DCDC 4	1.05
	AVDD_PEX_PLL	PMIC DCDC 4	1.05
	HVDD_PEX	PMIC LDO 7	3.3
	HVDD_PEX_PLL_E	PMIC LDO 7	3.3
	VDDIO_PEX_CTL	PMIC LDO 7	3.3
SATA	VDDIO_SATA	PMIC DCDC 4	1.05
	HVDD_SATA	PMIC LDO 7	3.3
	AVDD_SATA_PLL	PMIC DCDC 4	1.05
FUSE	VPP_FUSE	PMIC LDO 11	1.8
DDR	VDDIO_DDR_HS	PMIC LDO 0	1.05
	VDDIO_DDR_MCLK	PMIC DCDC 2	1.35
	VDDIO_DDR	PMIC DCDC 2	1.35
GPU	VDD_GPU	PMIC DCDC 6	0.75 to 1.23
CPU	VDD_CPU	PMIC DCDC 1	0.75 to 1.26
Core	VDD_CORE	PMIC DCDC 0	0.8 to 1.15

10.4 SOM Power Flow



10.5 Power supply input

Main Power Supply: 12V and 5V Input voltage
Tolerance Allowed: 5%
Current Consumption: Depends on Use case

Use case	Current @ 12V (mA)	Current @ 5V (mA)	Peripherals Connected
Peak consumption during BOOT	580	600	Mouse & Keyboard attached to the 2 USB ports, no hub used HDMI Monitor
Consumption after OS is booted	80	400	Mouse & Keyboard attached to the 2 USB ports, no hub used HDMI Monitor

2 cameras streaming on HDMI Monitor Wi-Fi Streaming (YouTube video being played) Audio (headphones attached)	540	705	13MP (CSI B) at full HD and 4MP (CSI A) at 2688 x 1520 HDMI Monitor Mouse & Keyboard attached to the 2 USB ports, no hub is used
2 cameras- record in SD card *Wi-Fi streaming	500	735	Two 13MP cameras at full HD and recording in SD card HDMI Monitor. Mouse & Keyboard attached to the 2 USB ports, no hub used

10.6 DC Electrical Characteristics

VDD = 1.8V / 3.3V

Pad Type	Symbol	Parameter	Min	Max	Unit	Notes
ST	VIL	Input Low Voltage	-0.5	0.25 x VDD	V	Weak PU: 50 kΩ Weak PD: 50 kΩ
	VIH	Input High Voltage	0.75 x VDD	0.5 + VDD	V	
	VOL	Output Low Voltage (IOL = 1mA)		0.15 x VDD	V	
	VOH	Output High Voltage (IOH - -1mA)	0.85 x VDD		V	
DD	VIL	Input Low Voltage	-0.5	0.25 x VDD	V	3.3V tolerant pad Weak PU: 50 kΩ Weak PD: 50 kΩ
	VIH	Input High Voltage	0.75 x VDD	3.63	V	
	VOL	Output Low Voltage (IOL = 1mA)		0.15 x VDD	V	
	VOH	Output High Voltage (IOH - -1mA)	0.85 x VDD		V	
LV	VIL	Input Low Voltage	-0.5	0.25 x VDD	V	Weak PU: 15 kΩ Weak PD: 15 kΩ
	VIH	Input High Voltage	0.75 x VDD	0.5 + VDD	V	
	VOL	Output Low Voltage (IOL = 1mA)		0.15 x VDD	V	
	VOH	Output High Voltage (IOH - -1mA)	0.85 x VDD		V	
OD	VIL	Input Low Voltage	-0.5	0.25 x VDD	V	5V tolerant pad Weak PD: 100 kΩ
	VIH	Input High Voltage	0.75 x VDD	5.3	V	
	VOL	Output Low Voltage (IOL = 1mA)		0.15 x VDD	V	
	VOH	Output High Voltage (IOH - -1mA)	NA		V	
CZ	VIL	Input Low Voltage	-0.5	0.25 x VDD	V	Weak PU: 15 kΩ Weak PD: 15 kΩ
	VIH	Input High Voltage	0.75 x VDD	0.5 + VDD	V	
	VOL	Output Low Voltage (IOL = 1mA)		0.15 x VDD	V	
	VOH	Output High Voltage (IOH - -1mA)	0.85 x VDD		V	

10.7 Environmental Specifications

Operating Ambient Temperature Range	Min	Max
Commercial Range (°C)	0	70
Industrial Range (°C)	-40	85

Note:
Maximum CPU Junction temperature for both industrial and commercial Range: 105°C

11 Mechanical Specifications

All Dimensions are in mm

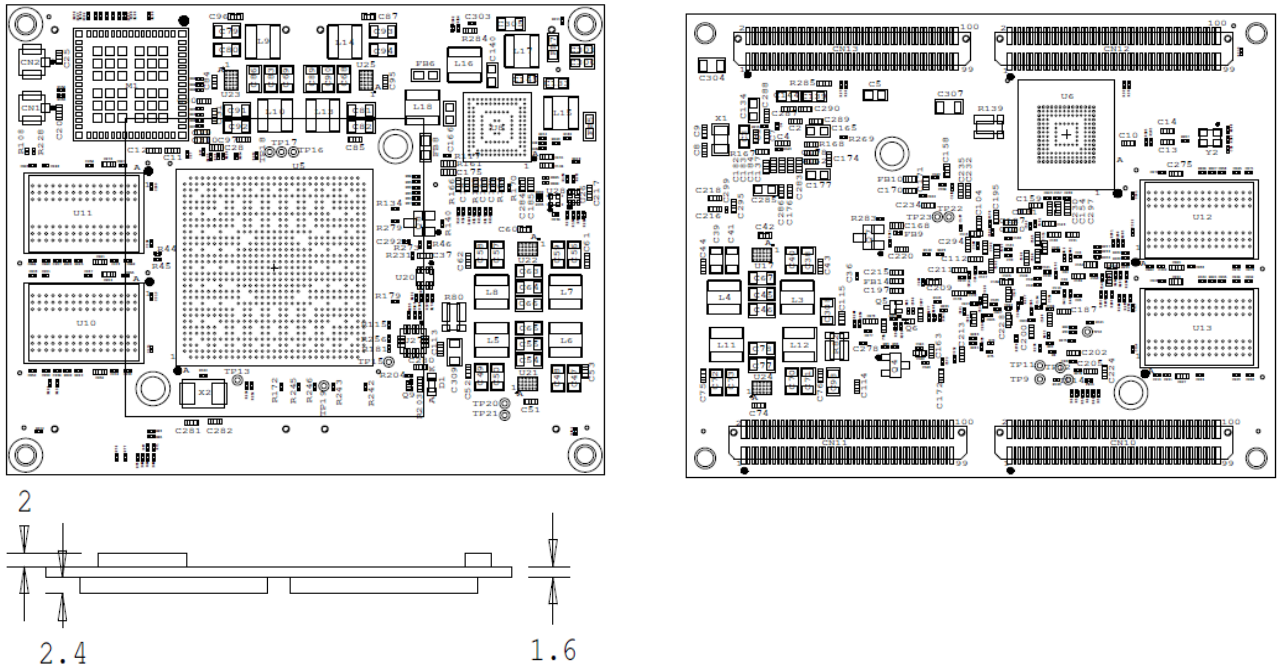
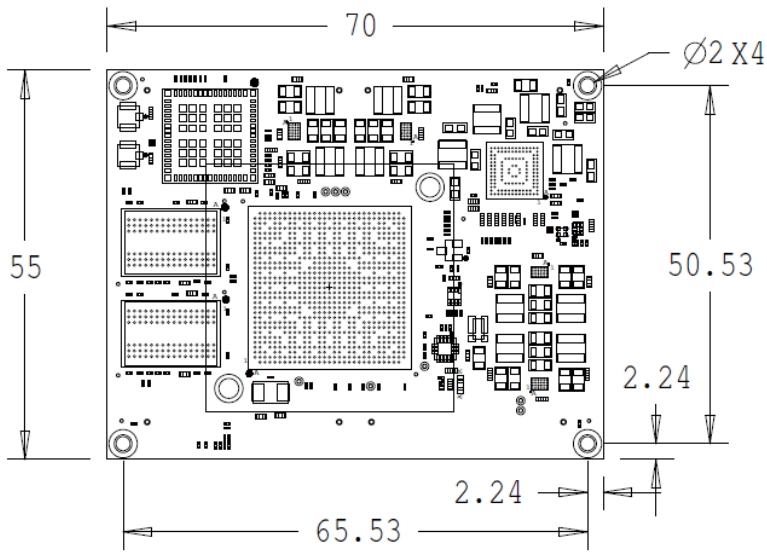


Figure 9-1: SOM – Top View, Bottom View and Side View

Mounting-hole position & SOM dimension



12 Revision History

Rev No	Date	Major Changes	Author
1.0	04 Feb 2016	Initial draft version	HW Team
1.1	22 July 2016	DDR Frequency changed to 792 MHZ	HW Team
1.2	07 Sep 2016	Operating Temperature and Current consumption added	HW Team
1.3	22 Sep 2016	Industrial Grade Part Number added	HW Team
1.4	28 Sep 2016	Output Power Supply Details updated	HW Team
1.5	06 Feb 2017	CPU Core Frequency Updated	HW Team
1.6	08 Jun 2017	SOM Power Flow, Processor Power Domains and SOM peripherals and their Interface added	HW Team
1.7	10 Aug 2017	Add Wi-Fi module certification information	HW Team