DVI-to-RGB (Sink) 1.7 IP Core User Guide

Revised February 2, 2017; Author Elod Gyorgy

1 Introduction

IP quick facts	
Provided with core	
Tested design flows	

2 Features

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3 Performance

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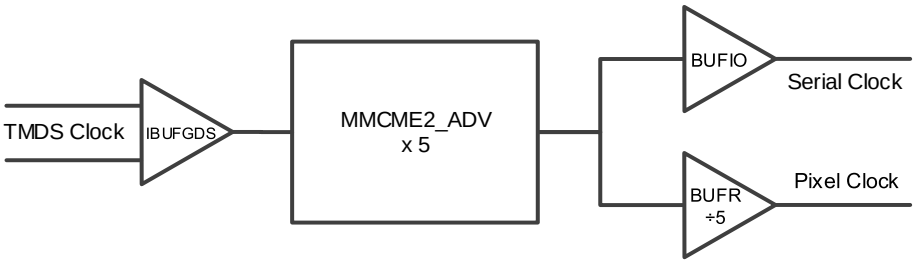

Figure 2. Clock network overview.

4.2 Data Decoder

4.2.1 Synchronization

4.2.2 Decoding

4.3 EDID ROM (Display Data Channel)

5 Port Descriptions

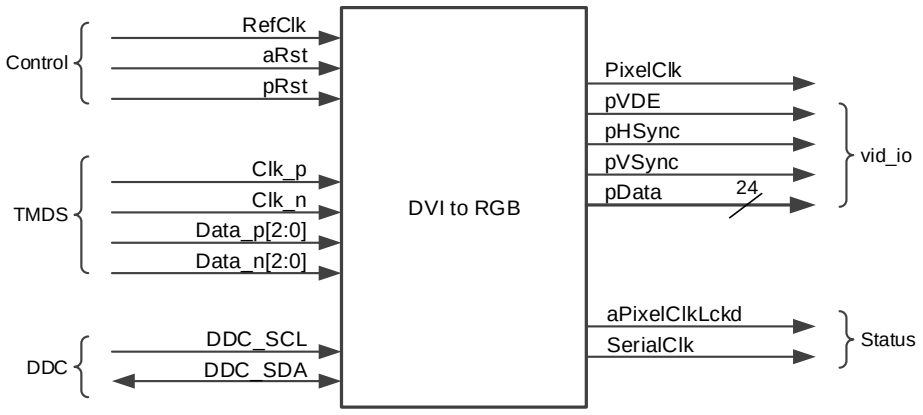

Figure 3. IP top-level diagram.

Table 1. Port descriptions.

6 Designing with the core

6.1 Constraints

```
create_clock -period 13.468 -waveform {0.000 5.000} [get_ports
hdmi_rx_clk_p]
```

6.2 Customization

might

6.3 Using SerialClk

6.4 Bundled EDID

Monitor	

Color characteristics	

Timing characteristics	

Table 2. Default EDID.

7 References

UG471: 7 Series FPGAs SelectIO Resources
UG472: 7 Series FPGAs Clocking Resources
XAPP460: Video Connectivity Using TMDS I/O in Spartan-3A FPGAs

XAPP495: Implementing a TMDS Video Interface in the Spartan-6 FPGA

WP249: SPI-4.2 Dynamic Phase Alignment
Digital Visual Interface DVI