

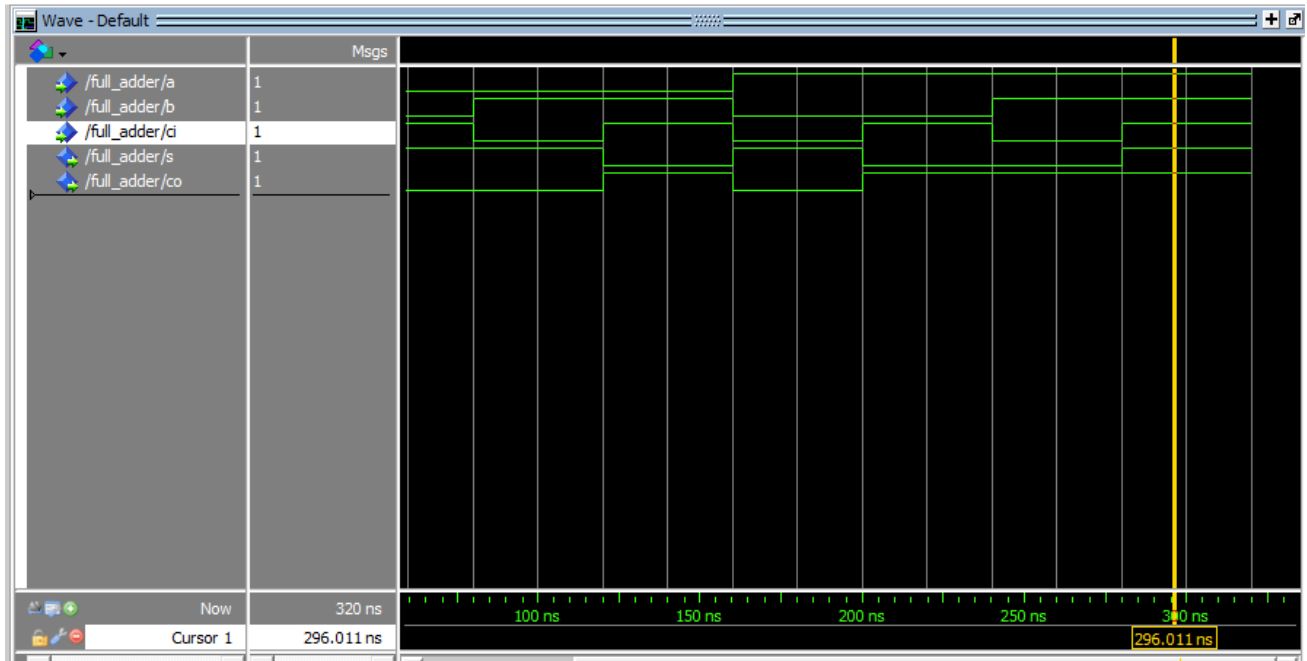
PACO, ARMIN R.
BSCpE – 3A

LOGIC GATES

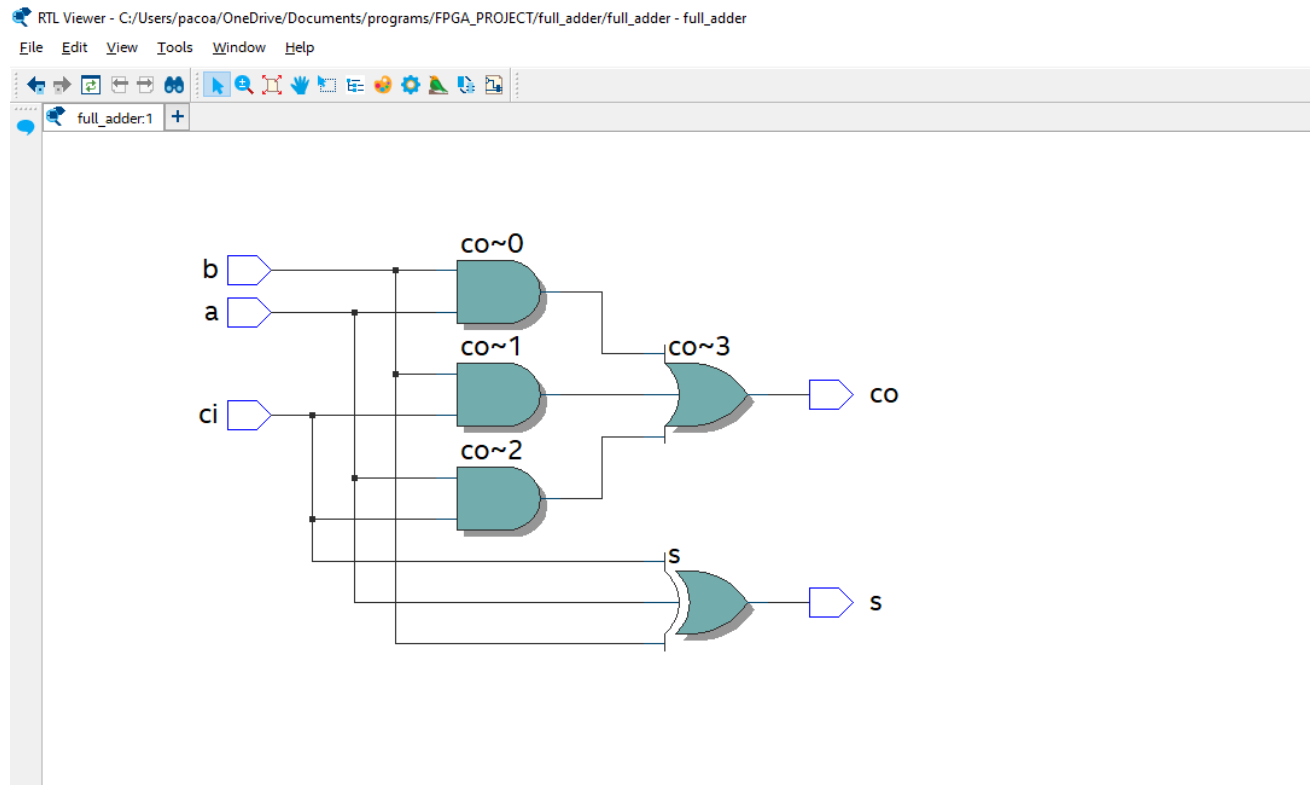
AIM: Write a VHDL code for all the logic gates.

#7-TITLE: EX-NOR gate

OUTPUT WAVE FORM:



RTL VIEW:



CODE:

full_adder.vhd

Compilation Report - full_adder

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5  entity full_adder is
6  Port (a, b, ci : in STD_LOGIC;
7        s, co : out STD_LOGIC);
8  end full_adder;
9
10 architecture behav1 of full_adder is
11 begin
12     s <= a xor b xor ci;
13     co <= (a and b) or (b and ci) or (ci and a);
14 end behav1;
```

