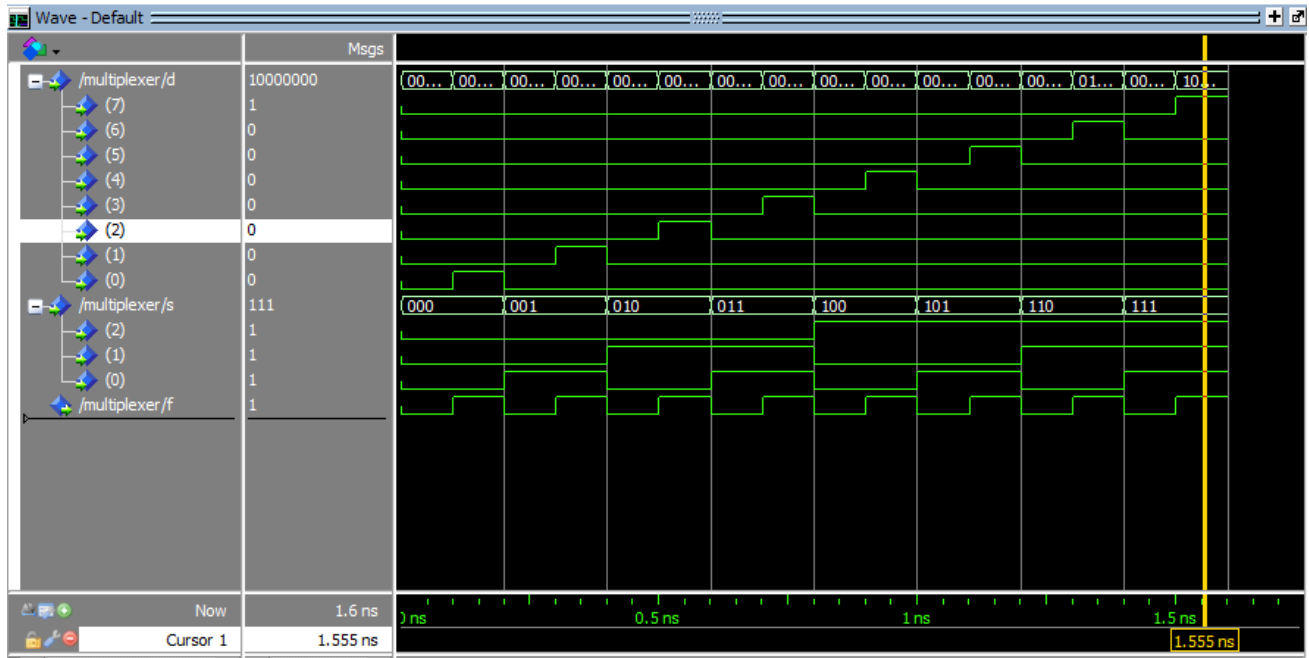


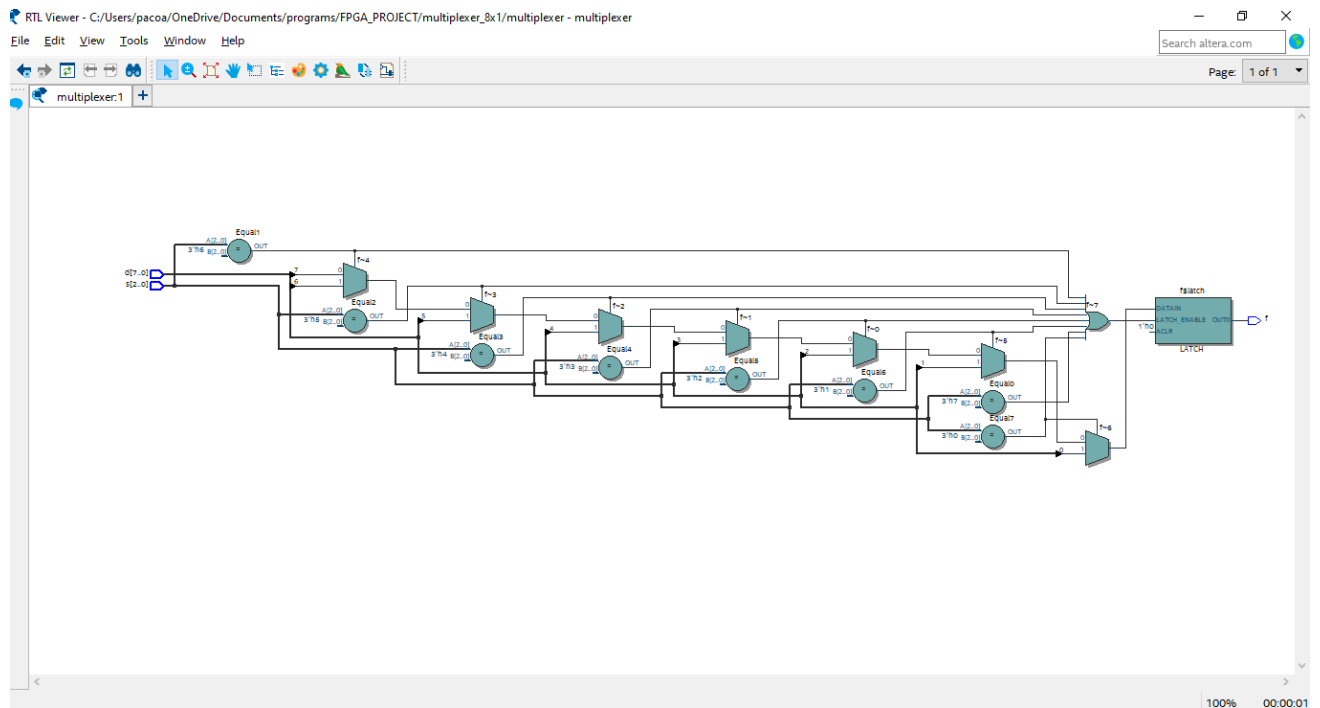
PACO, ARMIN R.
BSCpE – 3A

TITLE: MULTIPLEXER (8:1):

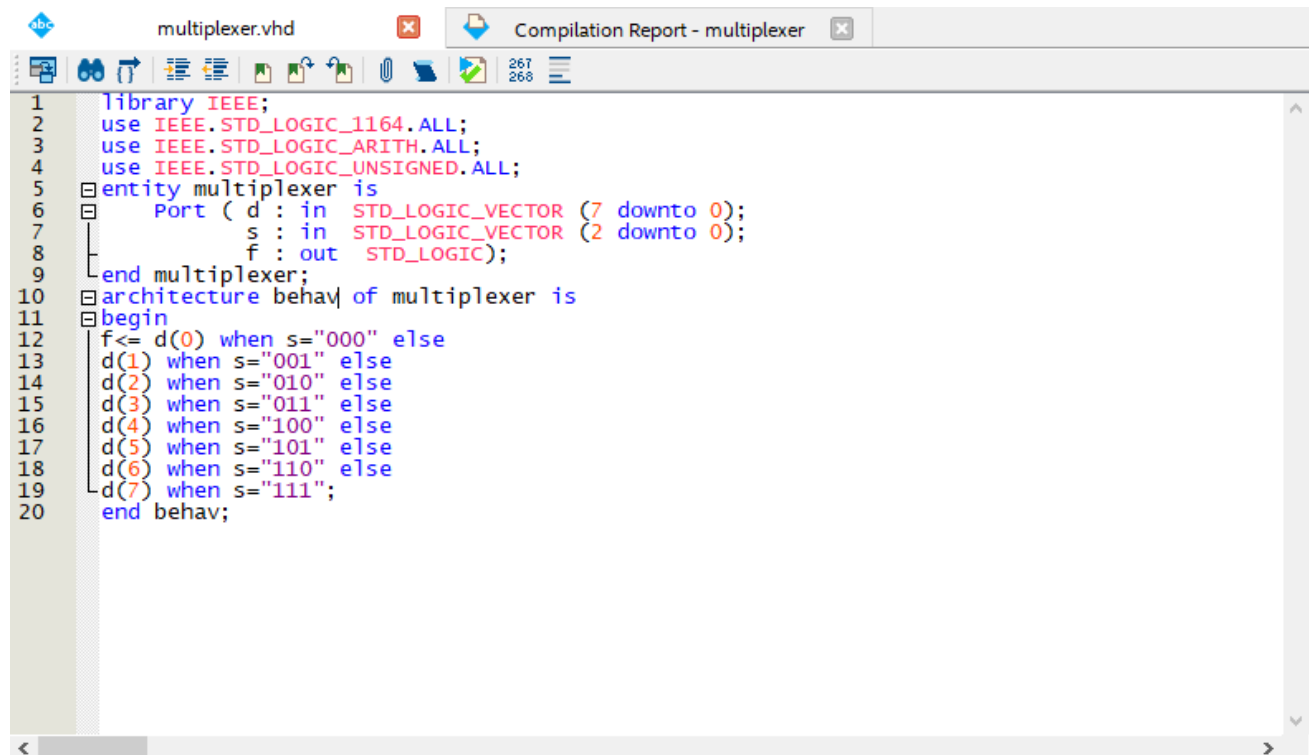
OUTPUT WAVE FORM:



RTL VIEW:



CODE:



The screenshot shows a VHDL code editor window titled "multiplexer.vhd". The code defines a multiplexer entity with two 8-bit data inputs (d) and a 2-bit select input (s), producing an 8-bit output (f). The architecture "behav" implements this using a series of conditional assignments based on the select input values.

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5  entity multiplexer is
6  Port ( d : in  STD_LOGIC_VECTOR (7 downto 0);
7        s : in  STD_LOGIC_VECTOR (2 downto 0);
8        f : out STD_LOGIC);
9  end multiplexer;
10 architecture behav of multiplexer is
11 begin
12   f<= d(0) when s="000" else
13   d(1) when s="001" else
14   d(2) when s="010" else
15   d(3) when s="011" else
16   d(4) when s="100" else
17   d(5) when s="101" else
18   d(6) when s="110" else
19   d(7) when s="111";
20 end behav;
```