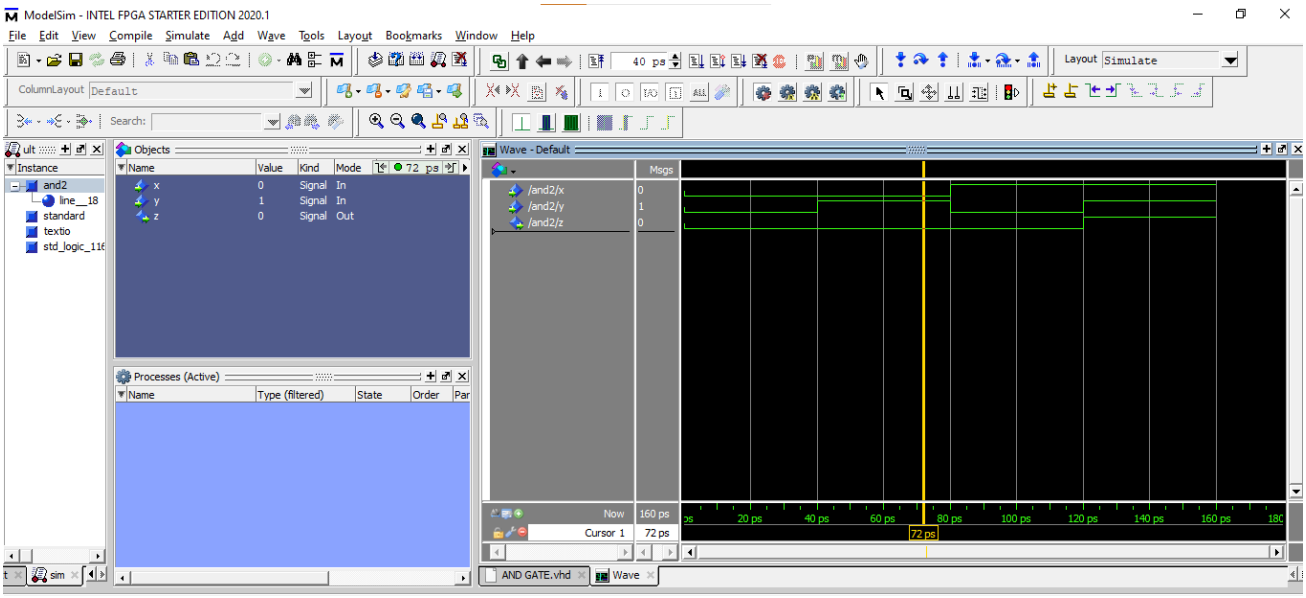
PACO, ARMIN R.
BSCpE – 3A

1.LOGIC GATES

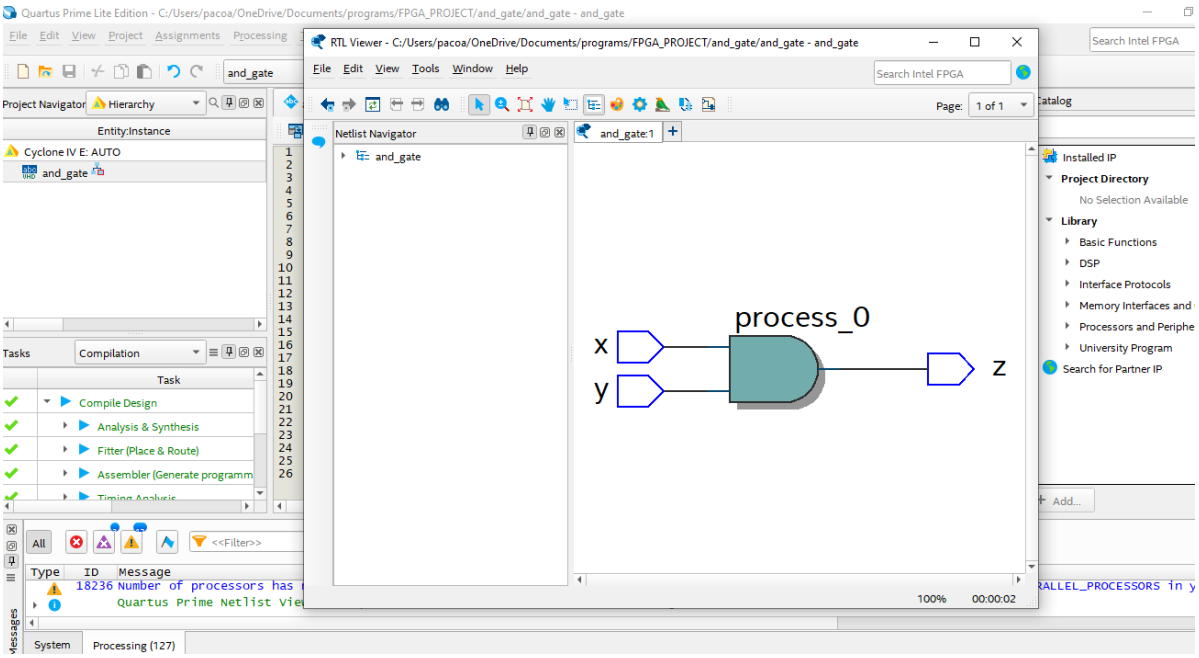
AIM: Write a VHDL code for all the logic gates.

#1-TITLE: AND gate

OUTPUT WAVE FORM:



RTL VIEW:



CODE:

and_gate.vhd

```
1  Library IEEE;
2              use IEEE.std_logic_1164.all;
3
4  entity and_gate is
5    port(
6     x : in STD_LOGIC;
7     y : in STD_LOGIC;
8     z : out STD_LOGIC
9        );
10 end and_gate;
11 --Dataflow model
12 architecture behav1 of and_gate is
13 begin
14 Z<= x and y;
15 end behav1; -- Behavioral model --Signal Assignment Statement
16 architecture behav2 of and_gate is
17 begin
18 process (x, y)
19 begin
20 if (x='1' and y='1') then    -- Compare with truth table
21 Z <= '1';
22 else
23 Z <= '0';
24 end if;
25 end process;
26 end behav2;
```