

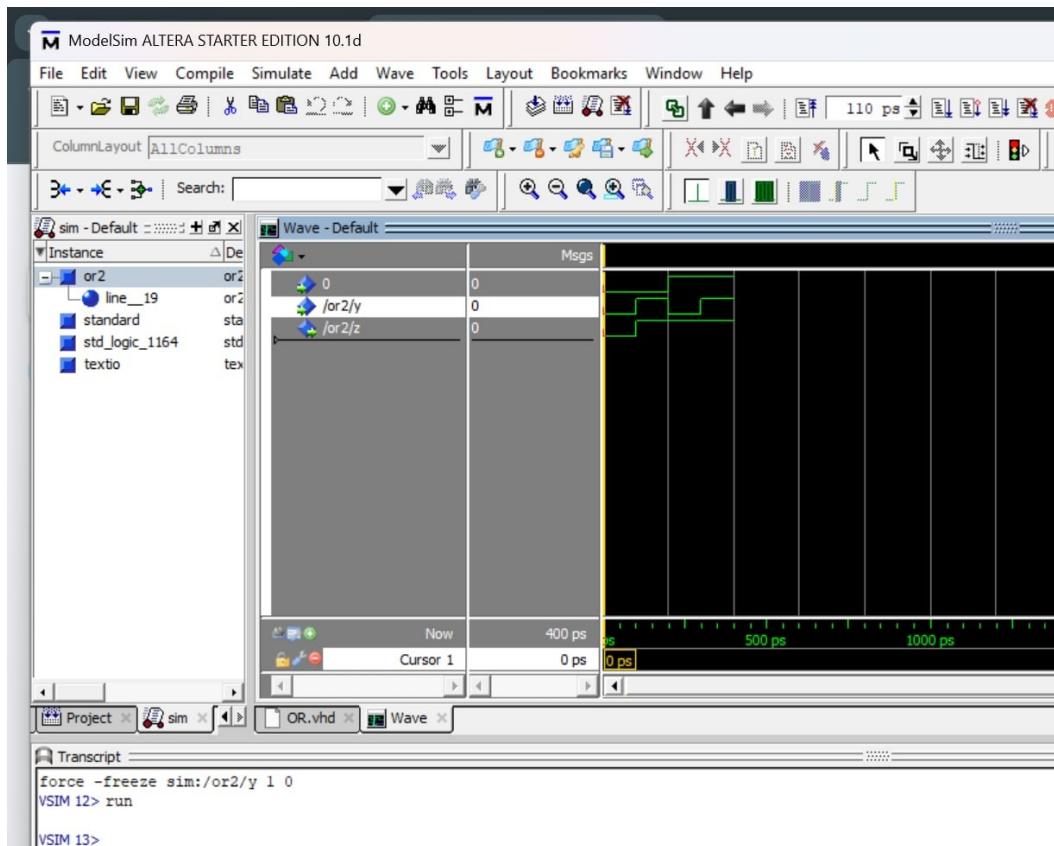
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BSCpE – 3A

1.LOGIC GATES

AIM: Write a VHDL code for all the logic gates.

#2-TITLE: OR gate

OUTPUT WAVE FORM:



RTL VIEW:

Quartus Prime Lite Edition - C:/Users/pacoa/OneDrive/Documents/programs/FPGA_PROJECT/or_gate/or_gate - or_gate

RTL Viewer - C:/Users/pacoa/OneDrive/Documents/programs/FPGA_PROJECT/or_gate/or_gate - or_gate

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Netlist Navigator

- or_gate

or_gate:1

```
graph LR; x --> process_0; y --> process_0; process_0 --> z_not[z~not]; z_not --> z;
```

100% 00:00:01

CODE:

The screenshot displays the Intel Quartus II IDE interface. On the left, the Project Navigator shows the hierarchy for 'Cyclone IV E: AUTO' with the file 'or_gate.vhd' selected. Below this, the Tasks window lists the compilation process: 'Compile Design', 'Analysis & Synthesis', 'Fitter (Place & Route)', 'Assembler (Generate programmm', and 'Timing Analysis'. The main editor window shows the VHDL code for 'or_gate.vhd'. The code defines an OR gate entity with two inputs (x, y) and one output (z). It includes two behavioral models: 'behav1' using a signal assignment statement and 'behav2' using a process block with an if-else statement to compare the inputs with the truth table. The bottom status bar includes a filter input and 'Find...' and 'Find Next' buttons.

```
1  Library IEEE;
2      use IEEE.std_logic_1164.all;
3
4  entity or_gate is
5      port(
6          x : in STD_LOGIC;
7          y : in STD_LOGIC;
8          z : out STD_LOGIC
9      );
10 end or_gate;
11 --Dataflow model
12 architecture behav1 of or_gate is
13 begin
14     Z <= x or y; --Signal Assignment Statement
15 end behav1;
16 -- Behavioral model
17 architecture behav2 of or_gate is
18 begin
19     process (x, y)
20     begin
21         if (x='0' and y='0') then -- Compare with truth table
22             Z <= '0';
23         else
24             Z <= '1';
25         end if;
26     end process;
27 end behav2;
```