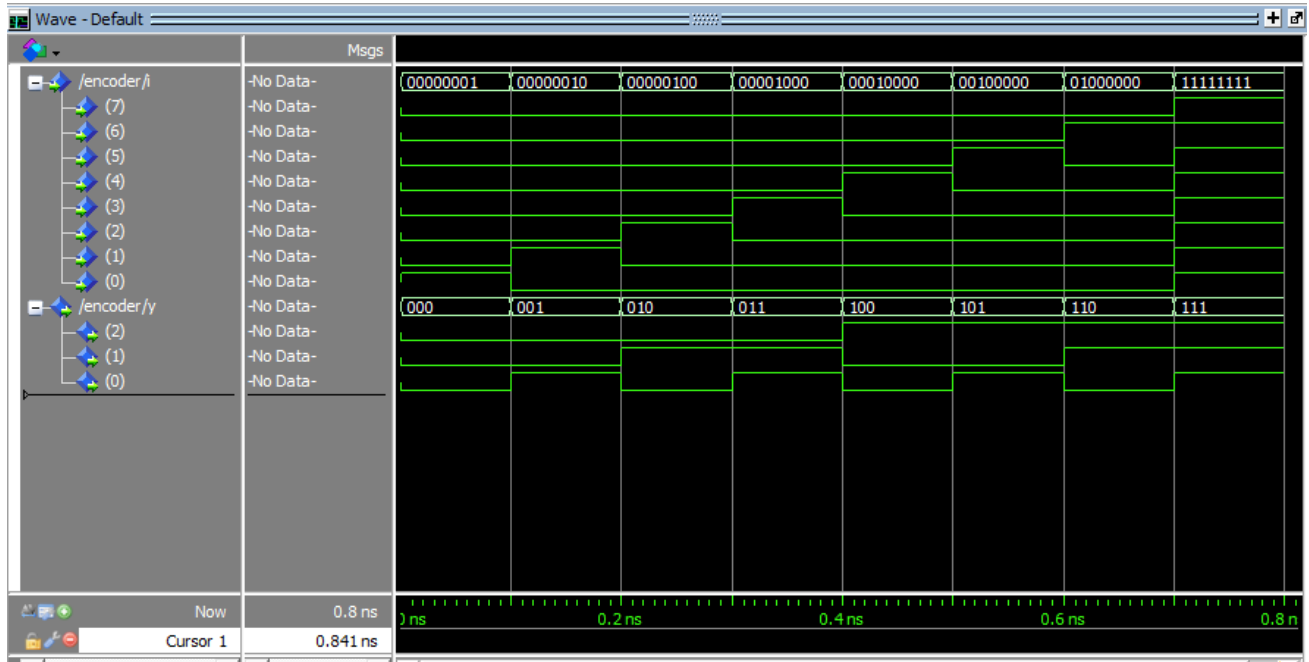


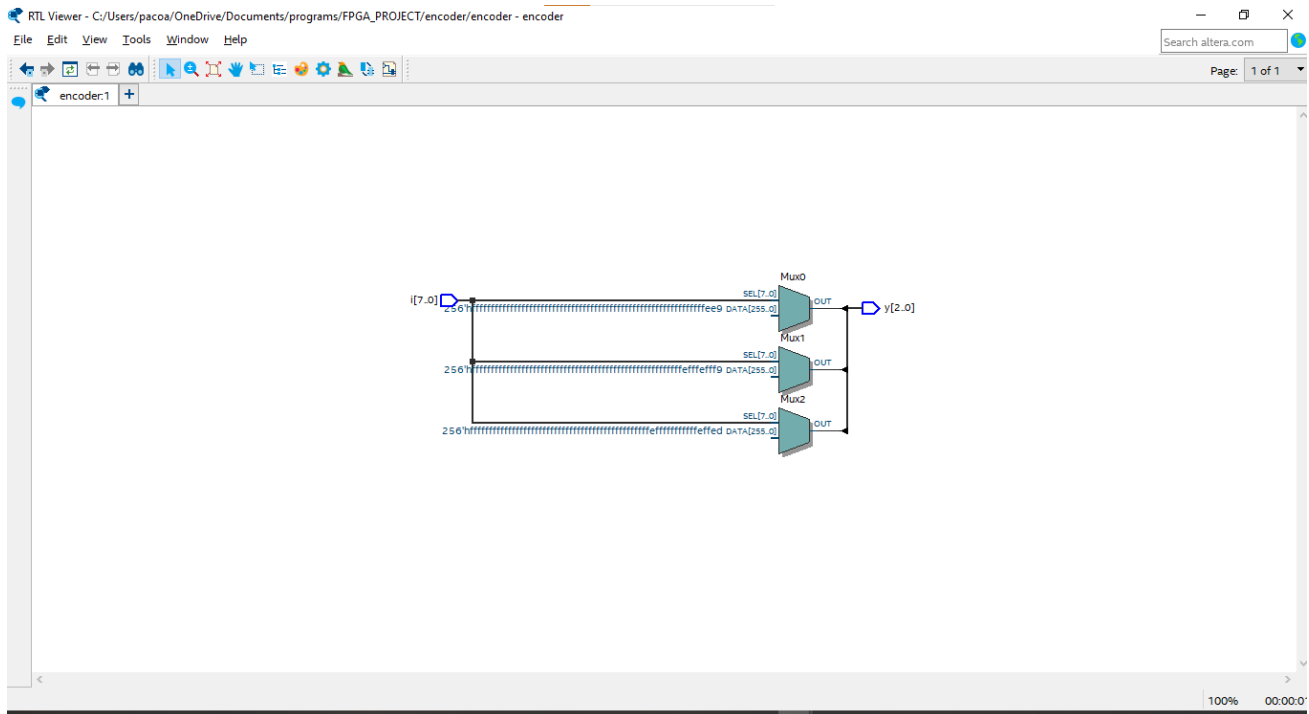
PACO, ARMIN R.
BSCpE – 3A

TITLE: ENCODER WITHOUT PRIORITY (8:3)

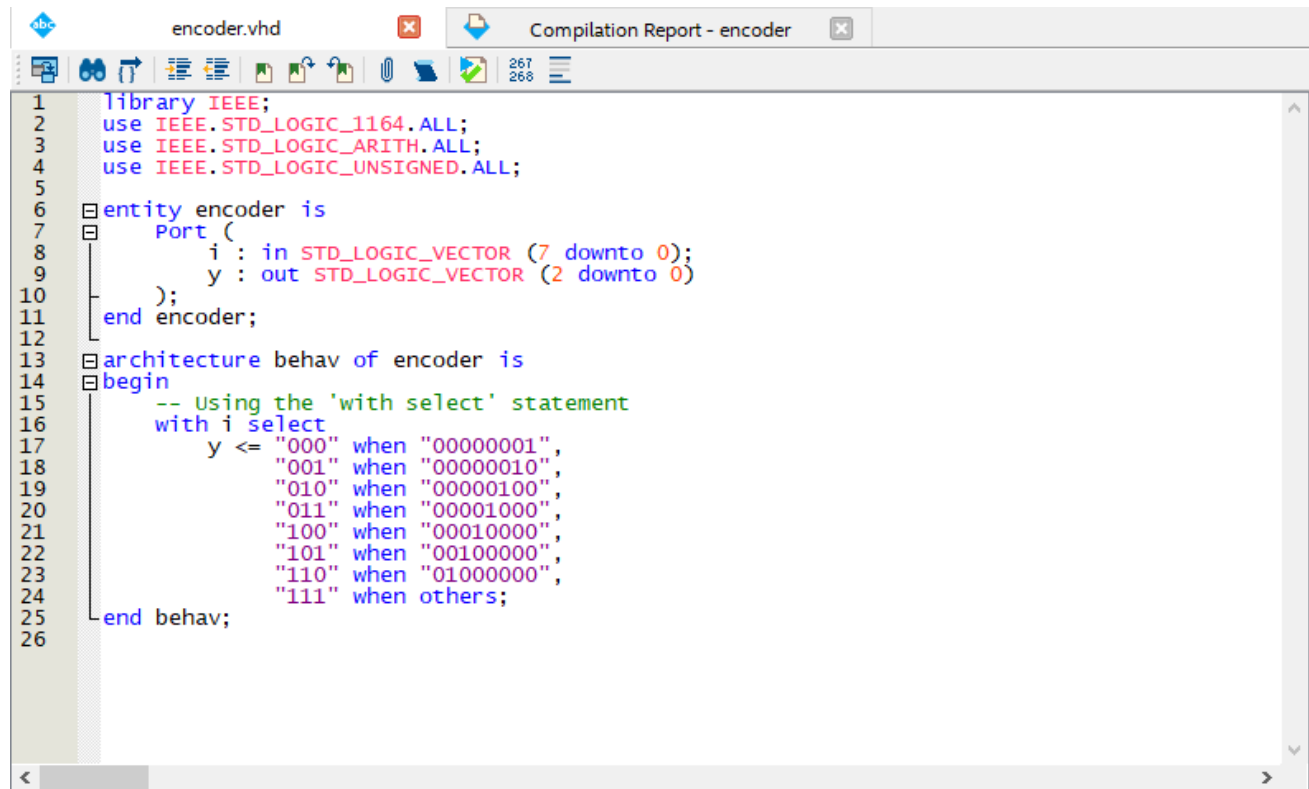
OUTPUT WAVE FORM:



RTL VIEW:



CODE:



The screenshot shows a VHDL code editor window titled 'encoder.vhd'. The code defines an entity 'encoder' with two ports: 'i' (a 7-bit input vector) and 'y' (a 2-bit output vector). The architecture 'behav' implements the encoder using a 'with select' statement. The output 'y' is assigned based on the value of 'i' using a case statement with 'when' clauses for each possible 3-bit input combination (000 to 111). The output values are the corresponding 2-bit binary representations of the input values.

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6  entity encoder is
7  port (
8      i : in STD_LOGIC_VECTOR (7 downto 0);
9      y : out STD_LOGIC_VECTOR (2 downto 0)
10 );
11 end encoder;
12
13 architecture behav of encoder is
14 begin
15     -- Using the 'with select' statement
16     with i select
17         y <= "000" when "00000001",
18             "001" when "00000010",
19             "010" when "00000100",
20             "011" when "00001000",
21             "100" when "00010000",
22             "101" when "00100000",
23             "110" when "01000000",
24             "111" when others;
25 end behav;
26
```