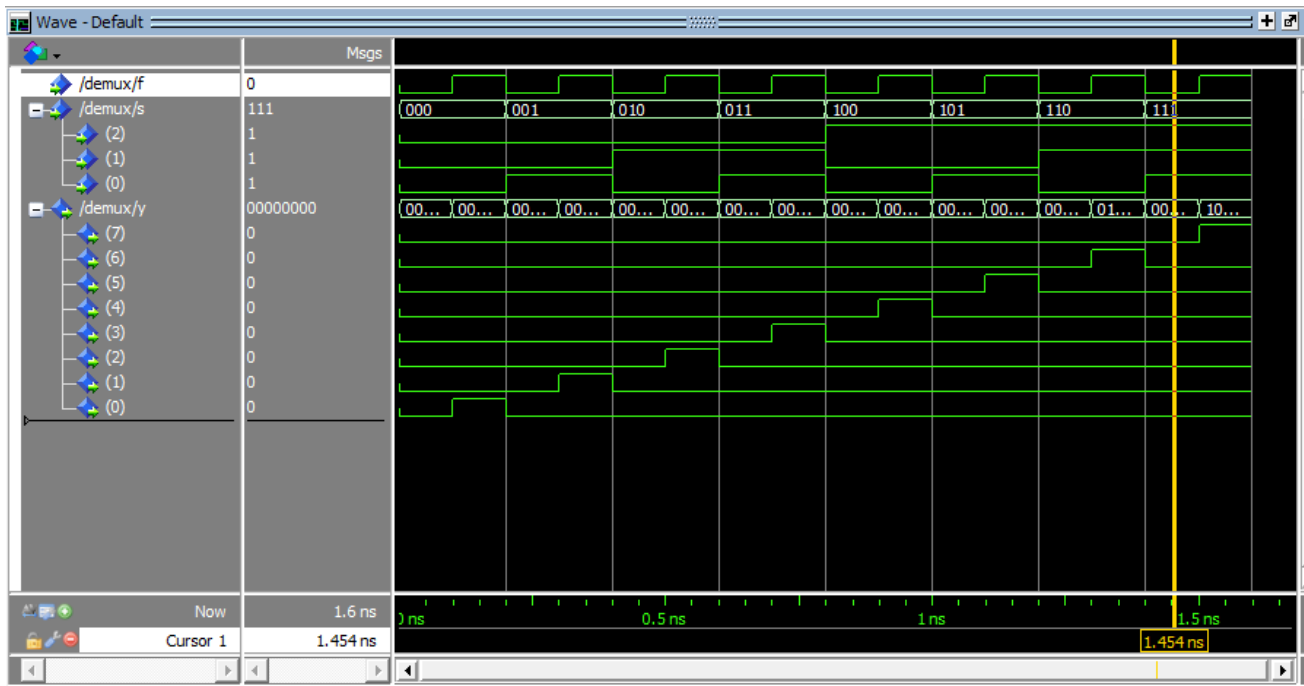


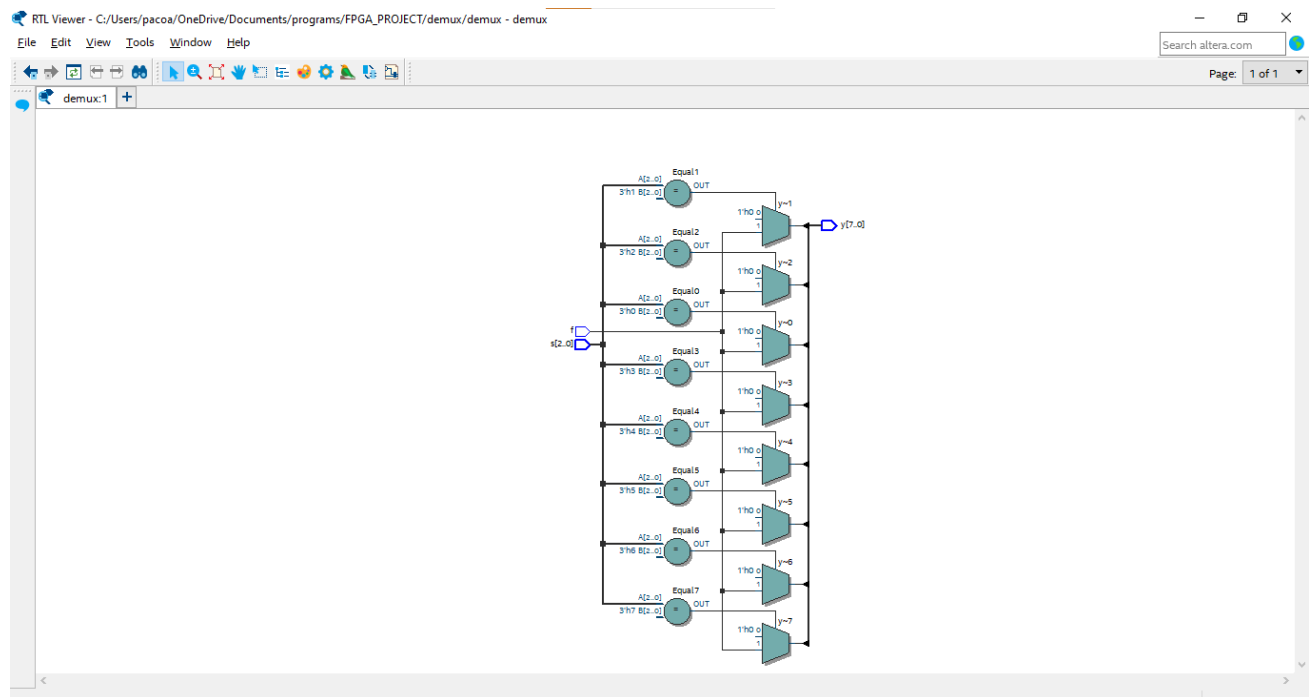
PACO, ARMIN R.
BSCpE – 3A

TITLE: Demultiplexer (1:8)

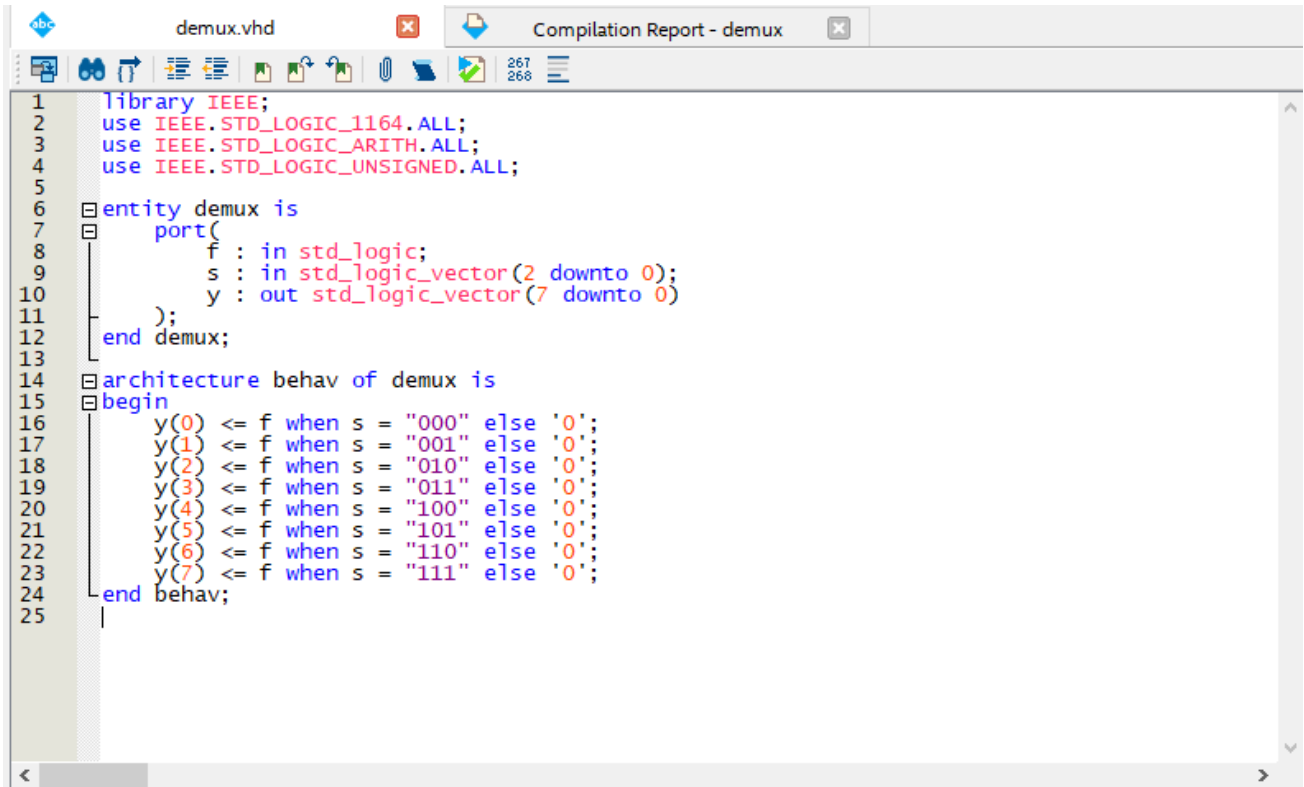
OUTPUT WAVE FORM:



RTL VIEW:



CODE:



The screenshot shows a VHDL code editor with a file named 'demux.vhd'. The code defines an entity 'demux' with three ports: 'f' (std_logic), 's' (std_logic_vector(2 downto 0)), and 'y' (std_logic_vector(7 downto 0)). The architecture 'behav' implements the demultiplexer logic using a series of conditional assignments. The output 'y' is set to '0' for all eight possible values of 's' (000 to 111), with the condition 'f' being checked for each. The code is as follows:

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6  entity demux is
7  port(
8      f : in std_logic;
9      s : in std_logic_vector(2 downto 0);
10     y : out std_logic_vector(7 downto 0)
11 );
12 end demux;
13
14 architecture behav of demux is
15 begin
16     y(0) <= f when s = "000" else '0';
17     y(1) <= f when s = "001" else '0';
18     y(2) <= f when s = "010" else '0';
19     y(3) <= f when s = "011" else '0';
20     y(4) <= f when s = "100" else '0';
21     y(5) <= f when s = "101" else '0';
22     y(6) <= f when s = "110" else '0';
23     y(7) <= f when s = "111" else '0';
24 end behav;
25
```