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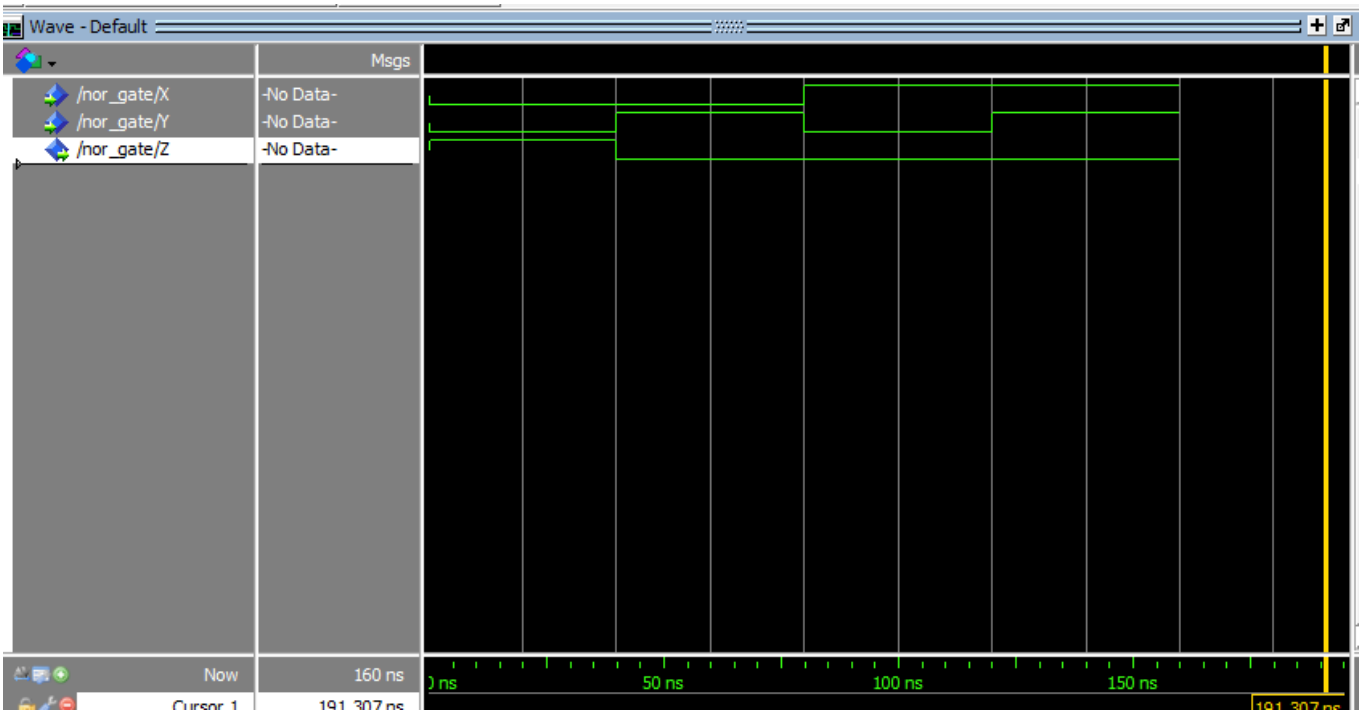
BSCpE – 3A

1.LOGIC GATES

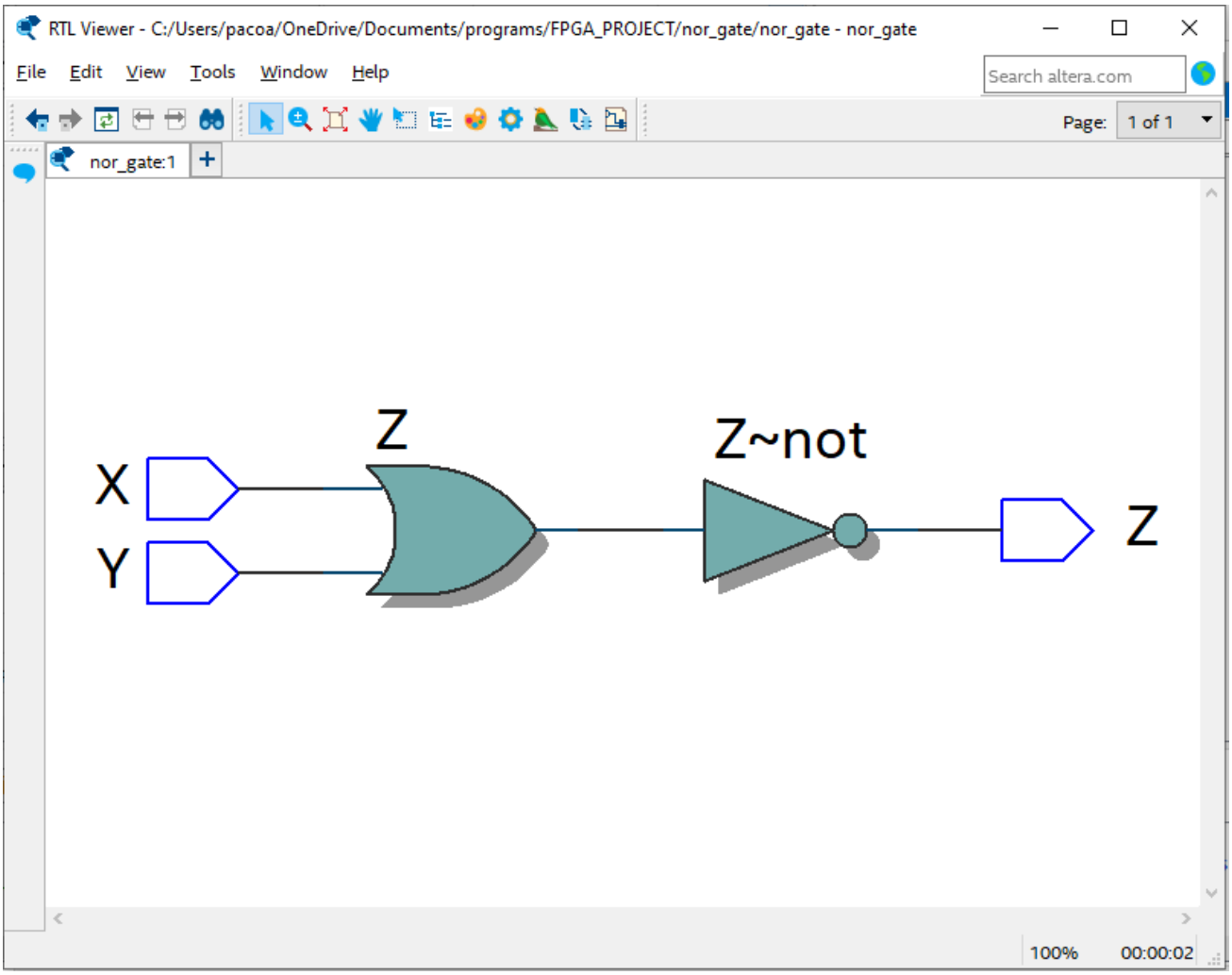
AIM: Write a VHDL code for all the logic gates.

#5- TITLE: NOR gate

OUTPUT WAVE FORM:



RTL VIEW:


RTL Viewer - C:/Users/pacoa/OneDrive/Documents/programs/FPGA_PROJECT/nor_gate/nor_gate - nor_gate
File Edit View Tools Window Help
Search altera.com
Page: 1 of 1
nor_gate:1
Z
Z~not
X
Y
Z
100%
00:00:02

CODE:

nor_gate.vhd | Compilation Report - nor_gate

```
1   Library IEEE;
2               use IEEE.std_logic_1164.all;
3
4   entity nor_gate is
5     Port (
6       X: in STD_LOGIC;
7       Y: in STD_LOGIC;
8       Z: out STD_LOGIC
9           );
10  end nor_gate;
11  --Dataflow model
12  architecture behav1 of nor_gate is
13  begin
14  Z<= x nor y; --Signal Assignment Statement
15  end behav1;
```