

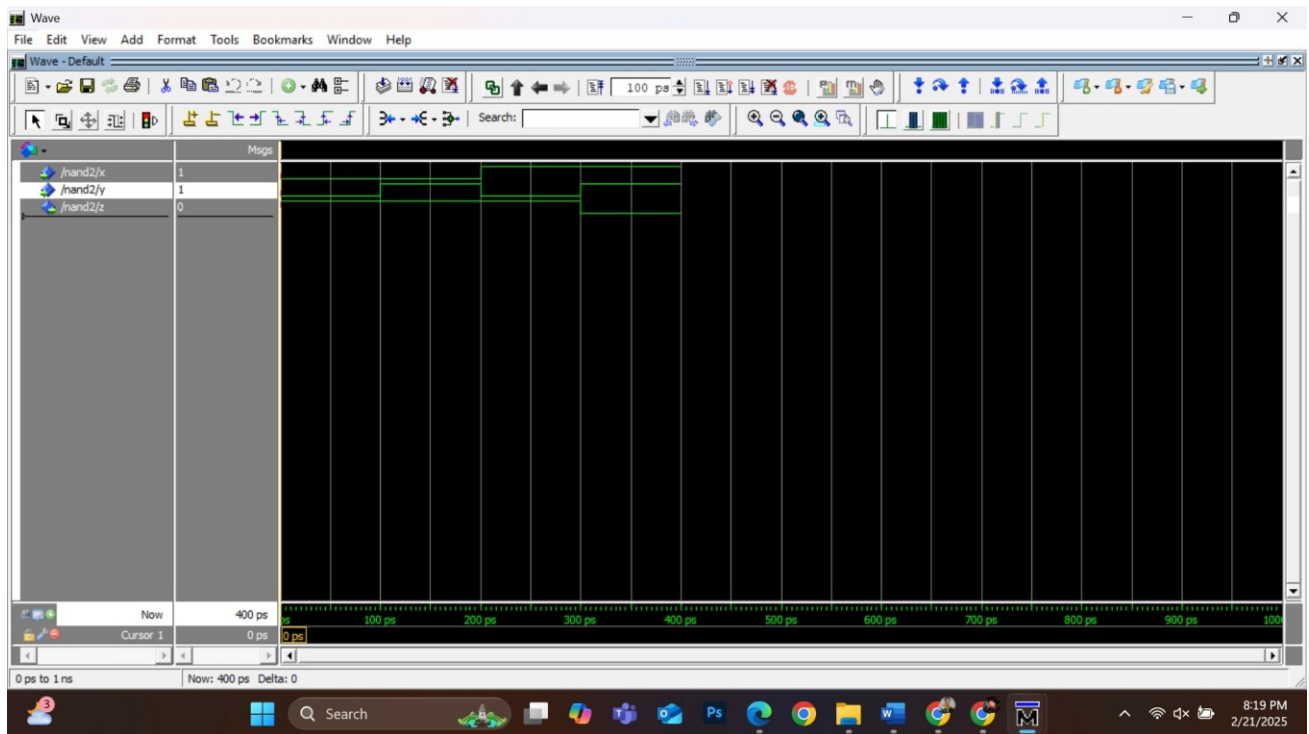
PACO, ARMIN R.
BSCpE – 3A

1.LOGIC GATES

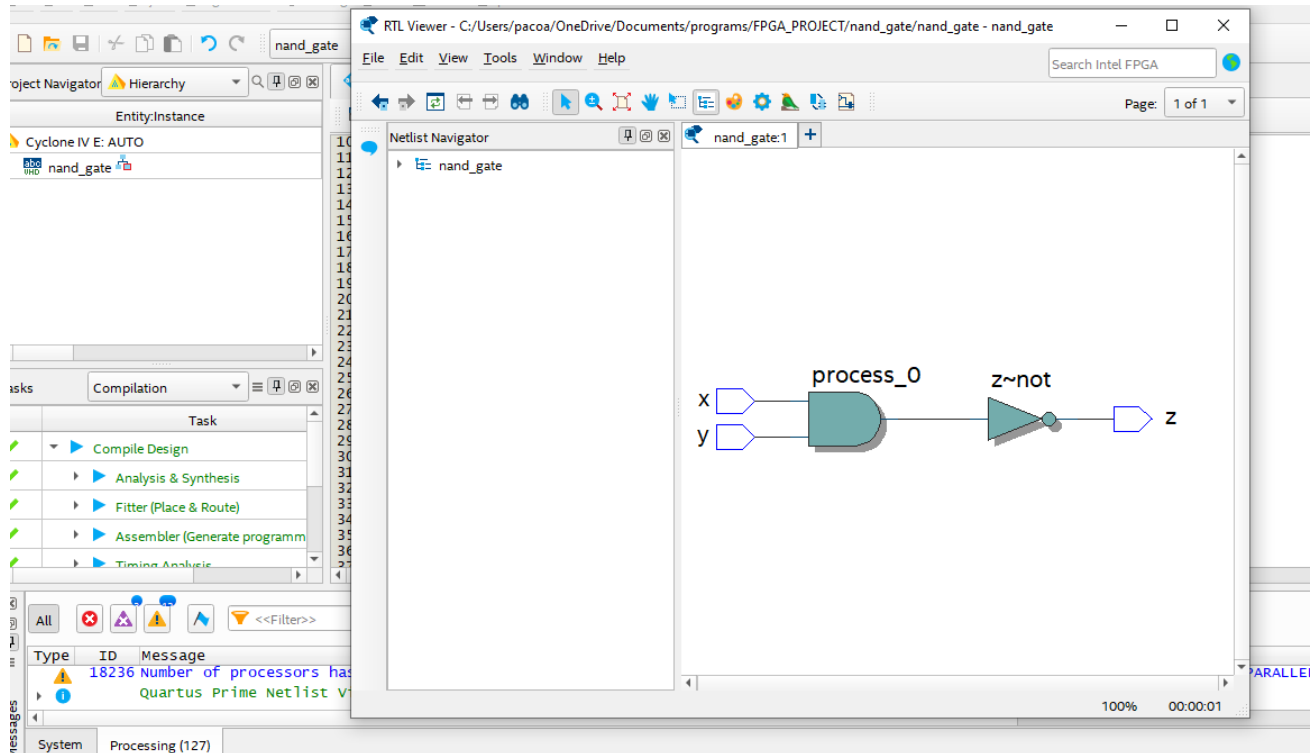
AIM: Write a VHDL code for all the logic gates.

#4-TITLE: NAND gate

OUTPUT WAVE FORM:



RTL VIEW:



CODE:

The screenshot shows the Quartus Prime IDE with the 'nand_gate.vhd' file open. The 'Project Navigator' on the left shows the hierarchy: 'Cyclone IV E: AUTO' > 'nand_gate'. The 'Tasks' pane shows a list of compilation tasks, with 'Compile Design' selected. The main area displays the VHDL code for the NAND gate. The code is as follows:

```
1  Library IEEE;
2      use IEEE.std_logic_1164.all;
3
4  entity nand_gate is
5  port(
6      x : in STD_LOGIC;
7      y : in STD_LOGIC;
8      z : out STD_LOGIC
9  );
10 end nand_gate;
11 --Dataflow model
12
13 architecture behav1 of nand_gate is
14 begin
15     z <= x nand y; --Signal Assignment Statement
16 end behav1;
17
18 -- Behavioral model
19
20
21
22
23 architecture behav2 of nand_gate is
24 begin
25     Process (x, y)
26     Begin
27
28         If (x='1' and y='1') then -- Compare with truth table
29             Z <= '0';
30         else
31             Z <= '1';
32         end if;
33     end process;
34
35
36 end behav2;
37
```