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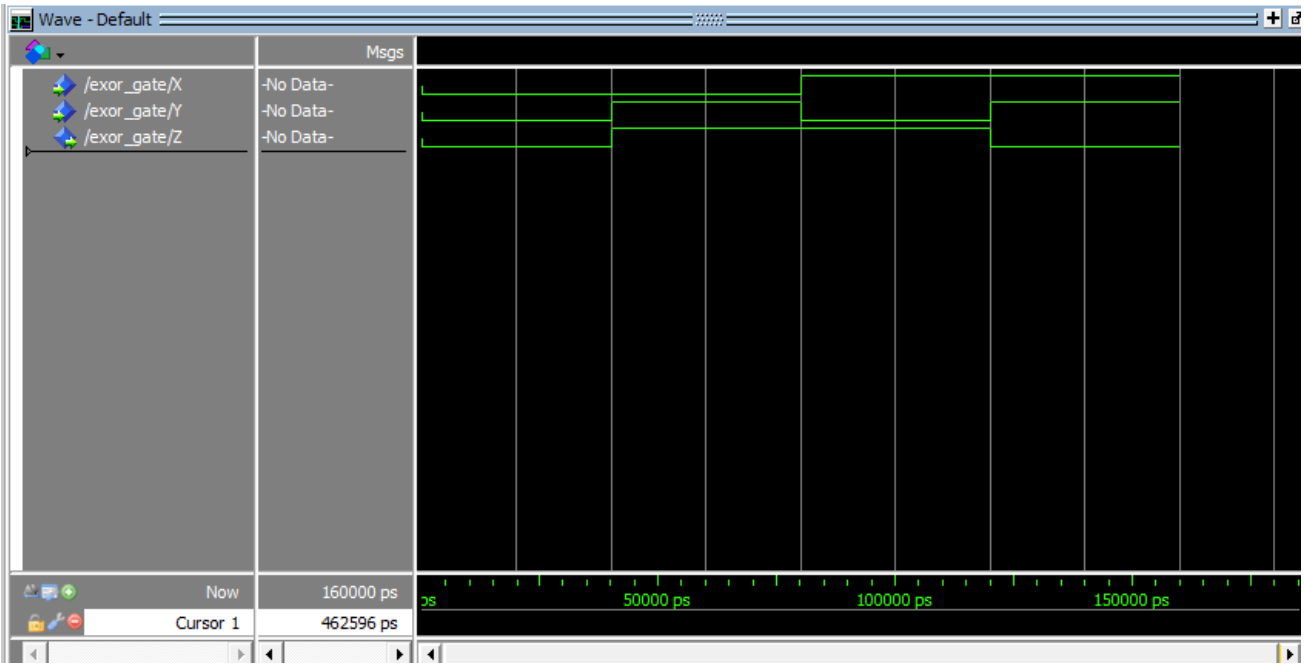
BSCpE – 3A

LOGIC GATES

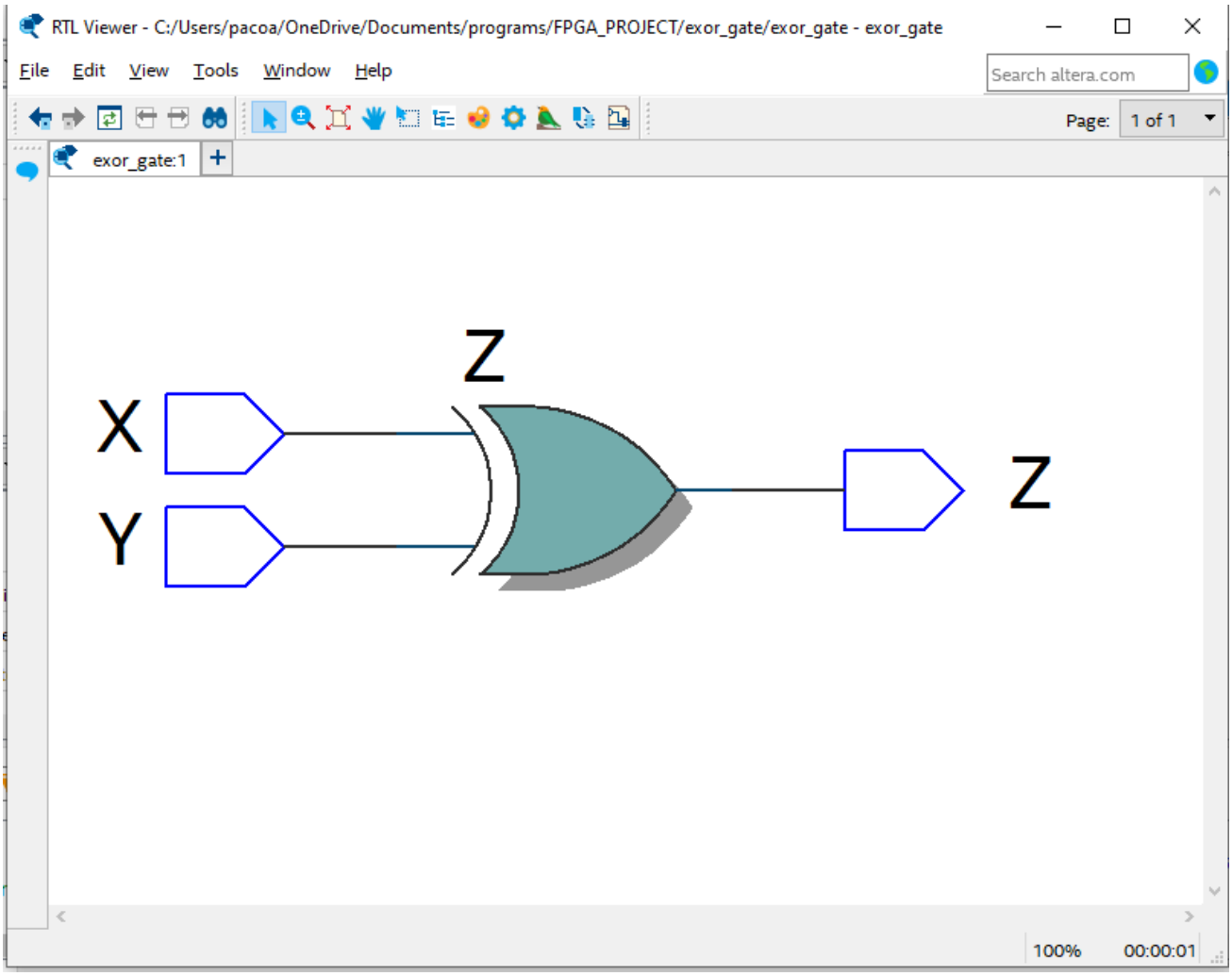
AIM: Write a VHDL code for all the logic gates.

#6-TITLE: EX-OR gate

OUTPUT WAVE FORM:



RTL VIEW:


RTL Viewer - C:/Users/pacoa/OneDrive/Documents/programs/FPGA_PROJECT/exor_gate/exor_gate - exor_gate
File
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Help
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Page:
1 of 1
exor_gate:1
Z
X
Y
Z
100%
00:00:01

CODE:

exor_gate.vhd | Compilation Report - exor_gate

```
1   Library IEEE;
2             use IEEE.std_logic_1164.all;
3
4   entity exor_gate is
5     Port (
6      X: in STD_LOGIC;
7      Y: in STD_LOGIC;
8      Z: out STD_LOGIC
9                       );
10  end exor_gate;
11   --Dataflow model
12
13  architecture behav1 of exor_gate is
14  begin
15
16   Z<= x xor y; --Signal Assignment Statement
17
18  end behav1;
```