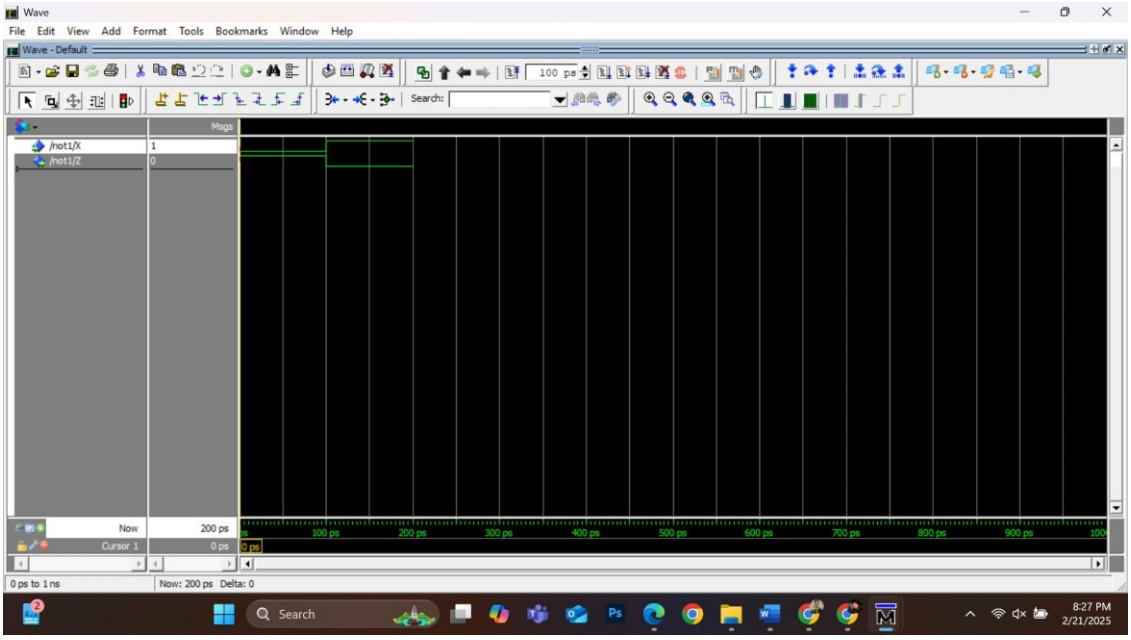
PACO, ARMIN R.
BSCpE – 3A

1.LOGIC GATES

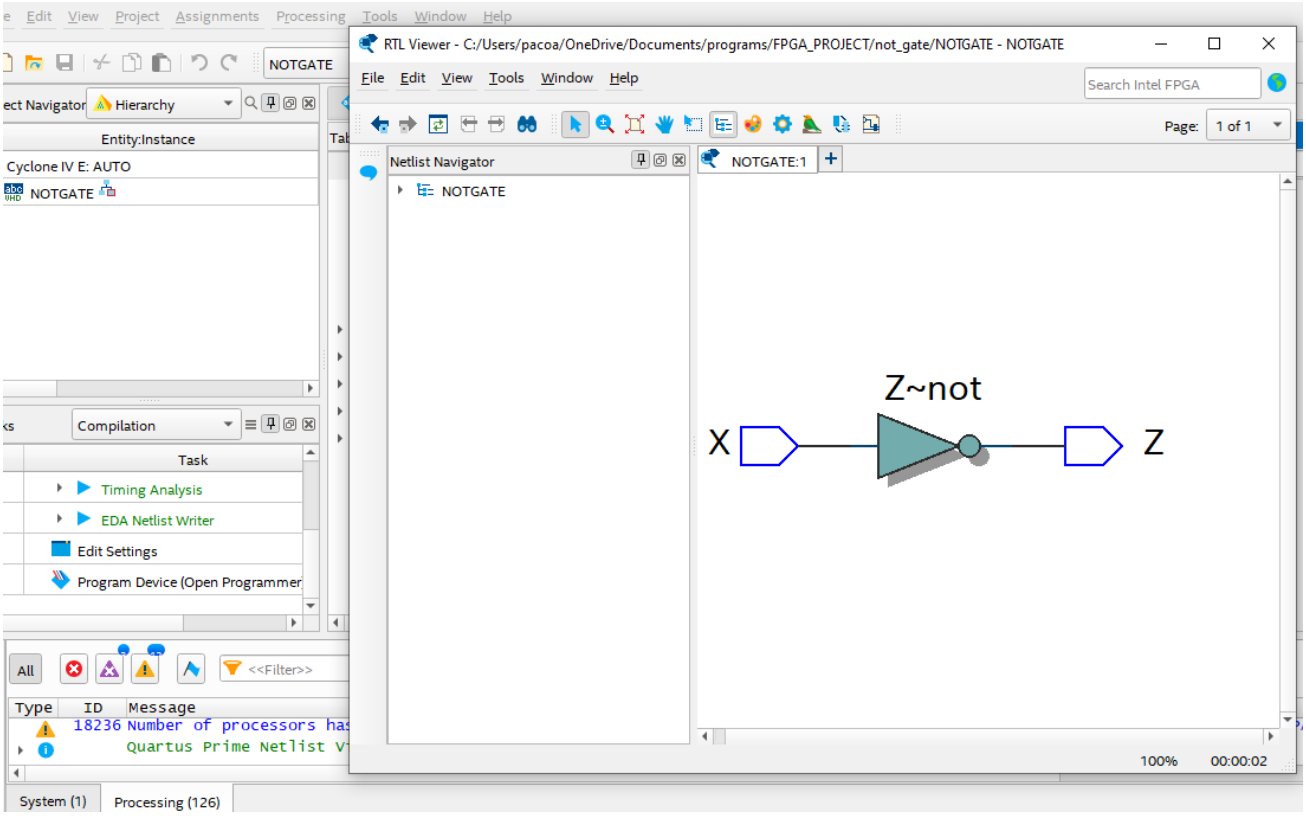
AIM: Write a VHDL code for all the logic gates.

#3-TITLE: NOT gate

OUTPUT WAVE FORM:



RTL VIEW:



CODE: