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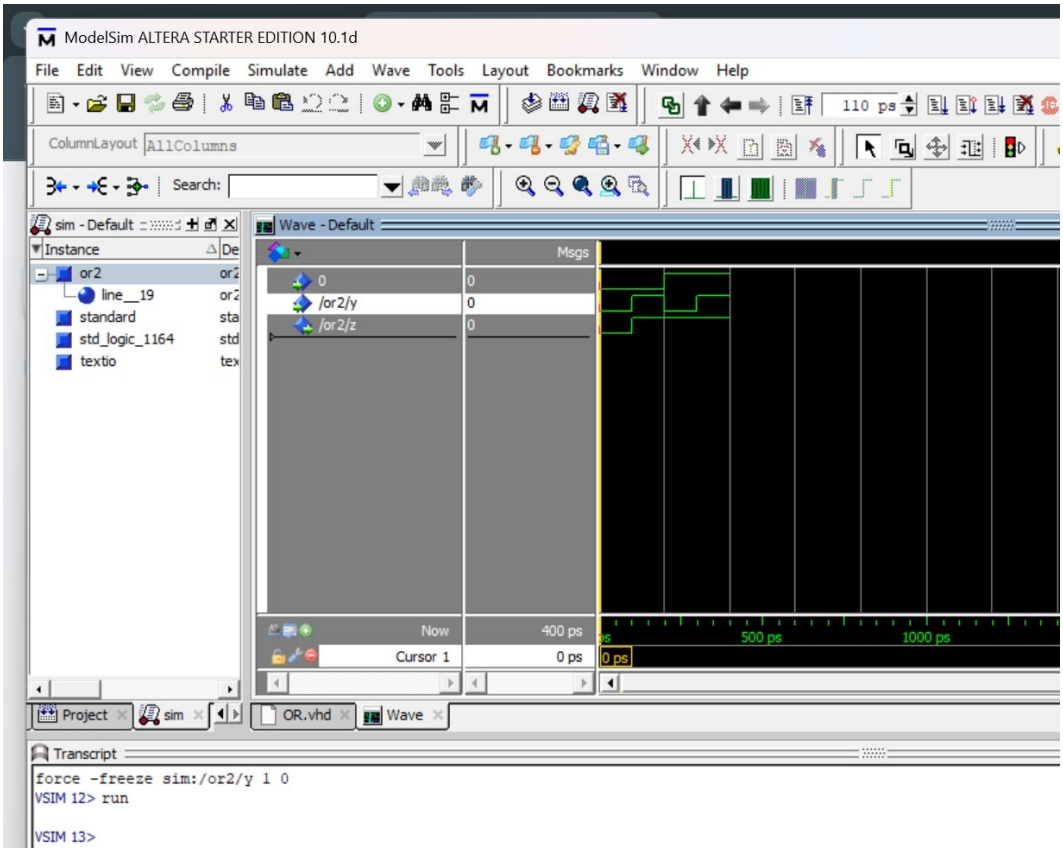
BSCpE – 3A

1.LOGIC GATES

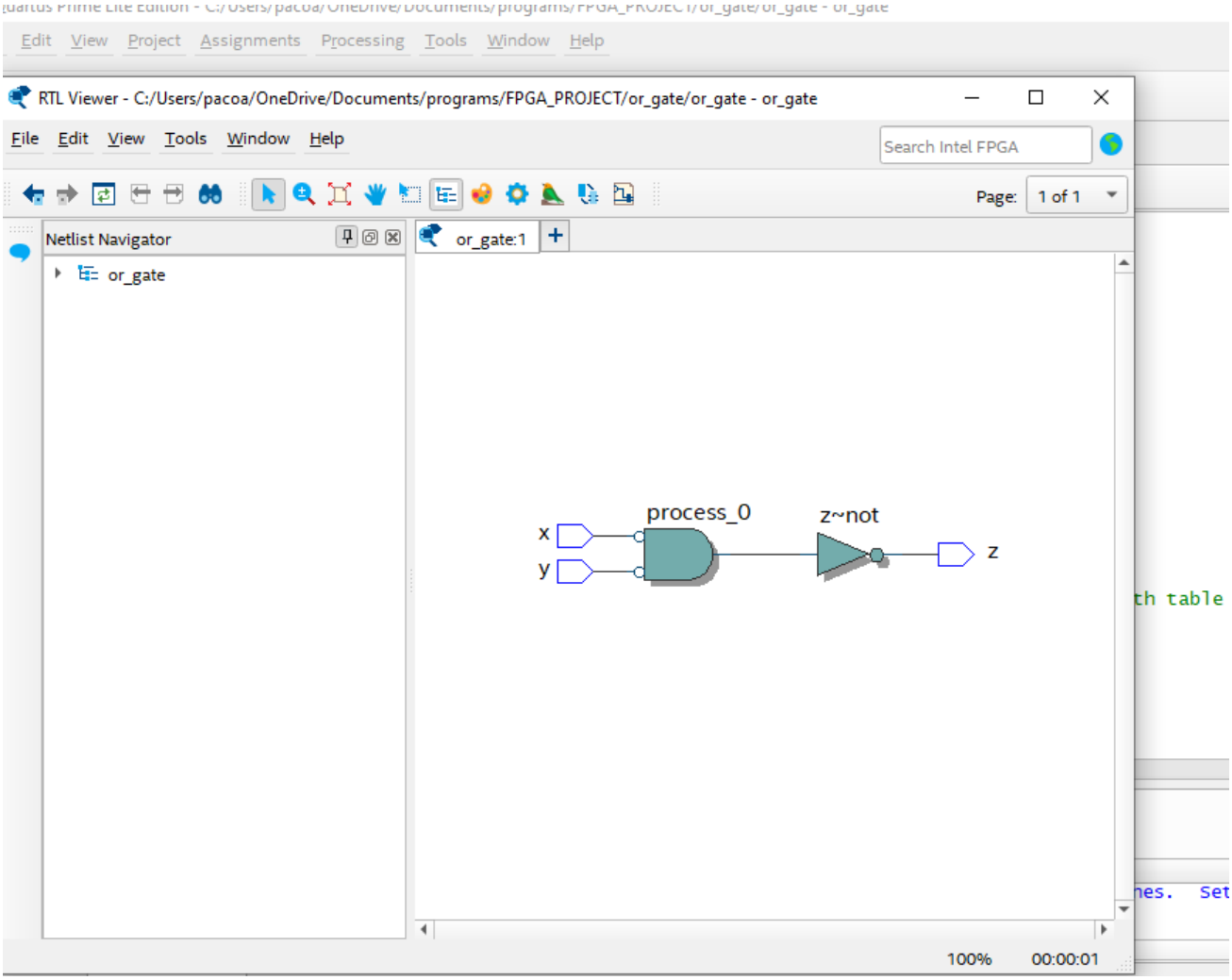
AIM: Write a VHDL code for all the logic gates.

#2-TITLE: OR gate

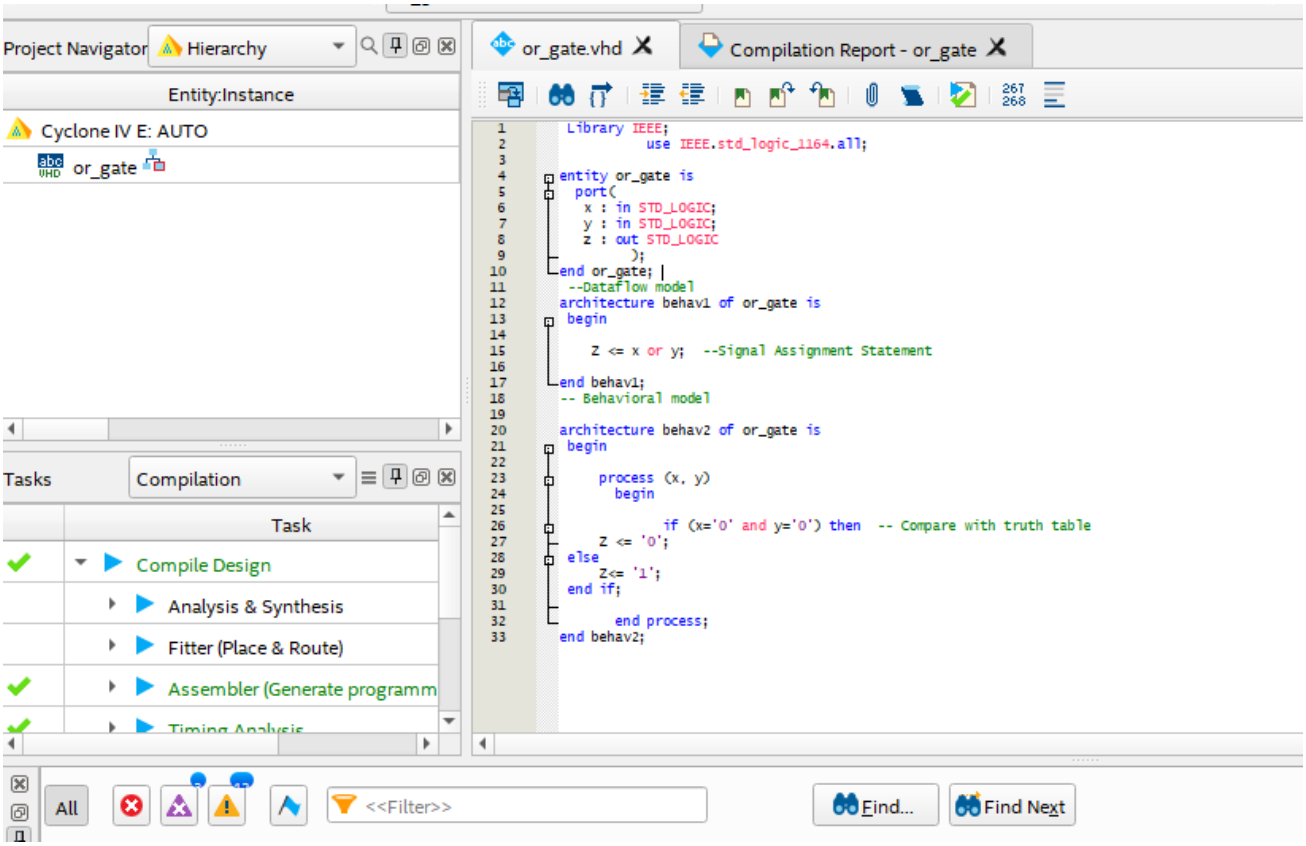
OUTPUT WAVE FORM:



RTL VIEW:


Edit View Project Assignments Processing Tools Window Help
RTL Viewer - C:/Users/pacoa/OneDrive/Documents/programs/FPGA_PROJECT/or_gate/or_gate - or_gate
File Edit View Tools Window Help
Search Intel FPGA
Page: 1 of 1
Netlist Navigator
or_gate
or_gate:1
process_0
z~not
x
y
z
100%
00:00:01

CODE:




```
1   Library IEEE;
2             use IEEE.std_logic_1164.all;
3
4   entity or_gate is
5     port(
6       x : in STD_LOGIC;
7       y : in STD_LOGIC;
8       z : out STD_LOGIC
9           );
10  end or_gate;
11    --Dataflow model
12  architecture behav1 of or_gate is
13   begin
14
15      Z <= x or y;  --Signal Assignment Statement
16
17  end behav1;
18  -- Behavioral model
19
20  architecture behav2 of or_gate is
21   begin
22
23      process (x, y)
24        begin
25
26              if (x='0' and y='0') then  -- Compare with truth table
27      Z <= '0';
28  else
29        Z<= '1';
30  end if;
31
32        end process;
33  end behav2;
```