Ramesh Ganapam

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ACADEMIC DETAILS

University of Kansas Aug 2021 - Present
PhD in Electrical and Computer Engineering *Current GPA: 3.8/4.0*
Area: Computer Architecture and VLSI Design
Advisor: Dr. Mohammad Alian

Birla Institute of Technology And Sciences, Pilani (BITS Pilani) Aug 2016 - May 2018
Master of Engineering *CGPA: 7.64/10.0*
Area: Wireless Communications and Minor in VLSI Design

Jawaharlal Nehru Technological University, Kakinada (Affiliated) Aug 2010 - May 2014
Bachelor of Technology in Electronics and Communication Engineering *Aggregate: 74.6 %*

Relevant Coursework

Modern Computer Architecture Design, VLSI Design, Digital Circuit Design, Analog Circuit Design, CMOS Device Physics, Electrical Networks, Operating Systems, Random Signals and Noise, Introduction to Machine Learning, Wireless Communications, Digital Signal Processing.

Skills

Languages: C/C++, Verilog, Matlab, Python

Tools: LTSpice, Cadence Virtuoso, Micron power models, Cacti, DRAMSpec, Rambus power model, Git/GitHub, Linux, LaTeX

Projects

Open-Source DRAM Circuit Chip Modeling Jan 2023 - Ongoing

Tools: *LT spice, 22–nm PTM, Micron power models, Cacti, DRAMSpce, Rambus power model*

- **Motivation:** Currently, there is no accurate open-source DRAM circuit chip available for the computer architecture community. This project aims to fill that gap.
- **Contribution:** Modeling modern DRAM architecture that utilizes bank group interleaving.
- Modeling the DRAM data path for effective DRAM cycle time calculation.
- Modeling DDR4 DRAM for *latency*, *area*, and *power* calculations for both existing and novel architectures.
- Using Near-Memory Processing to analyze the pros and cons of ALU placement at various locations on the DRAM Die.
- I have formulated an area calculation model for DRAM based on input technology parameters.

Design a Full adder with reduced Transmission Delay Aug 2016 - Dec 2016

Tools: *Cadence Virtuoso, DRC*

- **Goal:** Design a Full Adder (Carry, Sum) using a transmission gate with minimum number of CMOS gates.
- Analyzed static power dissipation of the circuit.
- Performed area analysis using Design Rule Checking (DRC).

Optimal Scheduling of URLLC and eMBB Users with DQN Agent Aug 2021 - Aug 2022

Tools: *NS-3, NS-3-Gym, C++*

- **Goal:** Maximize data rate for both user types while ensuring URLLC user delay requirements are not violated.
- Scheduler uses channel state information estimated using belief values.
- Belief values are estimated using probability theory.

Design of a Generalized Template for Filter Design Aug 2016 - Nov 2016

Tools: *Matlab*

- **Goal:** Model IIR and FIR filters (type-1, type-2, type-3, type-4) based on user-input filter type and order.
- Design filters with outputs including magnitude response, phase response, and poles and zeros locations in the z-plane.

Effect of Noise and Reverberation on Vowel Identification Feb 2017 - Mar 2017

Tools: *Matlab*

- Analyzed and estimated vowel formants using various transform techniques from Digital Signal Processing.
- Analyzed the impact of noise on vowel fundamental frequency and formant identification using the above methods.
- Conducted transform analysis on reverberated vowels and studied the effect of reverberation on vowel fundamental frequency and formant identification.

Modeling and Performance Analysis of Ultrawideband Communication System Jan 2017 - May 2017

Tools: *Matlab*

- **Aim:** Build a system with improved error resilience and higher data transmission rates.
- Modeled wireless communication system with components including Source Coding, Channel Coding, Modulator, Channel model (AWGN), and Receiver model (correlation mask receiver).
- Analyzed average symbol error probability in relation to source power.
- Studied average spectral efficiency and its upper bound as functions of source power for a single relay cooperative network.
- Simulated Average Symbol Error Probability (ASEP) across various source power levels for a single relayed system with diversity link.

Work Experience

Silicon Labs - Baseband Design Engineer - Full time Dec 2018 - Jan 2020

Tools: *Matlab, Verilog, C* | **Hardware:** *Vector Signal Generator, Vector Signal Analyzer*

- Obtained strong knowledge of the 802.11ax draft.
- Prepared functional and performance test cases (sanity check) for 802.11ax, including SU, MU, ER, and TB.
- Implemented the FFT algorithm using the radix-4 algorithm.
- Simulated 802.11ba Tx waveform in Matlab and Verilog.
- Performed overnight regressions for Bluetooth code improvements.
- Simulated the range extension of BLR 125 kbps Bluetooth waveform using a random signal waveform.

CISCO India - Software Developer - Intern Jan 2018 - Jun 2018

Tools: *C, Python*

- Conducted white box unit testing for the CISCO NRS component on a Moonshine platform and the TTY/VTY component on an NCS 5500 platform.
- Wrote the test cases and automated them.

Recognition and Leadership

WORKSHOP | ***Non-Traditional Computing Paradigms with Emerging Technologies for Energy Efficiency - ISSCC***

- Future direction of processing in memory with an emphasis on advantages and disadvantages.
- Emphasis on the cross-layer approach to perform energy efficiency computing.
- Advancing Ising accelerator for Combinatorial Optimization using PIM.

POSITIONS OF RESPONSIBILITY

- Worked as a Teaching Assistant in the Department of Electrical and Computer Engineering at the University of Kansas for the courses - *Introduction to Python* and *Electronics and Digital Circuits Design.*
- Worked as a Teaching Assistant in the Department of Electrical and Electronics at BITS Pilani for the course - *Analog Circuit Design.*

ACHIEVEMENTS AND AWARDS

- Recipient of the student travel grant for the ISPASS-2023 conference.
- Received the MHRD scholarship and Teaching Assistantship during the Master's program at BITS Pilani.