Ramesh Ganapam

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ACADEMIC DETAILS

Florida International University - GRA — Aug 2024 - going on
PhD in Computer Science — *Current GPA: 3.67*
Area: Processing-in-Memory for Digital Logic Synthesis
Advisor: Dr. Sumit Kumar Jha

University of Kansas - (GRA and GTA) — Nov 2022 - Jul 2024
PhD in Electrical and Computer Engineering — *Current GPA: 3.8/4.0*
Area: Computer Architecture and VLSI Design

Birla Institute of Technology And Sciences, Pilani (BITS Pilani) - TA — Aug 2016 - May 2018
Master of Engineering — *CGPA: 7.64/10.0*
Area: Wireless Communications and Minor in VLSI Design

Jawaharlal Nehru Technological University, Kakinada (Affiliated) — Aug 2010 - May 2014
Bachelor of Technology in Electronics and Communication Engineering — *Aggregate: 74.6 %*

Relevant Coursework

Analysis of Algorithms, Machine Learning Algorithms, Hardware Synthesis, Modern Computer Architecture Design, VLSI Design, Digital Circuit Design, Analog Circuit Design, CMOS Device Physics, Electrical Networks, Random Signals and Noise, Wireless Communications, Digital Signal Processing.

Skills

Languages: C/C++, Verilog, Matlab, Python

Tools: LTSpice, Cadence Virtuoso, Micron power models, Cacti, DRAMSpec, Rambus power model, Git/GitHub, Linux, LaTeX

Projects

Digital Logic Synthesis Using Processing-in-Memory on Crossbars (ICCAD 2025 - Planned) Aug 2024 - Ongoing
Tools: *Python,ABC*

- **Motivation:** The increasing volume of data necessitates performing computations using non-von Neumann architectures.
- **Contribution:** This project focuses on synthesizing Boolean logic and intelligently mapping it to the *RRAM* memory crossbar.

Open-source DRAM Circuit Model for Future Memory Systems (ISPASS 2025 - Rebuttal) Jan 2023 - Aug 2024
Tools: *LT spice, PTM models, Micron power models, Cacti, DRAMSpce, Rambus power model, Cadence Virtuoso, GPDK 45 nm*

- **Motivation:** Currently, no accurate open-source DRAM circuit chip is available for the computer architecture community. This project aims to fill that gap.
- **Contribution:** I worked on accurately modeling the *data path* from the DRAM cell to the entire chip, which is often missing in most architectural papers.
- Modeled an accurate access transistor with proper I_{on} and I_{off} currents, addressing gaps in DRAM circuit design models using PTM models.
- Developed the DRAM *background* section, covering data read/write paths and timing diagrams.

An open-source DRAM area modelling (continuation of the above project) Apr 2024 - Aug 2024
Tools: *Cacti, Python*

- **Goal:** To provide an accurate DRAM area model using real DRAM chip data.
- The model provides accurate DRAM area estimates with higher accuracy than existing models and calculates the area overhead for novel DRAM architectures as well as existing architectural combinations of DDR4 memory.
- The model supports upscaling and downscaling between 45, 32, 23, and 16 nm technologies.

Design a Full adder with reduced Transmission Delay Aug 2016 - Dec 2016

Tools: *Cadence Virtuoso, DRC*

- **Goal:** Design a Full Adder (Carry, Sum) using a transmission gate with minimum number of CMOS gates.
- Analyzed static power dissipation and performed area analysis of the circuit using Design Rule Checking (DRC).

Optimal Scheduling of URLLC and eMBB Users with DQN Agent Aug 2021 - Aug 2022

Tools: *NS-3, NS-3-Gym, C++*

- **Goal:** Maximize data rate for both user types while ensuring URLLC user delay requirements are not violated.
- The scheduler utilizes channel state information estimated through belief values derived from probability theory.

Design of a Generalized Template for Filter Design Aug 2016 - Nov 2016

Tools: *Matlab*

- **Goal:** Developed IIR and FIR filters (Type-1 to Type-4) based on user-defined specifications, generating magnitude and phase responses, as well as pole-zero plots in the z-plane.

Effect of Noise and Reverberation on Vowel Identification Feb 2017 - Mar 2017

Tools: *Matlab*

- Analyzed vowel formants and fundamental frequency using various Digital Signal Processing transform techniques, evaluating the impact of noise and reverberation on formant identification and frequency estimation.

Modeling and Performance Analysis of Ultrawideband Communication System Jan 2017 - May 2017

Tools: *Matlab*

- **Aim:** Build a system with improved error resilience and higher data transmission rates.
- Modeled and simulated a wireless communication system with components like Source Coding, Channel Coding, Modulator, AWGN Channel, and Receiver, evaluating Average Symbol Error Probability (ASEP) at different source power levels.
- Studied the relationship between source power, average spectral efficiency, and its upper bound in a single-relay cooperative network with diversity links.

Work Experience

Silicon Labs - Baseband Design Engineer - Full time Dec 2018 - Jan 2020

- **Tools:** Matlab, Verilog, C | **Hardware:** Vector Signal Generator, Vector Signal Analyzer
- Gained strong knowledge of the 802.11ax draft and prepared functional and performance test cases, including sanity checks for SU, MU, ER, and TB scenarios.
- Implemented the FFT algorithm using the radix-4 algorithm.
- Simulated 802.11ba Tx waveform in Matlab and Verilog.
- Simulated the range extension of BLR 125 kbps Bluetooth waveform using a random signal waveform.

CISCO India - Software Developer - Intern Jan 2018 - Jun 2018

- **Tools:** C, Python
- Conducted white-box unit testing and wrote automated test cases for the CISCO NRS component on the Moonshine platform and the TTY/VTY component on the NCS 5500 platform.

Recognition and Leadership

WORKSHOP | ***Non-Traditional Computing Paradigms with Emerging Technologies for Energy Efficiency - ISSCC***

- Explored the future direction of processing in memory with a focus on its advantages, disadvantages, and a cross-layer approach for energy-efficient computing.

POSITIONS OF RESPONSIBILITY

- Worked as a Teaching Assistant for courses including *Introduction to Python*, *Electronics and Digital Circuits Design*, and *Analog Circuit Design* at the University of Kansas and BITS Pilani.

ACHIEVEMENTS AND AWARDS

- Recipient of the student travel grant for the ISPASS - 2023 conference.
- Received the MHRD scholarship and Teaching Assistantship during the Master's program at BITS Pilani.