4x.3 Transresistance Amplifiers

We introduced the basic current-to-voltage, or *transresistance*, amplifier configuration in §4.3.1: an op-amp with feedback resistor R_f converts an input current I_{in} at the summing junction to an output voltage $V_{out} = -R_f I_{in}$. It is called transresistance because its "gain" (output/input) has units of resistance: Gain $= V_{out}/I_{in} = R_f$. (You often see the term "transimpedance" and "TIA" used instead, perhaps suggesting that you ought to be worrying about more general feedback circuits, and phase shifts; but in the real world people design these things as simple current-to-voltage amplifiers, and so we often say "transresistance amplifier," or "current-to-voltage amplifier.")

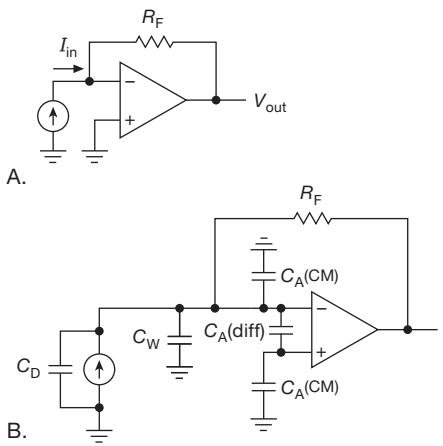


Figure 4x.16. Transresistance amplifiers. A. Basic circuit. B. Including real-world parasitic input capacitances.

4x.3.1 Stability problem

The basic transresistance amplifier is shown again in Figure 4x.16A, and with real-world complications in Figure 4x.16B. The problem with the simple circuit is, simply, that it will probably oscillate! That's because photodiodes (and other detectors, or current-output devices in general) have some intrinsic capacitance C_D, and this capacitance at the input forms a lowpass filter with R_f (with -3 dB "breakpoint" $f_{RCin} = 1/2\pi R_f C_D$), hence a lagging phase shift that approaches $-90°$ well beyond f_{RCin}. That's often well below the op-amp's gain–bandwidth product f_T, so the effect is to add nearly 90° of lagging phase shift to the feedback path, augmenting the op-amp's 90° (or greater) lagging internal phase shift. The situation is shown in the Bode plot of Figure 4x.17, where the feedback network contributes a second pole that increases the roll-off to 12 dB/octave, and the phase shift to $-180°$, at a frequency where the loop gain is still greater than unity; and it crosses the unity gain axis with still greater slope. That's the prescription for oscillation.

Note, by the way, the additional capacitances from the summing junction to ground shown in Figure 4x.16B: the op-amp's input capacitance (both differential and common-mode), and wiring capacitance. For the purposes of circuit behavior, they're all in parallel: $C_{in} = C_D + C_A + C_W$. Which capacitance dominates the sum depends on the size of the detector, the op-amp's internal input circuit, and the wiring. With a fast, small-geometry detector, the op-amp's input capacitance may well dominate; whereas a large-area detector's capacitance is likely to dominate (unless significant lengths of shielded cable are used with a remote detector). As we'll see shortly, the more capacitance you have, the poorer the performance (in terms of speed and noise). So it's always best to avoid adding significant capacitance, where possible. For example, if your detector is some distance from the rest of your circuit, it is often a good idea to put the transresistance preamp right at the detector, bringing the amplified voltage output back through shielded cable; this also has the advantage of minimizing noise pickup on the low-level, high-impedance input signal via capacitive and inductive pickup, ground loops, and the like. Also, detector capacitance decreases markedly with increasing applied back-bias, so speed is improved (but leakage current is introduced) by returning the detector common terminal to a quiet (i.e., well bypassed) bias supply instead of ground (Figure 4x.18).

4x.3.2 Stability solution

The simplest solution to this problem is to put a small parallel compensation capacitance C_f across the feedback resistor, as in Figure 4x.19. It's easiest to understand what's going on with a Bode plot (Figure 4x.17). C_f stops the 6 dB/octave roll-off of the feedback network at frequency $f_c = 1/2\pi R_f C_f$ (that's where the magnitude of C_f's reactance equals R_f, and is roughly the roll-off response frequency of the amplifier), which makes the overall roll-off of loop gain revert to its original 6 dB/octave slope (and corresponding 90° lagging phase shift). (In official jargon this is known as putting a "zero" into the feedback network.) The trick is to choose C_f so that the resulting closed-

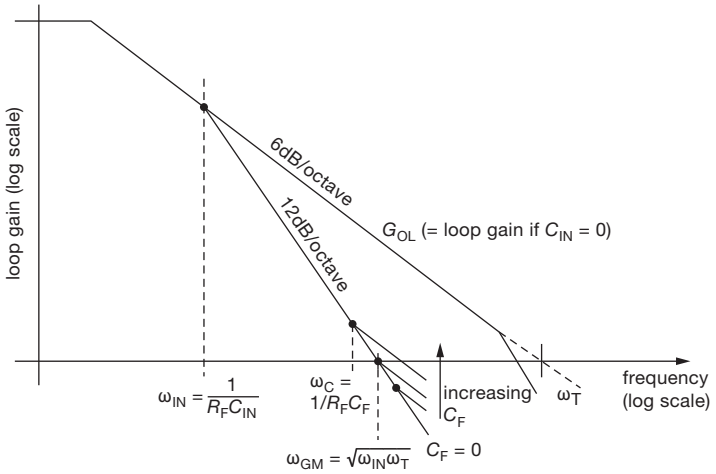


Figure 4x.17. Bode plot (log magnitude of gain vs log frequency for the transresistance amplifier). For stability the closed-loop gain curve must intercept the unity-gain axis at a 6 dB/octave slope.

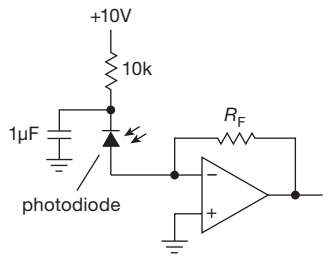


Figure 4x.18. Reverse biasing a photodiode decreases capacitance and increases speed (but at the expense of "dark current"). Be sure to use a clean, bypassed bias supply; choose the series resistor so that the drop across it is small compared with the bias voltage, at the maximum anticipated photodiode current.

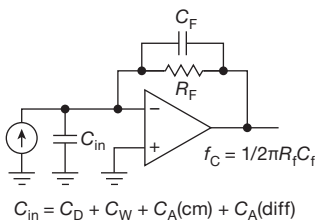


Figure 4x.19. Transresistance amplifier with stabilizing feedback capacitor C_f.

loop gain plot (Figure 4x.17) has reverted safely back to 6 dB/octave somewhat before reaching the unity gain axis.

Here's how you do it: First note that the unstabilized amplifier has the loop gain crossing the axis halfway (logarithmically) between $f_{RC\text{in}}$ and f_T; that is, at a frequency[9] that is the geometric mean:

$$f_{GM} = \sqrt{f_{RC_{in}} f_T}. \tag{4x.1}$$

If we were to choose C_f so as to put f_c at that frequency, we would be living dangerously – the loop gain plot would be in the midst of reverting to 6 dB/octave as it crossed the unity gain axis; to state things more accurately, the phase shift of the feedback network would have dropped to 45°, as *RC* circuits always do at their 3 dB points. The result would be an amplifier that is probably stable in the sense of not oscillating, but it might exhibit overshoot and ringing following a transient; and its closed-loop frequency response would exhibit "peaking," specifically a bump of about 1.3 dB near the unity-gain crossing frequency f_{GM} (we'll call this response trace f_a).

So, we choose C_f a bit larger. A common procedure is to choose C_f so that $f_c = 1/2\pi R_f C_f = \sqrt{f_{RC\text{in}} f_T/2}$, i.e., at about 70% of the geometric mean. This generally ensures good stability, and produces a closed-loop response that is maximally flat (actually, a second order Butterworth, see Chapter 6), without any peaking, and is down 3 dB at f_{GM} (Figure 4x.20). You'll often see a parameter called the "damping ratio," with the symbol ζ (zeta). The choice

$$f_c = 0.7 f_{GM} \tag{4x.2}$$

[9] An op-amp's f_T is the extrapolated frequency at which the log–log curve of open-loop gain versus frequency crosses the unity gain axis, extended from a lower frequency where there is plenty of gain and where the slope is 6 dB/octave (i.e., $\propto 1/f$). On datasheets this is usually called the gain–bandwidth product, GBW.

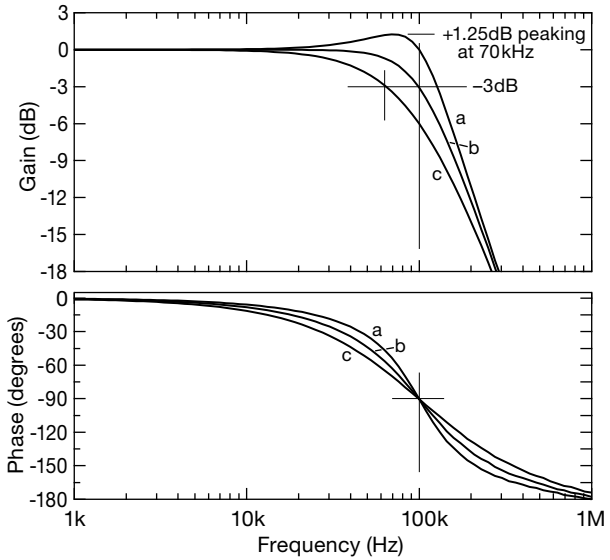


Figure 4x.20. TIA frequency response (normalized transresistance gain and phase vs frequency) for three choices of C_f, namely those corresponding to characteristic frequencies $f_c = 0.7 f_{GM}/\zeta$, with the damping ratio ζ equal to (a) 0.7, underdamped, (b) 1.0, critically damped, and (c) 1.4, overdamped. This SPICE-modeled transimpedance amplifier's bandwidth is 100 kHz; the convergence in gain at high frequencies is controlled by the op-amp, with a slope of 12 dB/octave.

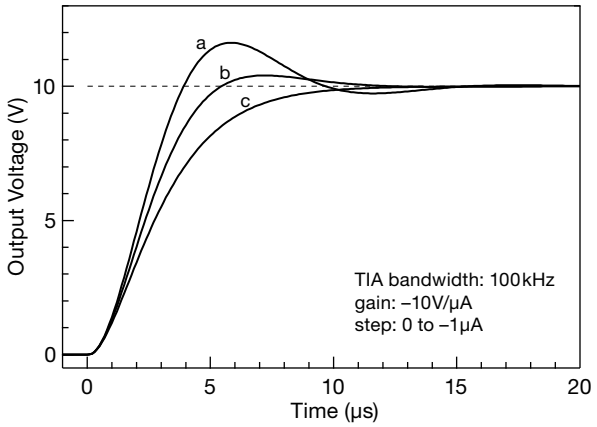


Figure 4x.21. TIA step response for the same three choices of C_f as in Fig. 4x.20.

corresponds to a damping ratio $\zeta = 1$.

If C_f is chosen still larger, it produces an overall amplifier bandwidth at a lower frequency (which we'll call f_b) equal to the roll-off frequency of the *RC*, i.e., $f_b = f_c = 1/2\pi R_f C_f$; the corresponding frequency response exhibits the usual slow roll-off characteristic of a single *RC* lowpass (a single "on-axis pole," Figure 1.104), with the familiar *RC* step response (Figure 1.34). But if C_f is chosen for maximally flat response (i.e., $f_c = 0.7 f_{GM}$), the result is to introduce just the right amount of "peaking" to extend the amplifier's response to $f_b = f_{GM}$, and to speed the step response so it smartly moves to the new output voltage with minimal overshoot (Curve b of the SPICE results in Figures 4x.20 and 4x.21, and seen in the measured $C_f = 2.4$ pF waveform of Figure 4x.26).[10]

It's customary to define the bandwidth of an amplifier by measuring the frequency at which the gain has fallen by 3 dB. But this simple measure does not take into account the possibility of overdamping, gain peaking due to underdamping, etc. The figure shows that an underdamped amplifier appears to have more bandwidth. One useful approach to determining bandwidth is to measure the frequency at which the phase shift reaches $-45°$. This is particularly relevant if the amplifier is used inside a feedback loop, e.g., in a scanning tunneling microscope preamp (see §8.11.12). Measured in this way,[11] an underdamped amplifier has more bandwidth, and an overdamped amplifier has less. As an example, here are SPICE results for the -3 dB and $-45°$ frequencies of a sample TIA with $f_c = 100$ kHz:

	damping, ζ	$f_{-3\,dB}$	$f_{-45°}$
a	0.7	129 kHz	62.7 kHz
b	1.0	100 kHz	51.5 kHz
c	1.4	66 kHz	40.8 kHz

4x.3.3 An example: PIN diode amplifier

As an example, let's design a photodiode amplifier for use with a typical silicon PIN diode of 5 mm^2 active area. These popular devices come in a TO-5 transistor package with glass window, and are meant to be operated with a back bias of 10 V to 20 V. Examples are the S1223 from Hamamatsu and the PIN-5D from UDT, with closely similar characteristics: terminal capacitance $C_D = 10$ pF at 20 V back bias, cutoff frequency (3 dB down) $f_c = 30$ MHz (corresponding to a rise time $t_r \approx 0.35/f_c = 12$ ns), and a red-weighted visible-light response rising to a maximum close to 1 μm wavelength.

A comment on detector speed: The rise time specification tells you the "datasheet speed" of the detector (usually specified for some wavelength of incident light, and with

[10] In the language of "root locus" in the *s*-plane, one would say that a single on-axis dominant pole has morphed into a pair of off-axis poles.

[11] That is, ignoring other aspects such as settling time, ringing, and the like.

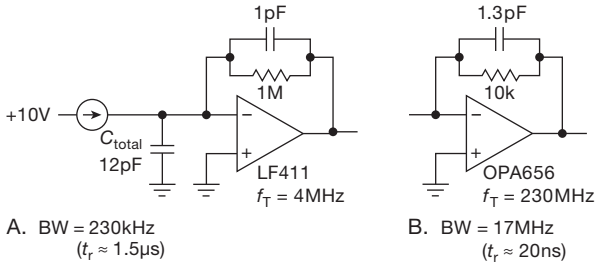


Figure 4x.22. Photodiode amplifier examples. A. Using jellybean LF411 (f_T=4 MHz), with G=1 V/μA. B. Using wideband OPA656 (f_T=230 MHz), with G=10 mV/μA.

some standard load resistance, usually 50 Ω); it depends on the detector's capacitance (which forms an *RC* time constant with the load resistance), and also upon the physics of charge carrier transit time in the detector itself (which in turn depends on semiconductor properties, junction geometry, and applied bias voltage). Depending upon your circuit, you may or may not achieve that "50 Ω–load" detector speed.[12] As we'll see, achieving adequate bandwidth may be harder than you think!

Let's arbitrarily choose the transresistance gain (V_{out}/I_{in}) to be 1 MΩ; that becomes the value of the feedback resistor: $R_f = 1\,\text{M}\Omega$. We'll see shortly that this is not a wise choice, if we care about speed. For the op-amp let's start with our standard jellybean LF411, with a gain–bandwidth product $f_T = 4$ MHz (typ). The amplifier datasheet gives no information about input capacitance, but it's probably safe to guess a value of about $C_A = 2$ pF, giving a total input capacitance $C_{in} = C_D + C_A = 12$ pF. In combination with the 1 MΩ feedback resistor, this produces a roll-off beginning at $f_{RCin} = 13$ kHz.

Next we calculate the value of feedback capacitor C_f to ensure stable operation. The geometric mean of f_{RCin} and f_T is $f_{GM} = 2.3 \times 10^5$ Hz. For optimum transient performance and good stability, we now choose C_f so that its characteristic frequency, in combination with the existing R_f, is 70% of that value: $1/2\pi R_f C_f = 0.7 f_{GM}$, giving $C_f = 1.0$ pF. The resulting amplifier has a 3 dB bandwidth of $f_b = 230$ kHz, (equal to f_{GM}), and a rise time of approximately $t_r \approx 0.35/f_b = 1.5\,\mu$s. (Figure 4x.22A)

A. Gaining speed

Our amplifier's bandwidth is only 1% of the detector's datasheet speed! And we got only 230 kHz response, even though we used a 4 MHz op-amp. What's going on here? There are two problems, actually: The large feedback resistor formed a very low frequency roll-off (at 13 kHz) with the input capacitance; and the final bandwidth is the geometric mean of that with op-amp's modest f_T.

Let's try a faster amplifier: The low-noise JFET-input OPA627 (a JFET version of the popular low-noise bipolar OP-27) has an f_T of 16 MHz, which sounds like it should help. However, it also has a total input capacitance of $C_A = 15$ pF (the sum of 8 pF of differential input capacitance and 7 pF of common-mode input capacitance), which pushes the input roll-off down to 6.4 kHz.[13] If you go through the design procedure as above, you'll find that $C_f = 0.7$ pF, and the 3 dB bandwidth of the completed amplifier is $f_b = f_{GM} = 320$ kHz, a minor improvement over our first design.

We can improve things by using an OPA637, which is a decompensated OPA627 (G_{min}=5). Note an important fact: it's not necessary to use unity-gain compensated op-amps in a transresistance configuration if the op-amp's second breakpoint (its "second pole," the frequency at which its open-loop gain begins dropping at 12 dB/octave) is well above f_c. The OPA637's f_T of 80 MHz allows us to extend f_c from 320 kHz to a more respectable 715 kHz. But we're still suffering from the penalty of the op-amp's high input capacitance.

B. "Pedal to the metal"

OK, let's really step on the gas: The high-speed JFET-input OPA656 has an f_T of 230 MHz, and total input capacitance of $C_A = 3.5$ pF. Going through the same design procedure, you'll find that f_{RCin} is still 13 kHz (as with the LF411), but the completed amplifier's bandwidth is now $f_b = 1.7$ MHz (with a smaller value of feedback capacitance $C_f = 0.13$ pF – see comments below). This is almost an order of magnitude better speed than our first pathetic attempt (because the op-amp's f_T is nearly 2 orders of magnitude higher); but it's still more than an order of magnitude slower than the detector itself (recall $f_c = 30$ MHz). We can do somewhat better here by using a decompensated op-amp (an OPA657, f_T=1.6 GHz, G_{min}=7), which pushes f_b up to a more respectable 4 MHz. We can't go much further down the path of increasing f_T, certainly not the factor of several hundred that we evidently still need.

One reasonable solution, if full speed is needed, is to trade off noise performance for speed, by reducing the gain

[12] However (looking on the bright side) you may in fact be able to do better (e.g., when the detector is loaded into the low-impedance presented by a good TIA, or when it is bootstrapped).

[13] The higher capacitance is related to the op-amp's lower e_n specification, 4.5 nV/$\sqrt{\text{Hz}}$ versus 25 nV/$\sqrt{\text{Hz}}$; we'll see the important significance of that later.

of the transresistance stage, then follow it with a wideband voltage amplifier. For example, if we reduce the feedback resistor to $R_f = 10\,k\Omega$ (gain of 10 V/mA), we drive the input pole up by a factor of 100, to $f_{RCin} = 1.3\,MHz$. The completed amplifier's resulting bandwidth goes up by the square root of that factor, or a factor of 10, to $f_b = 17\,MHz$; the corresponding value for C_f is 1.3 pF. With this design we are getting most of the detector's speed (and we could do still better with the decompensated OPA657). Whether we can accept the lower gain depends on issues of noise, which are discussed in Chapter 8 (§8.11).

Another interesting solution is to *bootstrap* the detector, greatly reducing the effective input capacitance seen at the TIA's input; we illustrate this important technique in §4x.3.4.

C. Sub-picofarad capacitors

The calculated value of feedback capacitance in our last iteration – $C_f = 0.13\,pF$ – sounds awfully small; can you actually get such capacitors? That's an interesting question, but you might ask first how much "parasitic" capacitance there is between the leads of the feedback resistor itself. We treat this and similar topics in Chapter 1x (properties of components); we have found, by actual measurement, that a standard metal-film resistor ("RN55D-type") has something like 0.07 pF – 0.15 pF of parasitic parallel capacitance, the exact value depending on manufacturer and resistance value. So, you might need to add a tiny bit of capacitance across the resistor, perhaps using a "gimmick," the official term for a pair of short insulated wires that you twist up until there's enough capacitance. When dealing with circuits like this, in which a fraction of a picofarad has important effects, be careful about component placement and lead dress; for example, the feedback resistor (and perhaps the inverting input pin of the op-amp) should be raised up from the circuit board to minimize capacitance to ground and to other signals. You often see similar advice when dealing with ultra-low input currents (femtoamps), namely to float the input leads, or support them on a Teflon standoff insulator.

What should you do if the calculated feedback capacitance comes out *less* than the parasitic capacitance of the feedback resistor? One solution is to reduce the feedback resistor value until the calculated capacitance is about equal to the parasitic capacitance. This reduces the transresistance gain of the amplifier, of course, perhaps requiring additional gain downstream.[14] A clever alternative is

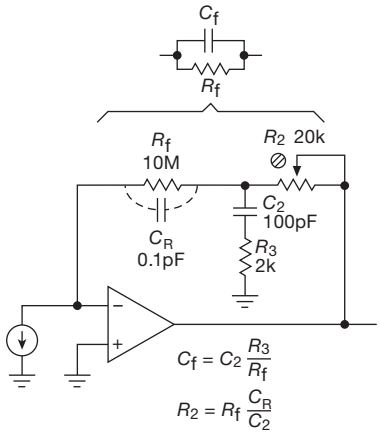


Figure 4x.23. "Pole-zero" trick when the parasitic capacitance C_R of the gain-setting feedback resistor R_f is itself larger than the calculated shunt feedback capacitance.

shown in Figure 4x.23: Here the unavoidable time constant R_fC_R of the feedback resistor with its own parasitic capacitance C_R (a "zero") is canceled by a deliberate lagging time constant R_2C_2 (a "pole"); then the addition of a resistor R_3 reintroduces a zero with time constant C_2R_3. For example, if a certain circuit needed C_f=0.02 pF across a 10 MΩ feedback resistor, we would be in trouble because of the ∼ 0.1 pF of parasitic capacitance. We cancel this by choosing R_2=10k and C_2=100 pF; then we choose R_3=2k, as shown.[15] We haven't seen this trick described elsewhere, but we've used it successfully in several wideband photodiode amplifiers.

Figure 4x.24 shows another trick, helpful when dealing with these small-value compensation capacitors. Here the effective feedback capacitance is the fraction of C_f set by trimmer R_1.

To recapitulate the major results: The "bandwidth" of this properly stabilized current-to-voltage amplifier is far less than the op-amp's gain–bandwidth product f_T. It is, rather, at the geometric mean of that frequency and the (much lower) characteristic frequency set by the time constant of the total input capacitance and the feedback resistor. This shows why input capacitance compromises speed,

[14] It also increases R_f's Johnson noise contribution – see the extensive discussion in Chapter 8 (§8.11).

[15] That is, $R_3C_2 = R_fC_f$, where C_f was the desired feedback capacitance (0.2 pF) appropriate to the gain-setting feedback resistance R_f (10 MΩ). Note how the new effective C_f is well predicted, set by low-tolerance parts. R_2 has to be adjustable, because we don't know the value of the stray capacitance C_R; it should be adjusted for a flat gain response in the crossover region, $f = 1/2\pi R_fC_R$, about 160 kHz in this case, well below the circuit's f_{3dB} bandwidth. Choosing a 20k trimmer for R_2 allows canceling 0 pF to 0.2 pF of stray capacitance C_R.

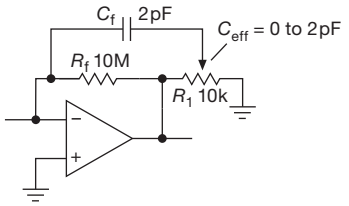


Figure 4x.24. Creating a "tunable" low-value feedback capacitor. The total effective feedback capacitance includes ~ 0.1 pF of stray capacitance of R_f (not shown).

and the surprising need for op-amps that are much faster than you might have guessed. And we'll see presently how input capacitance also degrades noise performance (we saw it initially in Chapter 8 of AoE3 (§8.11.3)).

4x.3.4 A complete photodiode amplifier design

The circuit of Figure 4x.25 should help tie these ideas together.[16] It's the basic design of RIS-617, a photodiode amplifier that has been in wide use in the laboratories at our Rowland Institute. For the transimpedance stage we chose the JFET-input OPA637 (or equivalent ADA4637) for its combination of low input current and low noise voltage (e_n=4.5 nV/$\sqrt{\text{Hz}}$), combined with wide bandwidth (f_T=80 MHz). This op-amp is the decompensated ($G > 5$) version of the unity-gain-stable OPA627 (which has f_T=16 MHz); it's suitable for a transimpedance application like this, owing to the aggressive compensation provided by the external compensation capacitor C_f. And of course that extra bandwidth translates into improved amplifier speed.

Less obvious is the desirability of low op-amp input noise voltage, e_n. At first sight it might seem to be of little concern, perhaps contributing only that quantity of noise voltage at the output. That would be wrong. In fact, as we saw in Chapter 8, the op-amp's e_n grinds up against the input capacitance C_{in} to create an effective input noise current $i_n = e_n \omega C_{in}$ (which we like to call "e_nC" noise). This can easily dominate over all other sources of noise, particularly when you're striving for substantial bandwidth.

In this circuit we chose R_f for a modest first-stage transimpedance gain (0.1 V/μA), with a second stage of selectable voltage gain to set the overall instrument gain. The trade-off is speed (smaller R_f, thus greater $f_{RC\text{in}}$) versus noise (larger R_f, thus less Johnson noise current $i_n = \sqrt{4kT/R_f}$; see §8.11).

In a transimpedance amplifier input capacitance is the villain: it drives down the bandwidth (via necessarily larger C_f), and it drives up the noise (via the input i_n produced by the op-amp's e_n imposed across C_{in}). Because high-performance transimpedance amplifiers are generally expected to work properly with rather large input capacitances[17] (up to 1000 pF), we added a 2-stage bootstrap follower (Q_1Q_2), which reduces the effective input capacitance at signal frequencies by roughly a factor of ten (thus 100 pF maximum). Q_2 is a very low noise (0.8 nV/$\sqrt{\text{Hz}}$) JFET[18] of high transconductance ($\sim$ 25 mS, thus $\sim 40\,\Omega$ output impedance), here buffered by Q_1 for plenty of drive muscle. See §8.11 for more detail.

To figure the compensation capacitor C_f, we take the maximum effective C_{in}=100 pF, for which $f_{RC\text{in}}$=16 kHz, f_c=1.1 MHz, and critical damping ($\zeta = 1$) would require C_f=2.1 pF. The 4 pF shown in the diagram is quite conservative, and produces an overdamped response, as shown in the measured response traces of Figure 4x.26.

The second stage is a wideband voltage amplifier, here implemented with a current feedback (CFB) op-amp. The LT1217 maintains 5 MHz bandwidth at G=10, with decent accuracy (V_{os}=3 mV max) and noise (e_n=6.5 nV/$\sqrt{\text{Hz}}$). The offset trim network is worthwhile, given the 0.5 mV maximum offset of the input stage; you can think of it as a trim of the combined 2-stage offset, if that makes you happier. Both amplifier stages use "high-voltage" op-amps (i.e., $\pm$15 V supplies), permitting output swings to $\pm$10 V.[19]

The lowpass filter R_5C_2 between the stages, with its 300 kHz breakpoint, is important in reducing out-of-band noise. However, as discussed in §8.11.3, we struggle with an ugly current noise whose spectrum rises with frequency. The single lowpass pole introduced at f_c cancels the rising noise density, but still leaves a noise spectrum flat with frequency (although we do benefit from an additional pole at f_{GM}).

Sharper lowpass filter.

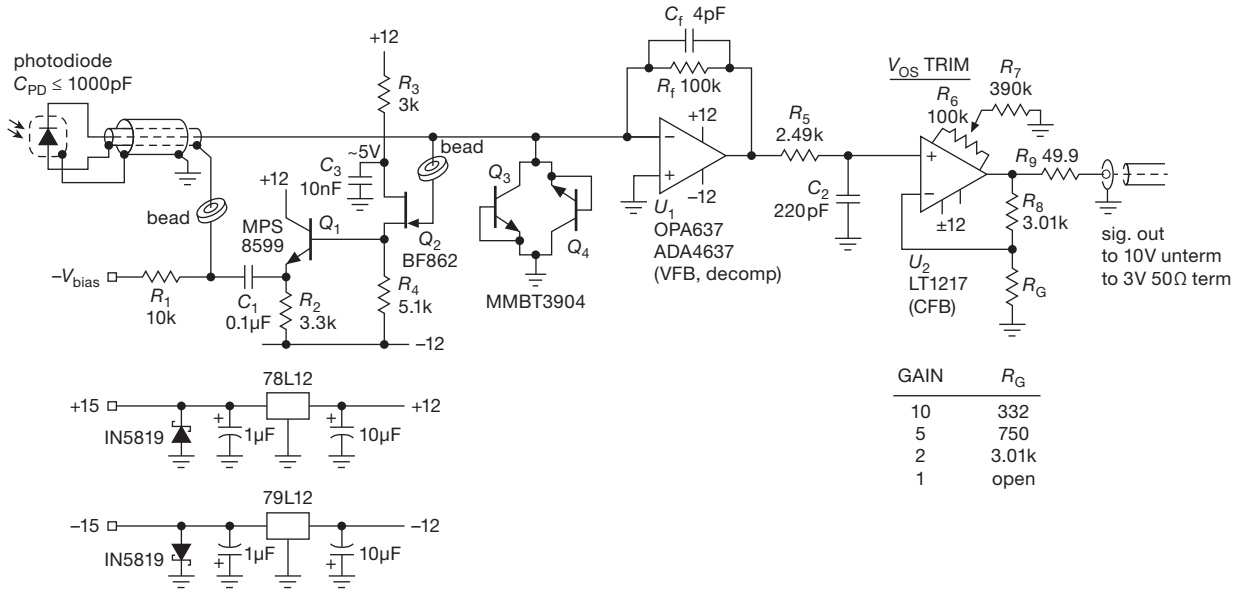
Better, though, to add a steeper lowpass cutoff to limit the rms noise degradation, which we can do by turning U_2 into a second-order filter, with the addition of two parts, see

[16] "That rug really tied the room together . . . "

[17] It's unusual to find a case where the bootstrap isn't a critically important part, the exception being tiny sensors (of the type used for fiber optic receivers).

[18] Sadly *discontinued!* But the CPH3910 from ONSemi is just as good, and available as a dual (CPH3910).

[19] With the photodiode configured to sink current, as shown here, the output will only go positive; but the circuit happily accepts input currents of either polarity.



GAIN	R_G
10	332
5	750
2	3.01k
1	open

Figure 4x.25. A complete photodiode amplifier, suitable for input capacitances up to 1000 pF. Input bootstrapping greatly reduces the effective photodiode and cable capacitance, for enhanced speed and reduced noise.

Figures 4x.27 and 4x.28.[20] The filter's second pole is less effective for gains <10, where however you're dealing with larger signals, thus less sensitivity to noise filtering. From the response curves (Fig. 4x.28) you might initially choose $C_1 = 140$ pF for its pretty curve; but sometimes it's nice to exploit a peaky response (e.g., with $C_1 = 160$ pF) to extend somewhat the response of an amplifier in its rolloff region.

Expensive amplifiers need protection; U_1 will set you back $30 (!), so we added diode clamps Q_3Q_4 (an *npn* base–collector junction is an inexpensive diode of low capacitance and very low leakage; see for example Figure 5.2).

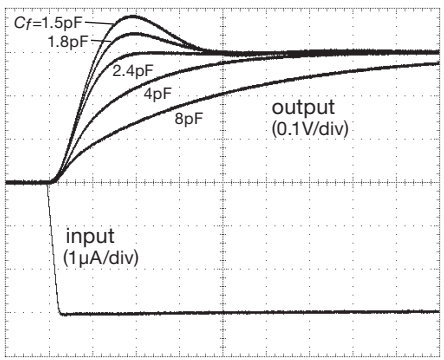


Figure 4x.26. Measured response of the transresistance stage (U_1) of Figure 4x.25 to a current step input, with an input (summing-junction) capacitance of 100 pF, for several values of feedback capacitor C_f. Horizontal: 200 ns/div.

4x.3.5 Gain-switching

The TIA stage in Figure 4x.25 has been set at a fixed gain ($G = v_{out}/i_{in} = -100\,\text{k}\Omega$), with a selection of higher gain steps provided by the 1–2–5–10× voltage-amplifying stage U_2. That's OK – but we could do better if instead we increased R_f to go to higher gain: that's because the (fixed, 100k) low value of R_f introduces more current noise than the alternative of using higher values of R_f when we want more gain.[21]

Figure 4x.29 shows two approaches to finessing this problem. We've used the same $f_T = 80$ MHz op-amp, and we've assumed there's some 25 pF of input capacitance. We should be able to achieve 500 kHz of bandwidth with a gain of 1 MΩ. In circuit A we took the simple solution of a

[20] This is a modification of the VCVS lowpass filter (Fig. 6.28A), in which we've set G=10 and, keeping R_1=R_2, we've chosen the capacitor values to produce a smooth low-Q roll-off to −12 dB/octave. Put another way, we've broken the rules for a VCVS Butterworth lowpass filter: for G=10 choose C_1 and C_2 to be 0.4 and 2.5 times the respective canonical value of $C = 1/2\pi R f_c$. This generalization of the Sallen-and-Key filter was discussed in AoE3's §6.3.2D.

[21] Recall §8.1.1, where resistor current noise is seen to go as $i_n = \sqrt{4kT/R}$.

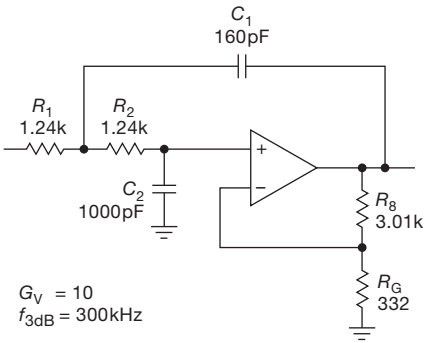


Figure 4x.27. Two-pole lowpass filter with G=10 to replace U_2 in Fig. 4x.25.

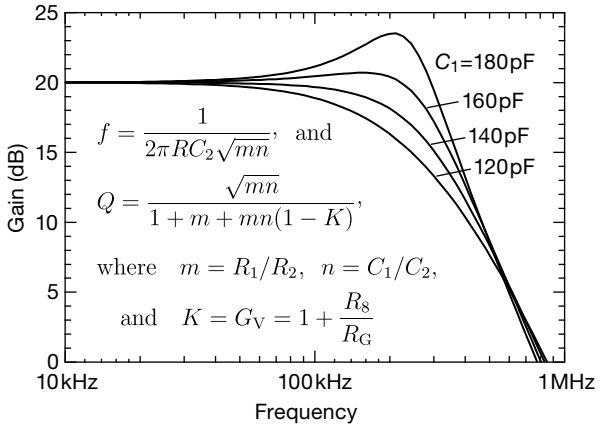


Figure 4x.28. Response of the lowpass filter of Fig. 4x.27, as similated in SPICE. Note the sensitivity to C_1.

3-position (center-OFF) toggle switch to select the feedback resistor, shunted by appropriate small capacitors, to select TIA gains of 10k, 100k, and 1M. But the problem here is that the switch, in the middle (open) position, introduces some 0.5 pF to 1.5 pF of capacitance that effectively shunts R_f, overriding the 0.3 pF that's supposed to be across the 1M feedback resistor (there's about 0.1 pF parasitic capacitance of R_f itself, thus the 0.2 pF explicit capacitor shown). That kills our target 500 kHz bandwidth![22] We might try replacing the toggle switch with a CMOS SPDT switch; but the parasitic capacitance in the OFF state is even worse than the mechanical switch – about 5 pF.

Circuit B is the better solution: here we've used a CMOS switch, wired "backwards" (in current-steering mode),

[22] There is a workaround, of sorts, by adding 10 to 20 pF capacitors to ground at each switch terminal – but this is ugly, loading the 80 MHz op-amp, and it's only a partial solution because there's some capacitive signal leaking through, lowering the gain.

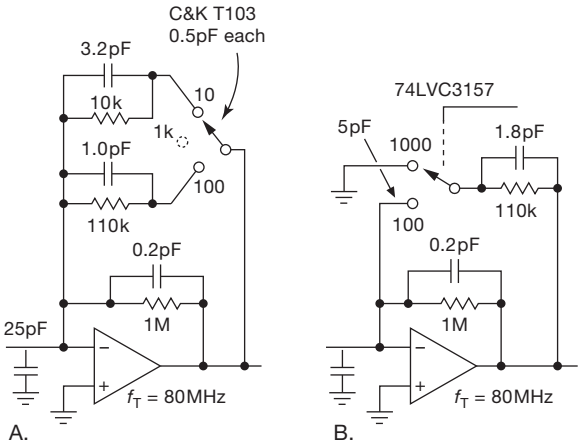


Figure 4x.29. Minimizing bandwidth-killing capacitance while gain-switching the TIA with several values of feedback resistor. Circuit B nicely circumvents the degrading effects of parasitic switch capacitance in circuit A.

with the two signal terminals always at ground potential. They switch *currents* (rather than voltages), a scheme we first encountered in Figure 13.47 in Keysight's "Multislope III" converter. The ground potential means we can use a low-voltage switch, even with high-voltage signals. We chose a '3157-type switch (see §13.8.5 and Table 13.7) for its low capacitance (accepting its moderately high R_{ON}).

In the high-gain position (switch open) we're adding an acceptable 5 pF to the summing junction, while the damaging 100k and 1.8 pF currents are safely shunted to ground. In the low-gain 100k position the switch capacitance increases to 17 pF, forcing us to increase C_f to 1.8 pF, slightly reducing the bandwidth. The 74LVC1G3157 is available in SOT23-6 and SC70-6 packages, the latter small enough to squeeze in at the summing junction. If you want three gain choices with R_f switching, you can add a second switch.

4x.3.6 Some loose ends

- Note that you generally can assume that the op-amp is behaving like a classical 6 dB/octave, 90° lagging phase amplifier; you can take a "single dominant pole" model, in engineer's lingo, and you don't have to worry about additional phase shifts that usually creep in as you approach the op-amp's f_T. That's because the large feedback resistors used in these amplifiers usually put the input pole f_{RCin} at a very low frequency, such that the trouble region at $f_{GM} = \sqrt{f_{RCin} f_T}$ is far below the frequencies at which the op-amp departs from the single-pole model.
- For the same reason – namely that the loop gain is

brought to unity far below the op-amp's f_T – you can safely use *decompensated* op-amps in this circuit, as we did with the OPA637 in our second design attempt. That more than doubled the speed, because it has 5 times greater bandwidth ($f_T = 80\,\text{MHz}$); but it is only stable at closed-loop gains of 5 or greater. A warning, however: if you use decompensated op-amps in this circuit, make sure that the ratio of C_{in} to C_f is greater than the minimum specified closed-loop gain (this will usually be true), because that ratio sets the high-frequency closed-loop gain of the transresistance amplifier. Also note that circuit stability depends upon a minimum input capacitance, so the circuit may oscillate with the input unplugged.

- Following similar reasoning, it is possible to raise the gain–bandwidth product inside the feedback loop by cascading two op-amp stages, properly configured. The stability of this arrangement depends on careful placement of the unity-gain crossing of the loop gain within this transresistance configuration – don't try this trick with a conventional *voltage* amplifier!
- We have only briefly discussed here the important issue of *noise* in transresistance amplifiers (which are often called upon to amplify very small signals). That is treated in Chapter 8 of AoE (devoted to low-noise design, including both discrete and op-amp voltage amplifiers), where there's a discussion of the unfortunate property of transresistance amplifiers of converting internal op-amp voltage noise into an effective input current noise, which rises proportional to frequency and to total C_{in}.
- As in Figure 4x.25, it's good hygiene to put low-capacitance protective clamps at the input of TIAs in which there's risk of high-voltage transients (from a biased detector, etc.). A nice (but unrelated) trick we've seen[23] is the deliberate use of the CMOS op-amp's input protection diodes to reset the integrator capacitor – by simply pulsing the supply rails with a momentary (and current-limited) polarity reversal.
- To trim the compensation it's a good idea to use a test fixture that can provide a clean nanoamp-scale square wave. This is discussed in §8.11.13 in AoE3, with a suggested circuit (Fig. 8.91).

4x.3.7 Designs by the masters: A wide-range linear transimpedance amplifier

The dynamic range (i.e., ratio of maximum to minimum input current) of a resistance-feedback transimpedance amplifier like that in Figure 4x.16A is limited by several factors. First, the op-amp's input bias current sets an approximate lower bound on measurable currents, typically somewhere around a picoamp for op-amps of reasonable precision (but as low as 10 fA for less accurate CMOS parts[24]).

Second, for a given feedback resistance R_f, the current range is bounded at the high end by the op-amp's supply voltage, i.e., $I_{max} \leq V_S/R_f$; and at the low end it becomes inaccurate when the output approaches the op-amp's offset voltage, i.e., $I_{min} \geq V_{os}/R_f$. These constraints limit the dynamic range to $I_{max}/I_{min} \lesssim V_S/V_{os}$. In practical terms, that's roughly a dynamic range of 10^5 ($\sim$10V/100μV) for low-offset op-amps.

One way to get a larger dynamic range is to use nonlinear diode-like feedback to create a logarithmic response (see §4x.20). For some applications this is just what you want. But this method suffers from several drawbacks: (a) you can't average or lowpass-filter the output voltage to get the average input current (because the average of the log is not the log of the average); (b) it's difficult to get significant precision, say at the part-per-thousand level, owing to drift and calibration uncertainties; and (c) you often want good linearity with signals of both polarities (and which cross through zero).

What you want, then, is a linear precision TIA that somehow spans multiple sensitivity ranges simultaneously. Figure 4x.30 shows an elegant implementation, devised by Stephen Eckel and his team at Yale University.[25] The basic topology is a standard resistive-feedback TIA, here implemented with op-amp A_1 and a series string of resistors (R_1–R_3, with successive ratios of 100:1) that individually would span four decades of full-scale sensitivity. To this basic circuit JFETs Q_1–Q_4 have been added, which go into conduction progressively as each range reaches full-scale output; this prevents op-amp A_1 from saturating, as explained below.

Here's how it works: for the lowest input currents ($I_0 < 100\,\text{nA}$) the voltage developed at A_1's output is just $I_0(R_1+R_2+R_3)$, and output amplifier A_2's gain (approximately $\times 2$) is chosen to produce 10 V output (called V_1) for 100 nA input. That input current is full-scale for the most sensitive range, and at that current the op-amp's output is approximately 5 V. The other output amplifiers A_3

[23] Thanks to Bernie Gottschalk for this elegant suggestion.

[24] With the stunning exception of the ADA4530-1, with its 1 fA typ (20 fA max) bias current at 25°C, remarkably combined with a precise 9 μV typ (50 μV max) offset voltage. Its noise performance is, uh, underwhelming – some 80 nV/$\sqrt{\text{Hz}}$ at 10 Hz.

[25] S. Eckel, A.O. Sushkov, and S.K. Lamoreaux, "A high dynamic range, linear response transimpedance amplifier," *Rev. Sci. Instrum.*, **83**, 026106 (2012).

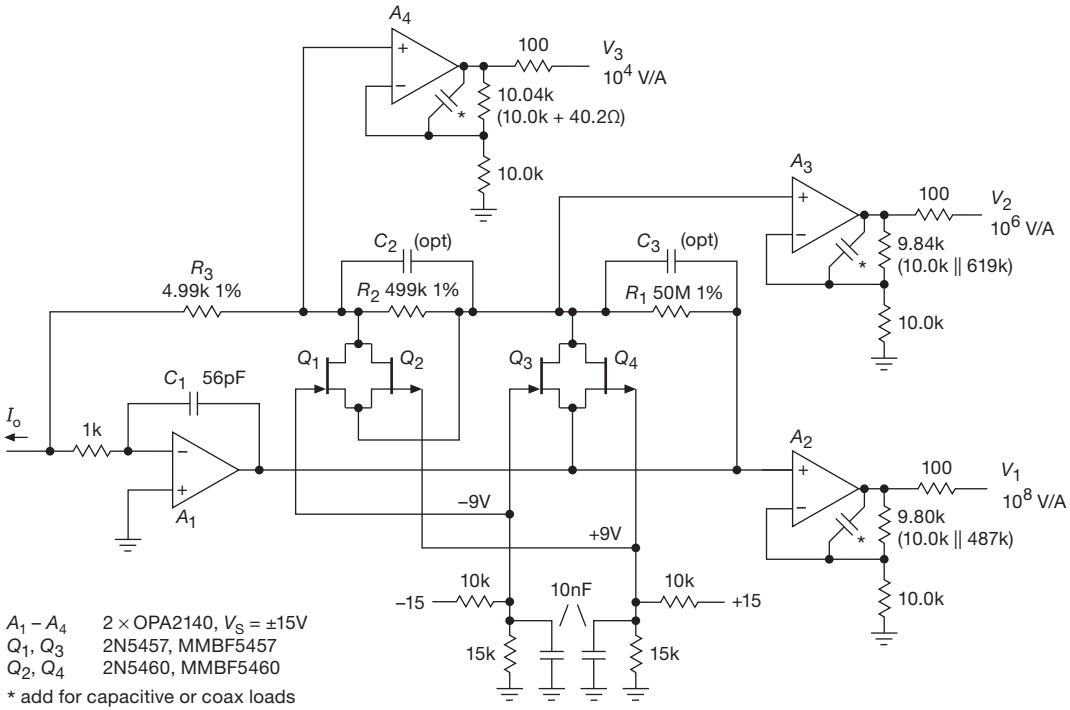


Figure 4x.30. Wide dynamic-range linear transimpedance amplifier, with three simultaneous outputs with sensitivities in ratios of 100:1. The JFETs Q_1–Q_4 shunt current around each gain-setting feedback resistor after the respective stage passes its full-scale output.

and A_4 generate the outputs for the higher-current ranges: A_3 picks off the voltage developed by I_0 flowing through R_2+R_3, and A_4 picks off the voltage developed by I_0 flowing through R_3 alone.

Now for the trick: for input currents significantly greater than 100 nA, A_1's output would saturate, but that is prevented by Q_3 or Q_4. For example, an input sinking current of 200 nA, which would bring A_1's output to +10 V, instead causes *p*-channel JFET Q_4 to conduct (its gate is biased at +9 V), effectively shunting R_1 and preventing saturation. So the TIA loop remains in the active region, and A_3's output (V_2, with its sensitivity of 1 V/μA) will be at the correct +0.1 V. Similarly, input currents great enough to bring V_2 beyond full-scale cause Q_2 to shunt current around R_2, again preventing A_1's saturation.

Figure 4x.31 shows measured performance, plotted on log–log axes, illustrating nicely the stacking of simultaneous linear outputs, each of which saturates just beyond full-scale. These data were taken for positive output polarity only (i.e., input sinking current, shown as I_0 in the circuit diagram), but the circuit as drawn works properly for both polarities, notionally illustrated (on linear axes) in Figure 4x.32 and seen accurately in the measured data of Figure 4x.33. If only one polarity is required, the complementary JFETs in Figure 4x.30 can be omitted.

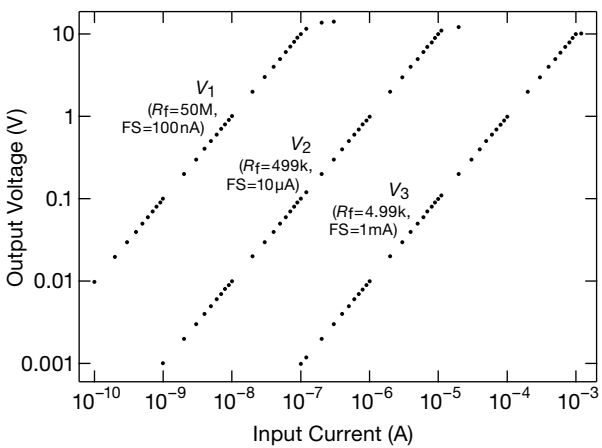


Figure 4x.31. Measured simultaneous outputs of the wide-range transimpedance amplifier of Figure 4x.30, demonstrating a dynamic range of 10^7:1. For V_2 and V_3, corrections (i.e., zero-current offsets) of 0.12 mV and 0.045 mV were applied; they barely nudged the lowest few points.

A few comments on the circuit: (a) C_1 provides fre-

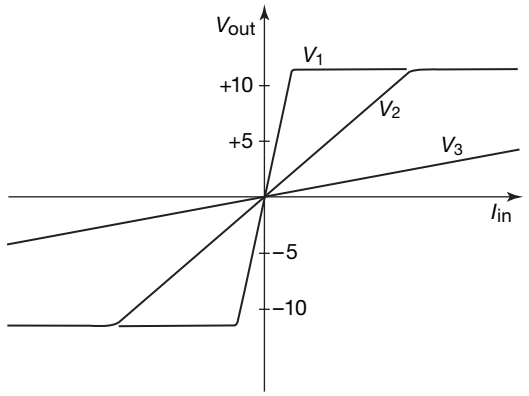


Figure 4x.32. The wide-range TIA, implemented with split supplies and with JFETs of both polarities (Fig. 4x.30), generates simultaneous linear outputs that transition smoothly through zero, as indicated in this sketch (with gain ratios of 5:1) and in the measured data in the next figure.

quency compensation; the 56 pF value we used would need to be increased for a capacitive input source.

(b) Additional compensation capacitors C_2 and C_3 can be used to tailor frequency response of the individual ranges; we omitted them for our measurements.

(c) The series 1k input resistor protects A_1 if the input is overdriven; it has no effect on performance.

(d) We chose OPA2140 op-amps for their low V_{os}, low I_B, and good value (see the mini-table below); the low-current performance could be improved somewhat with OPA627B's (expensive), or considerably more with the ADA4530-1 (but with poorer noise performance).

(e) To obtain the full dynamic range, it's necessary that the leakage currents of JFETs Q_1–Q_4 be no more than a few picoamps. The guidance provided by the datasheets will leave you sleepless: worst-case gate reverse currents of 1000 pA and 5000 pA (for *n*- and *p*-channel, respectively, at room temperature and 15 V–20 V reverse bias). And, if you worry about *channel* leakage when cutoff, the datasheet is particularly unhelpful, specifying only a range of gate voltages to produce "cutoff" drain currents of 10,000 pA and 1,000,000 pA (for *n* and *p* types, respectively). Happily, the manufacturers are highly conservative, and the actual situation is far better: we measured total leakage currents (at room temperature, and at gate-to-drain voltages to 15 V) ranging from 0.1 pA to 3 pA for 17 JFET samples; see the discussion in §2x.1.

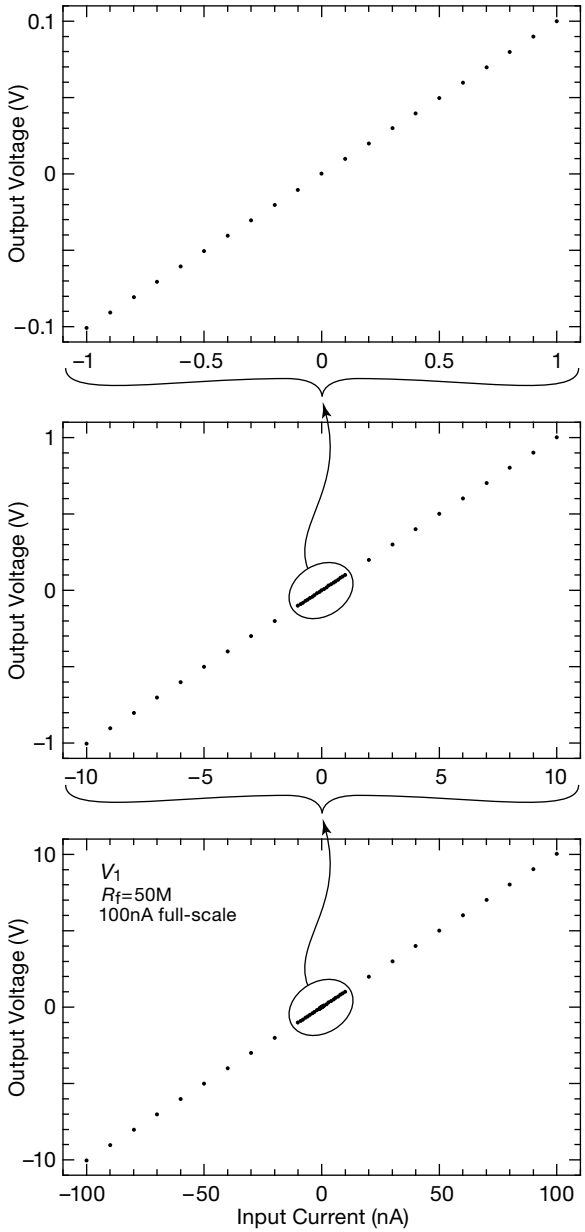


Figure 4x.33. These linear plots of output voltage versus input current for the most sensitive scale (i.e., V_1: 0.1V/nA) show the TIA's linearity straight through zero input current. No corrections have been applied to these measured data.

4x.3.8 A "starlight-to-sunlight" linear photometer

Here's a nice application for a wide-range linear transimpedance amplifier of the kind described in §4x.3.7 (which you should read first): a photometer that measures

Type[a]	V_{os} typ (μV)	V_{os} max (μV)	I_b typ (pA)	I_b max (pA)	e_n 10Hz (nV/◊)	e_n 1kHz (nV/◊)	i_n typ (fA/◊)	Price qty 10 (US$)
OPA627B	40	100	1	5	15	5.2	1.6	30.81
OPA2140[b]	30	120	0.5	10	8	5.1	0.8	5.38
ADA4530-1[c]	9	50	0.001	0.02	80	16	0.07	21.72

Notes: ◊ = nV/√Hz. (a) except as noted, V_S=36V max total supply. (b) dual. (c) V_S=16V max total.

Figure 4x.34. Op-amp choices for wide-range linear transimpedance amplifier.

a wide range of illumination,[26] going from sunlight to starlight. This really pushes the limits of dynamic range, ranging over some 8 orders of magnitude: bright sunlight is approximately 110,000 lux, and dark-sky starlight is about 0.002 lux (100 times darker than the full moon's 0.25 lux). And we'd really like 9 orders of magnitude, to give us 10% accuracy at the lowest light levels.

Because the photocurrent is unipolarity, we can run the circuit from a single supply polarity (almost – see discussion below). We also need only p-channel JFETs for the successive resistor clamping circuits. We chose the transimpedance gains of the taps in the ratio 300:1 (R_1, R_2, R_3), with full-scale output of +5 V; the output voltages are digitized by a 3-channel, 12-bit ADC running from +5 V and ground. The TIA stage is powered from +12 V, to accommodate the over-range behavior of the wide-range TIA scheme, while the unity-gain buffers and the ADC run from +5 V; the 10k resistors R_4–R_6 limit current into the input clamp diodes to less than 1 mA. Figures 4x.36 and 4x.37 show SPICE simulations of the input-current to output-voltage transfer characteristics: the log–log plot is helpful for seeing the stacked linear outputs, and the log–linear plot illustrates nicely the successive clamping as each stage saturates.

A significant challenge in this design was the choice of op-amps. The input (TIA) stage A_1 must run at 10–12 V to preserve a 5 V full-scale output on each tap (illustrated graphically in the plots of Fig. 4x.37), but we need more: its input current must be down in the 0.5LSB range (i.e., <6 pA), and its offset voltage should be less than the voltage step corresponding to 0.5LSB of the ADC (i.e., <0.6 mV). It also must operate with the inputs at ground, and its output voltage range must extend to ground (RRO). For the buffer op-amps A_3 and A_4 we can use a low-voltage part (i.e., +5 V single supply), but with rail-to-rail input and output.

With these constraints we found two good candidates for A_1 – TI's LMP7701 and LTC's LTC6240HV – and two candidate dual op-amps for A_3A_4 – ADI's AD8616 and LTC's LTC6078. The table lists their relevant specifications. For the input stage A_1 we're down around 0.2 LSB for V_{os} and 0.1 LSB for I_B, conservatively taking the worst-case (max) values. But these are FET inputs, so we should expect significantly higher bias currents at elevated temperatures; even so, we're OK up to 60°C or so. For the followers A_3A_4 the dual op-amps AD8616 and LTC6078 meet our requirements.

The photodiode was chosen to match the amplifier's gain and dynamic range. The S1133-14 is an inexpensive silicon photodiode in a ceramic package, producing 3 mA in full sunlight; it's being operated here in photovoltaic mode (zero bias), but it does see the op-amp's offset voltage across its terminals. No worry, though – the S1133-14 photodiode spec shows dark current (with an extravagant 10 mV bias) as 0.2 pA (typ), and sloping down to an extrapolated current less than 0.1 pA at 1 mV bias. The S2387-33R photodiode does even better, in fact specifying a maximum leakage of 5 pA at 10 mV bias (and a typical value of 0.1 pA).

"Getting to ground"

And now for the troublesome business of RRO op-amps not delivering on their promise: the cruel fact is that most RRO op-amps operating with a single positive supply cannot bring their output fully to ground, even when unloaded. The V_{OL} specs in the table (taken from the datasheets) show this problem, which we discuss in further detail in §§4x.11.3 and 4x.11.4; but, put simply, the quiescent current through the op-amp's push–pull output stage produces a drop across the pulldown transistor's R_{ON}. In §4x.11.4 we show two ways of dealing with this (sinking current from the op-amp's output, or bringing the op-amp's negative supply terminal a hundred millivolts or so below ground). We prefer the latter, and we've indicated such a connection on the schematic.

Some additional circuit details: (a) Because full-scale current for the least-sensitive range is 5 mA (compared with 1 mA for the circuit of Fig. 4x.30), we chose a larger JFET (type J175), which specifies I_{DSS}=7 mA (min). You may worry about JFET leakage current compromising the

[26] Officially, *illuminance*, which is the flux of light per unit area (lumens/meter) upon a surface, weighted to take account of the eye's spectral sensitivity. Photometric units can drive you nuts, with candela, lumen, lux, and a host of confusing names like radiant flux, radiant intensity, radiance, irradiance, radiosity, radiant exitance, radiant exposure, luminous flux, luminous intensity, luminance, illuminance; and most of these can host the modifier "spectral," meaning the same photometric quantity per unit frequency (or per unit wavelength). See also §9x.22.

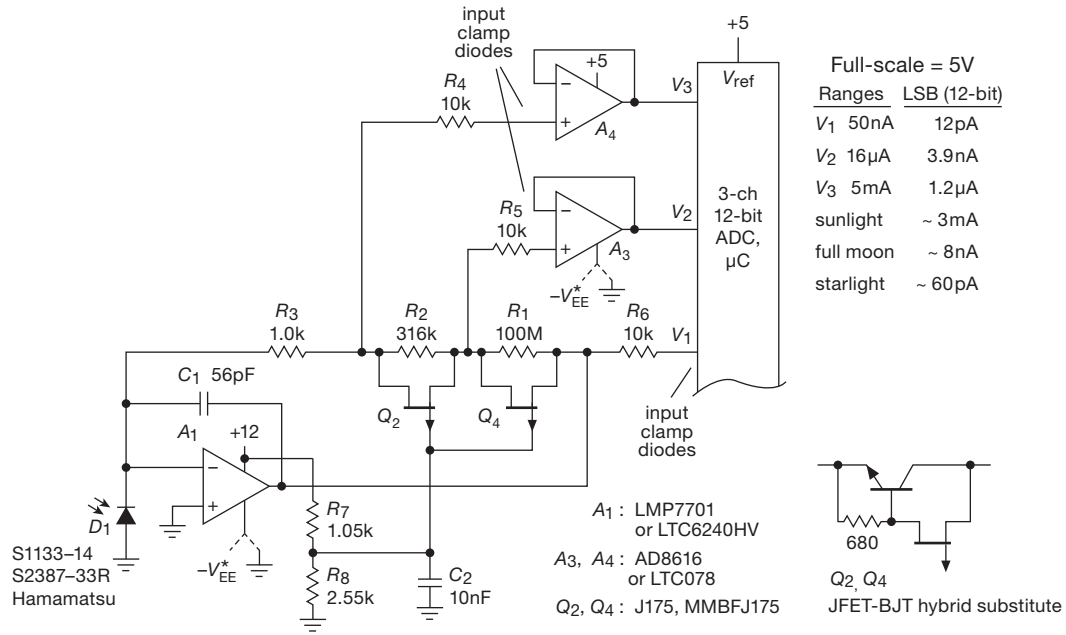


Figure 4x.35. Starlight-to-sunlight linear photometer, based on the method of §4x.3.7. The V_{SS} terminal of the "single-supply" op-amps should be powered from −100 mV or so, to ensure operation all the way to ground; see §4x.11.3.

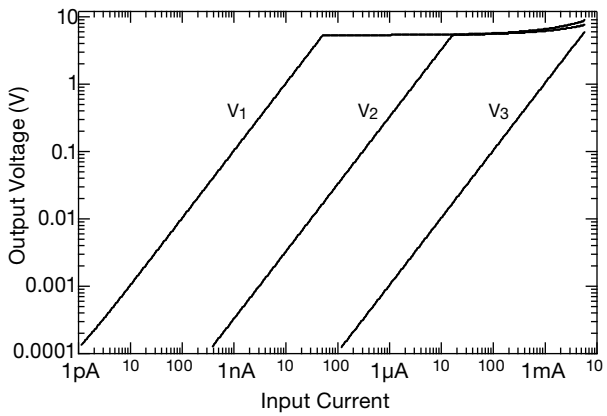


Figure 4x.36. SPICE simulation of the three output voltages versus (sinking) input current, for the circuit of Fig. 4x.35.

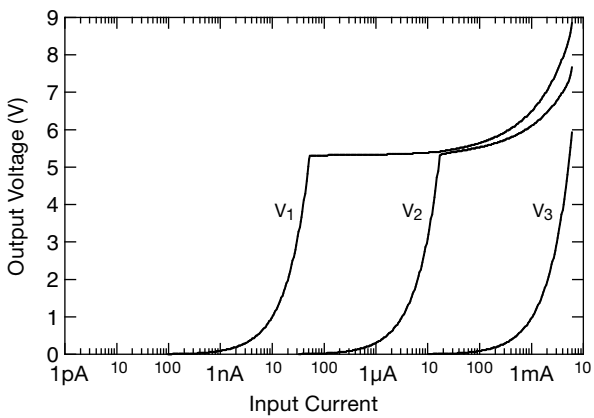


Figure 4x.37. Same data as Fig. 4x.36, plotted on log-linear scales.

dynamic range at the low-current end; but, in spite of its larger die geometry, the several samples we measured[27] exhibited leakage currents of only 1 pA at room temperature (with as much as 15 V gate-to-channel bias).

(b) Another way to extend the operating current is to add a small *npn* BJT to Q_2 and Q_4 as shown in the inset in Figure 4x.35. If you go this route, be warned that BJT leakage is highly unpredictable, as we found by actual measurement, see §2x.1.

(c) The loose V_P specification makes it difficult to set Q_2's and Q_4's gate bias: 3 V (min), 6 V (max). We've complained about this JFET ugliness before, you know the drill. It's probably best to trim the bias manually (and while you're at it, measure the output with zero input current, to ensure that leakage effects do not prevent proper operation down to ∼10 pA or so).

[27] See the discussion of transistor leakage in §2x.1.

Type	V_{supply} (V)	I_b[a] typ (pA)	I_b[a] max (pA)	V_{os} typ (μV)	V_{os} max (μV)	V_{OL} typ (mV)	V_{OL} max (mV)	I_s typ (mA)	GBW typ (MHz)
LMP7701	2.7-12	0.2[b]	1[b]	37	200	40[c]	50[c]	0.8	2.5
LTC6240HV	2.8-11	0.5[b]	1[b]	60	250	15	30	2.7	18
AD8616[d]	2.7-5.5	0.2	1	80	500	7.5[e]	15[e]	1.7[f]	24
LTC6078[d]	2.7-5.5	0.2	1	25	100	1	–	0.06[f]	0.75

Notes: (a) at T=25°C. (b) at V_S=+10V. (c) when sinking 0.5mA. (d) dual. (e) when sinking 1mA. (f) per amplifier.

Figure 4x.38. Op-amp choices for Fig. 4x.35.

4x.3.9 Autoranging wideband transimpedance amplifier

In §4x.3.7 we presented a linear TIA with a seven-decade dynamic range. The trick was to generate three simultaneous linear outputs, each with its own gain factor (going by factors of 100); so the output with the highest gain pins at full scale, while the others continue working. The input current is then read from the most sensitive non-saturated range. We used this same trick in §4x.3.8 to create a "starlight-to-sunlight photometer" with linear outputs and with sensitivity to photocurrents from 1 pA to 5 mA (a factor of 5×10^9).

As nice as those circuits are, they do have the drawback of rather limited bandwidth. For example, in Figure 4x.30 the "bypass" JFETs Q_3 and Q_4 add bandwidth-robbing capacitance to ground at the downstream side of the highest-value (50MΩ) feedback resistor R_1. Ordinary (single-gain) transimpedance amplifiers, lacking bypass JFETs, do not suffer from this problem.

But there's another way to achieve wide dynamic range in a linear transimpedance amplifier, based on a suggestion by the ever-creative John Larkin. Look at Figure 4x.39, which illustrates this novel technique in the context of a wideband photodiode amplifier (where we've chosen OSI's PIN-13D silicon photodiode: 13 mm^2 area in a TO-5 hermetic package).

In this unusual circuit the lower-sensitivity ranges start operating after each more-sensitive range saturates, and (unlike the earlier schemes) the input current is derived as a weighted sum of the outputs of all the individual gain stages, as we'll see presently.

In this single-polarity circuit, TIA amplifier A_1 (a wideband RRIO with 3 pA bias current) operates normally until enough input current causes its output to saturate at the positive supply rail. Further input current causes A_1 to lose control of its summing-junction node, whereupon the voltage at its inverting input drops below ground enough to

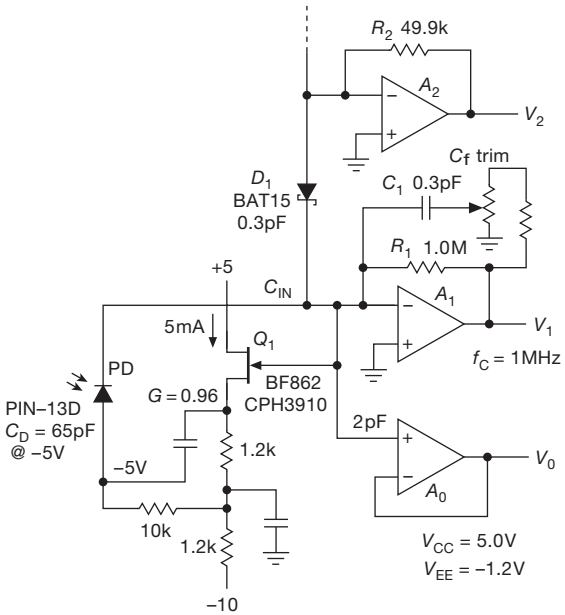


Figure 4x.39. Linear autoranging TIA. When high-gain TIA A_1 saturates, lower-gain A_2 absorbs the additional input current, while A_0 corrects for the offset at A_1's summing junction.

forward bias Schottky diode D_1, allowing amplifier A_2 to take over.[28] The use of rail-to-rail op-amps allows us to know the saturation voltage, thus the current through the feedback resistor when stage A_1 (and subsequent stages, if used) is in saturation.

Once A_2 takes over, A_1's summing junction (buffered by A_0) will be below ground by a Schottky diode drop, which means the current through R_1 is now $(V_1-V_0)/R_1$, so the correct input current (sinking) is just

$$I_{in} = \frac{V_1 - V_0}{R_1} + \frac{V_2}{R_2} \tag{4x.3}$$

Bandwidth

It's a struggle to get bandwidth in a high-gain TIA. To achieve 1 MHz in a TIA with 1MΩ feedback resistance we needed a feedback capacitance C_f of 0.16 pF, implemented here with a 0.3 pF capacitor "tuned" with a trimmer.

The total capacitance at the summing-junction node C_{in} is the sum of Q_1's feedback capacitance C_{rss}, plus the common-mode and differential capacitances of A_0 and A_1, plus D_1's capacitance at zero bias, plus the (bootstrapped) capacitance of the photodiode.[29] The latter is a bit less than 5% of the photodiode's 65 pF capacitance at −5 V, thanks

[28] The photodiode's bias will drop slightly, but this is of no consequence.
[29] See §8.11.9.

to the bootstrap from JFET follower Q_1 (whose voltage gain is >0.95). These terms add up to about 11.2 pF, for an f_{RC} of 14.2 kHz – the penalty over a conventional single-gain TIA is only 2.3 pF, great!. With the 100 MHz rail-to-rail OPA357 for A_1 and a CPH3910[30] for Q_1, we get an f_{GM} of 1.2 MHz, and the damping factor for $f_c = 1.0$ MHz is about 0.8 (see §4x.3.2). Overall we're getting a bandwidth improvement (for equivalent transimpedance gain) of some 10×–20×, as compared with the JFET-bypass scheme of §4x.3.8.

Some details.

(1) For D_1 we chose a small-die Schottky diode, BAT15-03W, for its low 0.3 pF capacitance. At 100 μA (where A_2 goes into saturation) the diode's drop is about 180 mV, which adds about 4% current through R_1; that is why follower A_0 is needed to get 1% precision in this circuit.

(2) Because the summing junction is pulled a diode drop below ground when A_1 saturates, it's necessary[31] to power its negative rail a volt or so below ground; here we chose −1.2 V (two diode drops, easily generated).

(3) We're powering our op-amps with a precision +5.0 V supply. The OPA357 has a 7.5 V absolute maximum rating, enough for us to use more than a −1.2 V negative rail. If you wanted a higher saturated output voltage (say +10.0 V), this would be a good place to use a composite amplifier configuration (see Figure 8.78 for inspiration).

(4) This scheme can be extended to additional stages, by adding another Schottky diode and (lower gain) TIA stages at the top. Each stage (except the topmost) needs a follower to track its summing-junction offset at saturation; and each stage increases the negative offset of lower stages by a diode drop. So it may be better to use the "JFET-bypass" method (Figure 4x.35) for the lower-gain stages, where higher capacitances wouldn't matter. But in the example here, A_1 is the special high-gain stage where it's hard to achieve a 1 MHz bandwidth in a TIA stage with 1MΩ feedback resistance.

4x.3.10 Multiple-range cascode-bootstrap wideband TIA

Continuing the theme of wideband transimpedance amplifiers, the critical bandwidth-robbing (and e_nC noise-degrading) issue of summing-junction capacitance in photodiode amplifiers can be nicely addressed by a combination of an isolating cascode transistor and a bootstrap of the low side of the photodiode. We've seen these before (JFET bootstrap: Figure 4x.39 and §8.11.9; and cascode with bootstrap: §8.11.10), but not in the context of gain-switching.

Here we combine these bandwidth-enhancing techniques with the ability to switch the transimpedance gain. Figure 4x.29 showed the best way to connect an SPDT switch to change the gain of a wideband TIA, but it did not include circuitry to reduce summing-junction capacitance, which is almost always needed in a wideband TIA.

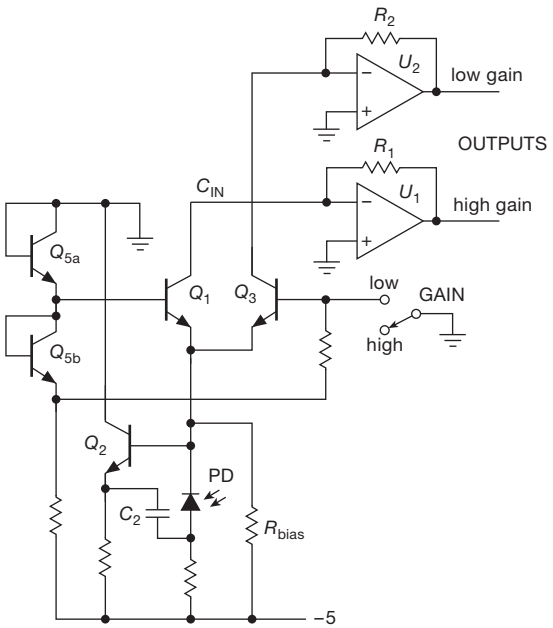


Figure 4x.40. Cascode-bootstrap wideband transimpedance amplifier with multiple switch-selected gain outputs.

Figure 4x.40, based on suggestions by Phil Hobbs,[32] fills this gap. In this circuit Q_2 is the bootstrap follower that dramatically lowers the effective photodiode capacitance, which is then isolated from the summing junction by cascode transistor Q_1. This enables both greater bandwidth and lower e_nC noise.

Before explaining the gain-switching, some important comments on the circuit so far:

(1) Q_2's operating current must be somewhat higher than the maximum photodiode current, making its base current

[30] To replace the popular BF862, inexplicably discontinued by NXP.

[31] But see §4x.11.3.

[32] For a good first reading assignment, try his "Photodiode Front Ends – The REAL Story," *Optics and Photonics News*, April 2001, pp 42–45. And follow that with his book *Building Electro-Optical Systems, Making It All Work*, 2nd ed., Wiley (2009), a fine collection of tricks for designing cascode photodiode amplifiers, including series peaking inductors and *T*-coils to extend the bandwidth, noise cancellers, and more.

a possible issue at low photodiode currents. Hobbs suggests using a high-beta MPSA18 (similar to 2N5089); the MMBT6429 and MMBT5962 are candidate surface-mount alternatives.

(2) The photodiode capacitance C_{PD} is in parallel with Q_1's base-emitter capacitance C_π (see §2x.11). This lowers Q_1's effective f_T, which we want to keep well above f_c. For example, a 2N5089 has an f_T of about 2 MHz at 10 μA (see Figure 2x.80 and note how f_T increases roughly proportional to I_C at low currents, due to fixed $C_\pi = C_{je}$ values below 30 μA). To make the cascode work at low photodiode currents we exploit Q_2's bootstrapping to reduce C_{PD} to values well below C_π of Q_1. We may also need to add R_{bias} to maintain a minimum current through Q_1 (Hobbs added 8 μA).[33]

Now for the gain-switching: We start by adding dual transistor[34] Q_5 to generate two stacked voltages just below ground, and we use the first voltage to bias our primary cascode transistor Q_1. Generally you'd dedicate Q_1 to the highest-gain stage. The second lower voltage is used to back-bias the unused secondary cascode-transistor candidates Q_3, Q_4, etc. These transistors can be turned on individually to take over the photodiode current, by switching their base to ground.[35] This scheme can be extended to additional range stages, each with its separate output. Unlike the two autoranging approaches discussed earlier, in this scheme you must select the single active range and output. However, you could use one of the cascode transistors to feed a JFET-bypass or diode-stacked autoranging circuit, as described in §§4x.3.7, 4x.3.8, and 4x.3.9.

[33] You can cancel most of this extra current with resistors from the summing junction to the positive supply, for example as shown in Fig. 8.87. But if you do that in the gain-switched circuit here (Fig. 4x.40), the "off" op-amp will saturate at the negative rail). These considerations reduce the attractiveness of this circuit for photocurrents below 100 nA.

[34] Some dual *npn* transistor choices are the DMMT3904W or MMDT3904. We like Diodes Inc.'s selection of dual transistors in SOT-23-6 (SOT-26) or SC-70-6 (SOT-363) and smaller(!) packages.

[35] Increasing the photodiode's back-bias by half a volt, of no consequence.