Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
- Computational Fluid Dynamics

cadence®

PCB Design and Analysis Learning Map

Beginner

Advanced

Logic Design

- Allegro® Design Entry HDL Front-to-Back Flow (3)
- Allegro Design Entry HDL Basics (1)
- Allegro System Capture (2.5)
- Allegro System Architect (2)
- Allegro Design Reuse (1)
- Allegro AMS Simulator (3)
  - Allegro AMS Simulator Advanced Analysis (1)
- Allegro Design Entry Using OrCAD® Capture (2)
- OrCAD CIS (1)
- OrCAD Capture Constraint Manager PCB Flow (1)
- Allegro EDM Design Entry HDL Front-to-Back Flow (3)
- Allegro Team Design Authoring (1)
- Analog Simulation with PSpice® (3)
  - Analog Simulation with PSpice® using System Capture (3)
  - Analog Simulation with PSpice Advanced Analysis (1)

PCB Design

- Allegro PCB Editor Basic Techniques (3.5)
  - Allegro PCB Editor Intermediate Techniques (2.5)
  - Allegro PCB Router Basics (2)
  - Allegro PCB Editor Advanced Methodologies (1)
- Allegro High-Speed Constraint Management (2)
- Allegro DesignTrue DFM NEW (2)
- Allegro Update Training (2)
- Advanced Design Verification with the RAVEL Programming Language (2)

SI/PI Analysis

- Essential High-Speed PCB Design for Signal Integrity (3)
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials (2)
- Allegro Sigrity™ SI Foundations (2)
- Allegro Sigrity PI (1)
- Sigrity PowerDC™ and OptimizePI™ (1)
- Sigrity Aurora (2)
- SystemSI for Parallel Bus and Serial Link Analysis NEW (2)
- Model Generation and Analysis using PowerSI and Broadband SPICE (3)
- Clarity 3D Solver (2)
- Celsius Thermal Solver (1)

Library Development

- Allegro PCB Librarian (2)
- Allegro EDM PCB Librarian NEW (2)
- Allegro Design Entry HDL SKILL® Programming Language (3)
- Allegro PCB Editor SKILL Programming Language (3)

NEW New Course

Number of days for instructor-led course

Online Course Available

Digital Badge Available

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IC Package Design and Analysis Learning Map

Beginner

Advanced

IC Package Design

- SiP Layout — 4
- Allegro® Package Designer — 4
- Allegro FPGA System Planner — 2
- Allegro Sigrity Package Assessment and Model Extraction — 1
- OrbitIO™ System Planner — 1
- Advanced Design Verification with the RAVEL Programming Language NEW — 2
- Allegro Package Designer Plus — 3

SI/PI Analysis

- Allegro Sigrity™ SI Foundations — 2
- Allegro Sigrity PI — 1
- Sigrity PowerDC™ and OptimizePI™ — 1
- SystemSI for Parallel Bus and Serial Link Analysis NEW — 2
- Model Generation and Analysis using PowerSI and Broadband SPICE — 3
- Clarity 3D Solver — 2
- Celsius Thermal Solver — 1

NEW New Course | # Number of days for instructor-led course | Online Course Available | Digital Badge Available

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Custom IC, Analog, Microwave and RF Design Learning Map

1 of 2 – see next page

Beginner

Advanced

Circuit Modeling, Analog/Mixed-Signal/RF Circuit Design and Simulation

Mixed-Signal Simulation

- Mixed-Signal Simulations using Spectre AMS Designer
- Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model NEW
- SimVision for Debugging Mixed-Signal Simulations

AMS/Real Number Modeling

- Analog Modeling with Verilog-A
- Behavioral Modeling with Verilog AMS
- Real Modeling with Verilog-AMS
- Real Modeling with SystemVerilog
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification NEW

- Virtuoso Schematic Editor
- Virtuoso Visualization and Analysis

Virtuoso® ADE Explorer & Assembler Series

- **S1** ADE Explorer & Single Test Corner Analysis
- **S2** ADE Assembler & Multi Test Corner Analysis
- **S3** Sweeping Variables and Simulating Corners
- **S4** Monte Carlo, Real-Time Tuning & Run Plans

Virtuoso® ADE Verifier Series

- **S1** Setup, Run, & View Verifier Results
- **S2** Reference Flow and Analog Coverage Using the Setup Library Assistant

Microwave & RF Design (AWR®)

- Microwave Office for RF Designers
- 5G mmWave Handset System Design – **S1** Simulation and Verification of the RFIC (Transceiver)

Spectre® Simulator Fundamentals Series

- **S1** Spectre Basics
- **S2** Large-Signal Analyses
- **S3** Small-Signal Analyses
- **S4** Spectre MDL

- Design Checks and Asserts
- High-Performance Spectre Simulation (APS, Spectre X)
- Spectre FX Simulator NEW

Virtuoso® Spectre® Pro Series

- **S1** DC Algorithm
- **S2** Transient Algorithm

Spectre® RF Series

- RF Analysis Using Shooting Newton NEW
- RF Analysis Using Harmonic Balance NEW

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Custom IC, Analog and RF Design Learning Map

2 of 2 – see prior page

Beginner

Advanced

IC CAD

- SKILL® Language Programming Introduction — 2
- SKILL Language Programming — 5
- SKILL Development of Parameterized Cells — NEW — 2
- Advanced SKILL Language Programming — NEW — 3

Physical Design and Advanced Nodes

- Virtuoso® Layout Design Basics — L — 1
- Virtuoso Connectivity-Driven Layout Transition — L, XL, GXL, EXL — 2
- Virtuoso Abstract Generator — GXL — 1
- Virtuoso Floorplanner — GXL — 1

Virtuoso® Advanced-Node – ICADVM

- Virtuoso Layout for Advanced Nodes — 2
  - T1: Place and Route — 1 — NEW
  - T2: Electromigration — 0.5
  - Virtuoso Layout for Advanced Nodes and Methodology Platform — EXL — 0.5

Virtuoso® Layout Pro Series

- T1: Env. and Basic Commands — L — 1
- T2: Create and Edit Commands — L — 1
- T3: Basic Commands — XL — 1
- T4: Advanced Commands — XL — 1
- T5: Interactive Routing — XL — 1
- T6: Constraint-Driven Flow and Power Routing — XL, GXL — 1
- T7: Module Generator and Floorplanner — XL, GXL — 1
- T8: Concurrent Layout Editing — EXL — 1 — NEW
- T9: Virtuoso Design Planner — EXL — 2 — NEW

Physical Verification

- Pegasus Verification System — NEW — 2
  - Physical Verification System — 2
    - Physical Verification Language Rules-Writer — 2

Quantus™ Extraction Solution Transistor-Level Series

- T1: Overview and Technology Setup — NEW — 0.5
- T2: Parasitic Extraction — NEW — 1
- T3: Extracted View Flows and Advanced Features — NEW — 0.5

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

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Digital Design and Signoff Learning Map

Beginner

Advanced

Synthesis and Test

- Fundamentals of IEEE 1801 Low-Power Specification Format
- Genus™ Synthesis Solution with Stylus Common UI
- Genus Low-Power Synthesis Flow with IEEE 1801
- Low-Power Synthesis Flow with Genus Stylus Common UI
- Test Synthesis with Genus Stylus Common UI
- Advanced Synthesis with Genus Stylus Common UI
- Modus DFT Software Solution
- Joules™ Power Calculator NEW

Implementation

- Design For Test Fundamentals
- Innovus Block Implementation with Stylus Common UI
- Innovus Hierarchical Implementation with Stylus Common UI
- Innovus Low-Power Flow with Stylus Common UI
- Innovus Clock Concurrent Optimization Technology with Stylus Common UI

Silicon Signoff

- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure with Stylus Common UI
- Voltus™ Power Grid Analysis and Signoff with Stylus Common UI

Equivalence Checking

- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal Low-Power Verification Using IEEE1801
- Conformal ECO

Digital IC Design Fundamentals NEW

Cadence® RTL-to-GDSII Flow

Virtuoso® Digital Implementation

Artificial Intelligence and Machine Learning Fundamentals NEW

Cadence® Cerebrus™ Intelligent Chip Explorer NEW

NEW New Course | # Number of days for instructor-led course | Online Course Available | Digital Badge Available

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System Design and Verification Learning Map

Beginner

Advanced

Simulation, Coverage and Debug

- Digital IC Design Fundamentals — NEW — 2.25
- Xcelium™ Simulator — NEW — 2
- Cadence® RTL-To-GDSII Flow — 2
- VIP Basic Building Blocks and Usage — NEW — 2
- Low-Power Simulation with CPF — 2
- Low-Power Simulation with IEEE1801 UPF — 2
- Foundations of Metric-Driven Verification — 1
- Xcelium Integrated Coverage — 2
- Metric-Driven Verification Using vManager™ — 3
- vManager Tool Usage in Batch Mode — 0.5
- Protium™ Introduction — NEW — 1
- Verisium™ Debug — NEW — 1
- Perspec™ System Verifier - Basic — NEW — 3
- Xcelium Fault Simulator — NEW — 1.5
- Specman® Fundamentals for Block-Level Environment Developers — 5
- Specman Advanced Verification — 4

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

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System Design and Verification Learning Map

Beginner

Advanced

Design and Verification Languages

- Verilog Language and Application — 4
- VHDL Language and Application — 5
- C++ Language Fundamentals for Design and Verification — 3
- Real Modeling with Verilog AMS — 2
- SystemVerilog for Design and Verification — 5
- SystemC® Language Fundamentals — 3
- Real Modeling with SystemVerilog — 3
- SystemC Synthesis with Stratus HLS — 3
- SystemVerilog Real Number Modeling (SV-RNM) Based Advanced Verification — NEW — 5
- UVM
  - Essential SystemVerilog for UVM (optional) — 1
  - SystemVerilog Accelerated Verification Using UVM — 4
- SystemVerilog Assertions — 2
- SystemC Transaction-Level Modeling TLM2.0 — 2
- Perl for EDA Engineering — 3
- Jasper® Formal Fundamentals — 2
- Tcl Scripting for EDA — 3
- SystemVerilog Advanced Register Verification Using UVM — NEW — 2
- Jasper® Formal Expert — NEW — 2

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

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Safety and Reliability Platform Learning Map

Beginner

Advanced

MIDAS Safety Platform

MIDAS™ Safety Platform Introduction NEW

0.5

Midas™ Safety Analysis Authoring NEW

0.5

Xcelium Fault Simulator NEW

1.5

Functional Safety Implementation with Midas™ NEW

0.5

Beginner

Advanced

NEW New Course

Number of days for instructor-led course

L XL GXL Tiers of Cadence products used in course

Online Course Available

Digital Badge Available

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Tensilica Processor IP Learning Map

1 of 2 – see next page

Tensilica Xtensa LX

- Tensilica® Xtensa® LX Processor Fundamentals (2)
- Tensilica Xtensa LX Processor Interfaces (0.5)
- Tensilica Xtensa LX Hardware Verification and EDA (0.5)
- Tensilica Instruction Extension Language and Design (1)
- Tensilica System Modeling using XTSC (1)

ConnX DSP

- Tensilica ConnX BBE16EP Baseband Engine (2)
- Tensilica ConnX BBE32EP Baseband Engine (2)
- Tensilica ConnX BBE64EP Baseband Engine (2)
- Tensilica ConnX 110 and 120 DSP Family (2)

Fusion & FloatingPoint DSP

- Tensilica Fusion F1 DSP (1)
- Tensilica Fusion G3 DSP (2)
- Tensilica Fusion G6 DSP (2)
- Tensilica FloatingPoint DSP Family (2)

HiFi Audio DSP

- Tensilica Audio Codec API (0.5)
- Tensilica HiFi 2/EP/Mini Audio Engine ISA (0.75)
- Tensilica HiFi 3 Audio Engine ISA (0.75)
- Tensilica HiFi 4 DSP (1)
- Tensilica HiFi 5 DSP (1)
- Tensilica Xtensa Audio Framework (0.5)

Vision DSP

- Tensilica Vision DSP Family (2)
- Tensilica Xtensa Neural Network Compiler v2 (0.5)
- Tensilica DNA 100 Architecture and Programming (1)

NEW New Course | # Number of days for instructor-led course | Online Course Available

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Tensilica Processor IP Learning Map

Tensilica Xtensa NX

- Tensilica® Xtensa® NX Processor Fundamentals (2)
- Tensilica Xtensa NX Processor Interfaces (1)
- Tensilica Xtensa NX Hardware Verification and EDA (1)
- Tensilica Instruction Extension Language and Design (1)
- Tensilica System Modeling using XTSC (1)

ConnX DSP

- Tensilica ConnX B10 DSP (2)
- Tensilica ConnX B20 DSP (2)

Vision DSP

- Tensilica Vision DSP Family (2)
- Tensilica Xtensa Neural Network Compiler v2 (0.5)

NEW New Course | # Number of days for instructor-led course | Online Course Available

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Computational Fluid Dynamics

Beginner

Advanced

Fidelity

Turbomachinery

Fidelity Turbo: Introduction

3

Meshing

Fidelity Automesh for Unstructured Meshing

1.5

Auto Aero

Fidelity Flow

2.25

Fine

Marine

Fine Marine for Beginners

2.5

Fine Marine for Advanced Users

1.75

Beginner

Advanced

NEW New Course

Number of days for instructor-led course

Online Course Available

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