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Vivado v2018.3 (64-bit)

SW Build 2405991 on Thu Dec 6 23:38:27 MST 2018

IP Build 2404404 on Fri Dec 7 01:43:56 MST 2018

Start of session at: Thu Oct 17 09:47:31 2024

Process ID: 2488

Current directory: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/impl_1

Command line: vivado.exe -log hello_world_arty_a7.vdi -applog -product Vivado -messageDb vivado.pb -mode batch -source hello_world_arty_a7.tcl -notrace

Log file: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/impl_1/hello_world_arty_a7.vdi

Journal file: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/impl_1\vivado.jou

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source hello_world_arty_a7.tcl -notrace

Command: link_design -top hello_world_arty_a7 -part xc7a100ticsg324-1L

Design is defaulting to srcset: sources_1

Design is defaulting to constrset: constrs_1

INFO: [Netlist 29-17] Analyzing 499 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100ticsg324-1L

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

Finished Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 662.672 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

link_design completed successfully

link_design: Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 . Memory (MB): peak = 666.695 ; gain = 342.516

Command: opt_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100ti'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100ti'

Running DRC as a precondition to command opt_design

Starting DRC Task

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more information.

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.396 . Memory (MB): peak = 673.355 ; gain = 6.660

Starting Cache Timing Information Task

INFO: [Timing 38-35] Done setting XDC timing constraints.

Ending Cache Timing Information Task | Checksum: d2908b99

Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 1226.879 ; gain = 553.523

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 1ae07186e

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.159 . Memory (MB): peak = 1321.395 ; gain = 0.000

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 2 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 1ce9b1b07

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.193 . Memory (MB): peak = 1321.395 ; gain = 0.000

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 25333abda

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.234 . Memory (MB): peak = 1321.395 ; gain = 0.000

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 25333abda

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.272 . Memory (MB): peak = 1321.395 ; gain = 0.000

INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 13bfedcda

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.428 . Memory (MB): peak = 1321.395 ; gain = 0.000

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Phase 6 Post Processing Netlist

Phase 6 Post Processing Netlist | Checksum: 13bfedcda

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.442 . Memory (MB): peak = 1321.395 ; gain = 0.000

INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed 0 cells

Opt_design Change Summary

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Phase	#Cells created	#Cells Removed	#Constrained objects preventing optimizations
Retarget	0	2	0
Constant propagation	0	0	0
Sweep	0	0	0
BUFG optimization	0	0	0
Shift Register Optimization	0	0	0
Post Processing Netlist	0	0	0

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.005 . Memory (MB): peak = 1321.395 ; gain = 0.000

Ending Logic Optimization Task | Checksum: 13bfedcda

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.453 . Memory (MB): peak = 1321.395 ; gain = 0.000

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Physopt 32-619] Estimated Timing Summary | WNS=2.584 | TNS=0.000 |

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

INFO: [Pwropt 34-9] Applying IDT optimizations ...

INFO: [Pwropt 34-10] Applying ODC optimizations ...

Starting PowerOpt Patch Enables Task

INFO: [Pwropt 34-162] WRITE_MODE attribute of 0 BRAM(s) out of a total of 2 has been updated to save power. Run report_power_opt to get a complete listing of the BRAMs updated.

INFO: [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports

Number of BRAM Ports augmented: 0 newly gated: 0 Total Ports: 4

Ending PowerOpt Patch Enables Task | Checksum: 13bfedcda

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.015 . Memory (MB): peak = 1493.020 ; gain = 0.000

Ending Power Optimization Task | Checksum: 13bfedcda

Time (s): cpu = 00:00:03 ; elapsed = 00:00:07 . Memory (MB): peak = 1493.020 ; gain = 171.625

Starting Final Cleanup Task

Ending Final Cleanup Task | Checksum: 13bfedcda

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1493.020 ; gain = 0.000

Starting Netlist Obfuscation Task

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1493.020 ; gain = 0.000

Ending Netlist Obfuscation Task | Checksum: 13bfedcda

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1493.020 ; gain = 0.000

INFO: [Common 17-83] Releasing license: Implementation

29 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt_design completed successfully

opt_design: Time (s): cpu = 00:00:08 ; elapsed = 00:00:15 . Memory (MB): peak = 1493.020 ; gain = 826.324

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1493.020 ; gain = 0.000

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.019 . Memory (MB): peak = 1493.020 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1493.020 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/impl_1/hello_world_arty_a7_opt.dcp' has been generated.

INFO: [runtcl-4] Executing : report_drc -file hello_world_arty_a7_drc_opted.rpt -pb hello_world_arty_a7_drc_opted.pb -rpx hello_world_arty_a7_drc_opted.rpx

Command: report_drc -file hello_world_arty_a7_drc_opted.rpt -pb hello_world_arty_a7_drc_opted.pb -rpx hello_world_arty_a7_drc_opted.rpx

INFO: [IP_Flow 19-234] Refreshing IP repositories

INFO: [IP_Flow 19-1704] No user IP repositories specified

INFO: [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.3/data/ip'.

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Coretcl 2-168] The results of DRC are in file C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/impl_1/hello_world_arty_a7_drc_opted.rpt.

report_drc completed successfully

Command: place_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100ti'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100ti'

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Running DRC as a precondition to command place_design

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: c5cb6cfe

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.012 . Memory (MB): peak = 1493.020 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 75699d37

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.637 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 12cca6339

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 12cca6339

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 1 Placer Initialization | Checksum: 12cca6339

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 2 Global Placement

Phase 2.1 Floorplanning

Phase 2.1 Floorplanning | Checksum: b5c48163

Time (s): cpu = 00:00:01 ; elapsed = 00:00:01 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 2.2 Physical Synthesis In Placer

INFO: [Physopt 32-65] No nets found for high-fanout optimization.

INFO: [Physopt 32-232] Optimized 0 net. Created 0 new instance.

INFO: [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell

INFO: [Physopt 32-456] No candidate cells for DSP register optimization found in the design.

INFO: [Physopt 32-775] End 2 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell

INFO: [Physopt 32-677] No candidate cells for Shift Register optimization found in the design

INFO: [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell

INFO: [Physopt 32-526] No candidate cells for BRAM register optimization found in the design

INFO: [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell

INFO: [Physopt 32-949] No candidate nets found for HD net replication

INFO: [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1493.020 ; gain = 0.000

Summary of Physical Synthesis Optimizations

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| Optimization | Added Cells | Removed Cells | Optimized Cells/Nets | Dont Touch | Iterations | Elapsed |

| Very High Fanout | 0 | 0 | 0 | 0 | 1 | 00:00:00 |

| DSP Register | 0 | 0 | 0 | 0 | 1 | 00:00:00 |

| Shift Register | 0 | 0 | 0 | 0 | 1 | 00:00:00 |

| BRAM Register | 0 | 0 | 0 | 0 | 1 | 00:00:00 |

| HD Interface Net Replication | 0 | 0 | 0 | 0 | 1 | 00:00:00 |

| Total | 0 | 0 | 0 | 0 | 5 | 00:00:00 |

Phase 2.2 Physical Synthesis In Placer | Checksum: dbc75597

Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 2 Global Placement | Checksum: cf3d6c6e

Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: cf3d6c6e

Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 186b2c8cf

Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: f8c2e1e2

Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 114314dd0

Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 3.5 Fast Optimization

Phase 3.5 Fast Optimization | Checksum: 15a2038d2

Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 3.6 Small Shape Detail Placement

Phase 3.6 Small Shape Detail Placement | Checksum: c605d06d

Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 3.7 Re-assign LUT pins

Phase 3.7 Re-assign LUT pins | Checksum: 18f3dca42

Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 3.8 Pipeline Register Optimization

Phase 3.8 Pipeline Register Optimization | Checksum: 1919d32eb

Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 3 Detail Placement | Checksum: 1919d32eb

Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 4.1.1 Post Placement Optimization

Post Placement Optimization Initialization | Checksum: 11f098c89

Phase 4.1.1.1 BUFG Insertion

INFO: [Place 46-33] Processed net rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1, BUFG insertion was skipped due to placement/routing conflicts.

INFO: [Place 46-46] BUFG insertion identified 1 candidate nets, 0 success, 0 bufg driver replicated, 1 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason

Phase 4.1.1.1 BUFG Insertion | Checksum: 11f098c89

Time (s): cpu = 00:00:04 ; elapsed = 00:00:08 . Memory (MB): peak = 1493.020 ; gain = 0.000

INFO: [Place 30-746] Post Placement Timing Summary WNS=0.652. For the most accurate timing information please run report_timing.

Phase 4.1.1 Post Placement Optimization | Checksum: 1dd605122

Time (s): cpu = 00:00:04 ; elapsed = 00:00:10 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 4.1 Post Commit Optimization | Checksum: 1dd605122

Time (s): cpu = 00:00:04 ; elapsed = 00:00:10 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 1dd605122

Time (s): cpu = 00:00:05 ; elapsed = 00:00:10 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 1dd605122

Time (s): cpu = 00:00:05 ; elapsed = 00:00:10 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 4.4 Final Placement Cleanup

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 4.4 Final Placement Cleanup | Checksum: 2667e634b

Time (s): cpu = 00:00:05 ; elapsed = 00:00:10 . Memory (MB): peak = 1493.020 ; gain = 0.000

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 2667e634b

Time (s): cpu = 00:00:05 ; elapsed = 00:00:10 . Memory (MB): peak = 1493.020 ; gain = 0.000

Ending Placer Task | Checksum: 18a1bf855

Time (s): cpu = 00:00:05 ; elapsed = 00:00:10 . Memory (MB): peak = 1493.020 ; gain = 0.000

INFO: [Common 17-83] Releasing license: Implementation

62 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

place_design completed successfully

place_design: Time (s): cpu = 00:00:05 ; elapsed = 00:00:11 . Memory (MB): peak = 1493.020 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1493.020 ; gain = 0.000

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1493.020 ; gain = 0.000

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.192 . Memory (MB): peak = 1493.020 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/impl_1/hello_world_arty_a7_placed.dcp' has been generated.

INFO: [runtcl-4] Executing : report_io -file hello_world_arty_a7_io_placed.rpt

report_io: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.038 . Memory (MB): peak = 1493.020 ; gain = 0.000

INFO: [runtcl-4] Executing : report_utilization -file hello_world_arty_a7_utilization_placed.rpt -pb hello_world_arty_a7_utilization_placed.pb

INFO: [runtcl-4] Executing : report_control_sets -verbose -file hello_world_arty_a7_control_sets_placed.rpt

report_control_sets: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.010 . Memory (MB): peak = 1493.020 ; gain = 0.000

Command: route_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100ti'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100ti'

Running DRC as a precondition to command route_design

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs

Checksum: PlaceDB: e3800a5a ConstDB: 0 ShapeSum: a69bedfb RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: 139447039

Time (s): cpu = 00:00:09 ; elapsed = 00:00:19 . Memory (MB): peak = 1527.500 ; gain = 34.480

Post Restoration Checksum: NetGraph: 5f9c486b NumContArr: d9a827ce Constraints: 0 Timing: 0

Phase 2 Router Initialization

Phase 2.1 Create Timer

Phase 2.1 Create Timer | Checksum: 139447039

Time (s): cpu = 00:00:09 ; elapsed = 00:00:19 . Memory (MB): peak = 1559.676 ; gain = 66.656

Phase 2.2 Fix Topology Constraints

Phase 2.2 Fix Topology Constraints | Checksum: 139447039

Time (s): cpu = 00:00:09 ; elapsed = 00:00:19 . Memory (MB): peak = 1565.852 ; gain = 72.832

Phase 2.3 Pre Route Cleanup

Phase 2.3 Pre Route Cleanup | Checksum: 139447039

Time (s): cpu = 00:00:09 ; elapsed = 00:00:19 . Memory (MB): peak = 1565.852 ; gain = 72.832

Number of Nodes with overlaps = 0

Phase 2.4 Update Timing

Phase 2.4 Update Timing | Checksum: 1ad362af0

Time (s): cpu = 00:00:10 ; elapsed = 00:00:20 . Memory (MB): peak = 1576.809 ; gain = 83.789

INFO: [Route 35-416] Intermediate Timing Summary | WNS=0.976 | TNS=0.000 | WHS=-0.090 | THS=-4.424 |

Phase 2 Router Initialization | Checksum: 19dbc5d9b

Time (s): cpu = 00:00:10 ; elapsed = 00:00:20 . Memory (MB): peak = 1582.121 ; gain = 89.102

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: 134ecab43

Time (s): cpu = 00:00:10 ; elapsed = 00:00:21 . Memory (MB): peak = 1589.543 ; gain = 96.523

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 2219

Number of Nodes with overlaps = 844

Number of Nodes with overlaps = 575

Number of Nodes with overlaps = 330

Number of Nodes with overlaps = 202

Number of Nodes with overlaps = 156

Number of Nodes with overlaps = 101

Number of Nodes with overlaps = 38

Number of Nodes with overlaps = 24

Number of Nodes with overlaps = 11

Number of Nodes with overlaps = 3

Number of Nodes with overlaps = 1

Number of Nodes with overlaps = 0

INFO: [Route 35-416] Intermediate Timing Summary | WNS=-0.224 | TNS=-0.729 | WHS=N/A | THS=N/A |

Phase 4.1 Global Iteration 0 | Checksum: 1b8544cd8

Time (s): cpu = 00:00:13 ; elapsed = 00:00:34 . Memory (MB): peak = 1592.492 ; gain = 99.473

Phase 4.2 Global Iteration 1

Number of Nodes with overlaps = 421

Number of Nodes with overlaps = 381

Number of Nodes with overlaps = 245

Number of Nodes with overlaps = 143

Number of Nodes with overlaps = 71

Number of Nodes with overlaps = 52

Number of Nodes with overlaps = 54

Number of Nodes with overlaps = 57

Number of Nodes with overlaps = 38

Number of Nodes with overlaps = 18

Number of Nodes with overlaps = 16

Number of Nodes with overlaps = 10

Number of Nodes with overlaps = 9

Number of Nodes with overlaps = 0

INFO: [Route 35-416] Intermediate Timing Summary | WNS=0.416 | TNS=0.000 | WHS=N/A | THS=N/A |

Phase 4.2 Global Iteration 1 | Checksum: 18de6dfbf

Time (s): cpu = 00:00:14 ; elapsed = 00:00:42 . Memory (MB): peak = 1592.492 ; gain = 99.473

Phase 4 Rip-up And Reroute | Checksum: 18de6dfbf

Time (s): cpu = 00:00:14 ; elapsed = 00:00:42 . Memory (MB): peak = 1592.492 ; gain = 99.473

Phase 5 Delay and Skew Optimization

Phase 5.1 Delay CleanUp

Phase 5.1 Delay CleanUp | Checksum: 18de6dfbf

Time (s): cpu = 00:00:14 ; elapsed = 00:00:42 . Memory (MB): peak = 1592.492 ; gain = 99.473

Phase 5.2 Clock Skew Optimization

Phase 5.2 Clock Skew Optimization | Checksum: 18de6dfbf

Time (s): cpu = 00:00:14 ; elapsed = 00:00:42 . Memory (MB): peak = 1592.492 ; gain = 99.473

Phase 5 Delay and Skew Optimization | Checksum: 18de6dfbf

Time (s): cpu = 00:00:14 ; elapsed = 00:00:42 . Memory (MB): peak = 1592.492 ; gain = 99.473

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1.1 Update Timing

Phase 6.1.1 Update Timing | Checksum: 17e99958e

Time (s): cpu = 00:00:14 ; elapsed = 00:00:43 . Memory (MB): peak = 1592.492 ; gain = 99.473

INFO: [Route 35-416] Intermediate Timing Summary | WNS=0.512 | TNS=0.000 | WHS=0.187 | THS=0.000 |

Phase 6.1 Hold Fix Iter | Checksum: 17e99958e

Time (s): cpu = 00:00:14 ; elapsed = 00:00:43 . Memory (MB): peak = 1592.492 ; gain = 99.473

Phase 6 Post Hold Fix | Checksum: 17e99958e

Time (s): cpu = 00:00:14 ; elapsed = 00:00:43 . Memory (MB): peak = 1592.492 ; gain = 99.473

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 1.49885 %

Global Horizontal Routing Utilization = 1.82651 %

Routable Net Status*

*Does not include unroutable nets such as driverless and loadless.

Run report_route_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Phase 7 Route finalize | Checksum: 212a4d049

Time (s): cpu = 00:00:14 ; elapsed = 00:00:43 . Memory (MB): peak = 1592.492 ; gain = 99.473

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: 212a4d049

Time (s): cpu = 00:00:14 ; elapsed = 00:00:43 . Memory (MB): peak = 1592.492 ; gain = 99.473

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: 23e442237

Time (s): cpu = 00:00:14 ; elapsed = 00:00:43 . Memory (MB): peak = 1592.492 ; gain = 99.473

Phase 10 Post Router Timing

INFO: [Route 35-57] Estimated Timing Summary | WNS=0.512 | TNS=0.000 | WHS=0.187 | THS=0.000 |

INFO: [Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report_timing_summary.

Phase 10 Post Router Timing | Checksum: 23e442237

Time (s): cpu = 00:00:14 ; elapsed = 00:00:43 . Memory (MB): peak = 1592.492 ; gain = 99.473

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:14 ; elapsed = 00:00:43 . Memory (MB): peak = 1592.492 ; gain = 99.473

Routing Is Done.

INFO: [Common 17-83] Releasing license: Implementation

80 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

route_design completed successfully

route_design: Time (s): cpu = 00:00:14 ; elapsed = 00:00:44 . Memory (MB): peak = 1592.492 ; gain = 99.473

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1592.492 ; gain = 0.000

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1592.492 ; gain = 0.000

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.343 . Memory (MB): peak = 1592.492 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/impl_1/hello_world_arty_a7_routed.dcp' has been generated.

INFO: [runtcl-4] Executing : report_drc -file hello_world_arty_a7_drc_routed.rpt -pb hello_world_arty_a7_drc_routed.pb -rpx hello_world_arty_a7_drc_routed.rpx

Command: report_drc -file hello_world_arty_a7_drc_routed.rpt -pb hello_world_arty_a7_drc_routed.pb -rpx hello_world_arty_a7_drc_routed.rpx

INFO: [IP_Flow 19-1839] IP Catalog is up to date.

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Coretcl 2-168] The results of DRC are in file C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/impl_1/hello_world_arty_a7_drc_routed.rpt.

report_drc completed successfully

INFO: [runtcl-4] Executing : report_methodology -file hello_world_arty_a7_methodology_drc_routed.rpt -pb hello_world_arty_a7_methodology_drc_routed.pb -rpx hello_world_arty_a7_methodology_drc_routed.rpx

Command: report_methodology -file hello_world_arty_a7_methodology_drc_routed.rpt -pb hello_world_arty_a7_methodology_drc_routed.pb -rpx hello_world_arty_a7_methodology_drc_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 2 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/impl_1/hello_world_arty_a7_methodology_drc_routed.rpt.

report_methodology completed successfully

INFO: [runtcl-4] Executing : report_power -file hello_world_arty_a7_power_routed.rpt -pb hello_world_arty_a7_power_summary_routed.pb -rpx hello_world_arty_a7_power_routed.rpx

Command: report_power -file hello_world_arty_a7_power_routed.rpt -pb hello_world_arty_a7_power_summary_routed.pb -rpx hello_world_arty_a7_power_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

92 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

report_power completed successfully

INFO: [runtcl-4] Executing : report_route_status -file hello_world_arty_a7_route_status.rpt -pb hello_world_arty_a7_route_status.pb

INFO: [runtcl-4] Executing : report_timing_summary -max_paths 10 -file hello_world_arty_a7_timing_summary_routed.rpt -pb hello_world_arty_a7_timing_summary_routed.pb -rpx hello_world_arty_a7_timing_summary_routed.rpx -warn_on_violation

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

INFO: [runtcl-4] Executing : report_incremental_reuse -file hello_world_arty_a7_incremental_reuse_routed.rpt

INFO: [Vivado_Tcl 4-1062] Incremental flow is disabled. No incremental reuse Info to report.

INFO: [runtcl-4] Executing : report_clock_utilization -file hello_world_arty_a7_clock_utilization_routed.rpt

INFO: [runtcl-4] Executing : report_bus_skew -warn_on_violation -file hello_world_arty_a7_bus_skew_routed.rpt -pb hello_world_arty_a7_bus_skew_routed.pb -rpx hello_world_arty_a7_bus_skew_routed.rpx

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

INFO: [Common 17-206] Exiting Vivado at Thu Oct 17 09:48:56 2024...