
| Tool Version : Vivado v.2018.3 (win64) Build 2405991 Thu Dec 6 23:38:27 MST 2018

| Date   : Thu Oct 17 09:48:09 2024

| Host   : Samuel running 64-bit major release (build 9200)

| Command   : report_control_sets -verbose -file hello_world_arty_a7_control_sets_placed.rpt

| Design   : hello_world_arty_a7

| Device   : xc7a100ti

Control Set Information

Table of Contents

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1. Summary

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| Status | Count |

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| Number of unique control sets | 62 |

| Unused register locations in slices containing registers | 72 |

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2. Histogram

Fanout	Control Sets
1	1
4	3
5	2
6	1
8	3
9	2
13	1
14	1
16+	48

3. Flip-Flop Distribution

Clock Enable	Synchronous Set/Reset	Asynchronous Set/Reset	Total Registers	Total Slices
No	No	No	23	16
No	No	Yes	0	0
No	Yes	No	188	70
Yes	No	No	9	5
Yes	No	Yes	0	0
Yes	Yes	No	1548	565

4. Detailed Control Set Information

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| Clock Signal | Enable Signal | Set/Reset Signal | Slice Load Count | Bel Load Count |

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| clock_IBUF_BUFG | | | 1 | 1 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/current_state[3]_i_2_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 1 | 4 |

| clock_50mhz_BUFG | | rvsteel_mcu_instance/rvsteel_spi_instance/curr_state0 | 3 | 4 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_spi_instance/bit_count[3]_i_2_n_0 | rvsteel_mcu_instance/rvsteel_spi_instance/cycle_counter1 | 1 | 4 |

| clock_50mhz_BUFG | | rvsteel_mcu_instance/rvsteel_core_instance/prev_write_request_reg_1[0] | 5 | 5 |

| clock_50mhz_BUFG | | rvsteel_mcu_instance/rvsteel_uart_instance/reset_internal | 3 | 5 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/csr_mcause[31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 6 | 6 |

| clock_50mhz_BUFG | | rvsteel_mcu_instance/rvsteel_spi_instance/cycle_counter[7]_i_1_n_0 | 2 | 8 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/mtimecmp[31]_i_2_0[0] | reset_debounced | 2 | 8 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/prev_rw_address_reg[3]_0[0] | reset_debounced | 3 | 8 |

| clock_50mhz_BUFG | | rvsteel_mcu_instance/rvsteel_core_instance/SR[0] | 3 | 9 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_uart_instance/tx_register | | 5 | 9 |

| clock_50mhz_BUFG | | rvsteel_mcu_instance/rvsteel_uart_instance/tx_register | 4 | 13 |

| clock_50mhz_BUFG | | reset_debounced
| 7 | 14 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/csr_mie_mfie0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 7 | 19 |

| clock_50mhz_BUFG | |
| 15 | 22 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/csr_mcause[31]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/csr_mcause[30]_i_1_n_0 | 18 | 26 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/csr_mepc[31]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 8 | 30 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_bus_instance/E[0] |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 15 | 31 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/csr_mtvec1 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 18 | 31 |

| clock_50mhz_BUFG | |
rvsteel_mcu_instance/rvsteel_uart_instance/rx_cycle_counter[0]_i_1_n_0 | 8 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[15][31]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 13 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/csr_minstret[31]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 8 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval[31]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 19 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[23][31]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 11 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/csr_minstret[63]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 8 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/csr_mscratch0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 19 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[3][31]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 9 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[21][31]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 14 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[11][31]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 12 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[17][31]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 12 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[10][31]_i_1_n_0 |
rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 9 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[12][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 8 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 10 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[14][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 12 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[16][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 12 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[1][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 8 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[22][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 11 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[27][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 13 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[28][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 12 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[13][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 11 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[25][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 9 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[29][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 10 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[2][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 11 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[26][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 12 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[18][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 14 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[30][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 13 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[24][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 8 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[9][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 10 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[6][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 10 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[5][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 14 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[7][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 9 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[4][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 12 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[8][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 10 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[20][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 10 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/mtimecmp[63]_i_2_0[1] | reset_debounced | 11 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/mtimecmp[63]_i_2_0[0] | reset_debounced | 7 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/prev_rw_address_reg[1]_0[0] | reset_debounced | 13 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/integer_file[19][31]_i_1_n_0 | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 11 | 32 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_core_instance/cr_en_reg[0] | reset_debounced | 20 | 64 |

| clock_50mhz_BUFG | | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 35 | 98 |

| clock_50mhz_BUFG | rvsteel_mcu_instance/rvsteel_bus_instance/prev_write_request_reg_0[0] | rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1 | 41 | 101 |

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