
| Tool Version : Vivado v.2018.3 (win64) Build 2405991 Thu Dec 6 23:38:27 MST 2018

| Date   : Thu Oct 17 09:48:55 2024

| Host   : Samuel running 64-bit major release (build 9200)

| Command   : report_methodology -file hello_world_arty_a7_methodology_drc_routed.rpt -pb hello_world_arty_a7_methodology_drc_routed.pb -rpx hello_world_arty_a7_methodology_drc_routed.rpx

| Design   : hello_world_arty_a7

| Device   : xc7a100ticsg324-1L

| Speed File   : -1L

| Design State : Fully Routed

Report Methodology

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1. REPORT SUMMARY

2. REPORT DETAILS

1. REPORT SUMMARY

Netlist: netlist

Floorplan: design_1

Design limits: <entire design considered>

Max violations: <unlimited>

Violations found: 2

| Rule | Severity | Description | Violations |

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| SYNTH-6 | Warning | Timing of a block RAM might be sub-optimal | 2 |

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2. REPORT DETAILS

SYNTH-6#1 Warning

Timing of a block RAM might be sub-optimal

The timing for the instance rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_0, implemented as a block RAM, might be sub-optimal as no output register was merged into the block

Related violations: <none>

SYNTH-6#2 Warning

Timing of a block RAM might be sub-optimal

The timing for the instance rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_1, implemented as a block RAM, might be sub-optimal as no output register was merged into the block

Related violations: <none>