Tool Version : Vivado v.2018.3 (win64) Build 2405991 Thu Dec 6 23:38:27 MST 2018		
Date : Thu Oct 17 09:48:08 2024		
Host : Samuel running 64-bit major release (build 9200)		
Command : report_utilization -file hello_world_arty_a7_utilization_placed.rpt -pb hello_world_arty_a7_utilization_placed.pb		
Design : hello_world_arty_a7		
Device : 7a100ticsg324-1L		
Design State : Fully Placed		
Utilization Design Information		
Table of Contents		
1. Slice Logic		
1.1 Summary of Registers by Type		
2. Slice Logic Distribution		
3. Memory		
4. DSP		
5. IO and GT Specific		
6. Clocking		
7. Specific Feature		
8. Primitives		
9. Black Boxes		
10. Instantiated Netlists		
1. Slice Logic		

1.1 Summary of Registers by Type

```
+----+
```

| Total | Clock Enable | Synchronous | Asynchronous |

+-----+

|0 | _| -| -|

| 0 | _ | - | Set |

| 0 | _ | - | Reset |

| 0 | _ | Set | - |

| 0 | _ | Reset | - |

| 0 | Yes | - | - |

| 0 | Yes | - | Set |

| 0 | Yes | - | Reset |

| 88 | Yes | Set | - |

| 1680 | Yes | Reset | - |

+-----+

2. Slice Logic Distribution

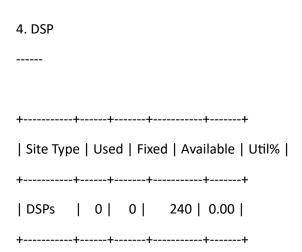
+	+
Site Type	Used Fixed Available Util%
+	+
Slice	843 0 15850 5.32
SLICEL	568 0
SLICEM	275 0
LUT as Logic	2394 0 63400 3.78
using O5 output only	1
using O6 output only	2151
using O5 and O6	242
LUT as Memory	0 0 19000 0.00
LUT as Distributed RAM	0 0
LUT as Shift Register	0 0
Slice Registers	1768 0 126800 1.39
Register driven from with	in the Slice 540
Register driven from outs	ide the Slice 1228
LUT in front of the regist	er is unused 609
LUT in front of the regist	er is used 619
Unique Control Sets	62 15850 0.39
+	+

^{*} Note: Available Control Sets calculated as Slice Registers / 8, Review the Control Sets Report for more information regarding control sets.

3. Memory

+-	+
	Site Type Used Fixed Available Util%
+-	+
	Block RAM Tile 2 0 135 1.48
	RAMB36/FIFO* 2 0 135 1.48
	RAMB36E1 only 2
	RAMB18 0 0 270 0.00
+-	+

^{*} Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1





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+-----+

| Site Type | Used | Fixed | Available | Util% |

+-----+

| Bonded IOB | 3 | 3 | 210 | 1.43 |

| IOB Master Pads | 1 | | |
```

```
| Bonded IPADs
       | 0 | 0 | 2 | 0.00 |
        | 0 | 0 | 6 | 0.00 |
| PHY_CONTROL
| PHASER_REF
        | 0 | 0 | 6 | 0.00 |
OUT_FIFO
        | 0 | 0 | 24 | 0.00 |
| IN_FIFO
       | 0 | 0 | 24 | 0.00 |
       | 0 | 0 | 6 | 0.00 |
| IDELAYCTRL
| IBUFDS
        | 0 | 0 | 202 | 0.00 |
| OLOGIC
       | 0 | 0 | 210 | 0.00 |
+-----+
```

6. Clocking

```
+----+
| Site Type | Used | Fixed | Available | Util% |
+-----+
| BUFGCTRL | 2 | 0 | 32 | 6.25 |
| BUFIO | 0 | 0 | 24 | 0.00 |
| MMCME2_ADV | 0 | 0 | 6 | 0.00 |
| PLLE2_ADV | 0 | 0 | 6 | 0.00 |
| BUFMRCE | 0 | 0 | 12 | 0.00 |
| BUFHCE | 0 | 0 | 96 | 0.00 |
| BUFR | 0 | 0 | 24 | 0.00 |
```

7. Specific Feature

8. Primitives

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| Ref Name | Used | Functional Category |

+----+

FDRE	1680	Flop & Latch
LUT6	1270	LUT
LUT5	584	LUT
LUT4	416	LUT
MUXF7	339	MuxFx
LUT3	263	LUT

```
| CARRY4 | 158 | CarryLogic |
| LUT2 | 94 | LUT |
| FDSE | 88 | Flop & Latch |
| LUT1 | 9 | LUT |
| RAMB36E1 | 2 | Block Memory |
| IBUF | 2 |
               10 |
| BUFG | 2 | Clock |
| OBUF | 1 |
               10 |
+----+
9. Black Boxes
+----+
| Ref Name | Used |
+----+
```

10. Instantiated Netlists

+----+

+----+

| Ref Name | Used |