	: 1986-2018 Xilinx, Inc. All Rights Reserved.
Tool Ver	rsion : Vivado v.2018.3 (win64) Build 2405991 Thu Dec 6 23:38:27 MST 2018
Date	: Thu Oct 17 09:47:57 2024
Host	: Samuel running 64-bit major release (build 9200)
Comma hello_wo	nd : report_drc -file hello_world_arty_a7_drc_opted.rpt -pb rld_arty_a7_drc_opted.pb -rpx hello_world_arty_a7_drc_opted.rpx
Design	: hello_world_arty_a7
Device	: xc7a100ticsg324-1L
Speed F	ile :-1L
Design S	State : Synthesized
Report Di	RC
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2. REPOR	T DETAILS
	T SUMMARY
Ne	tlist: netlist
Floc	orplan: design_1
	n limits: <entire considered="" design=""></entire>
Desigr	edeck: default
Desigr Rul	edeck: default ax violations: <unlimited></unlimited>

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2. REPORT DETAILS
