#-----------------------------------------------------------

# Vivado v2018.3 (64-bit)

# SW Build 2405991 on Thu Dec  6 23:38:27 MST 2018

# IP Build 2404404 on Fri Dec  7 01:43:56 MST 2018

# Start of session at: Wed Oct 16 15:22:56 2024

# Process ID: 28108

# Current directory: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/synth_1

# Command line: vivado.exe -log hello_world_arty_a7.vds -product Vivado -mode batch -messageDb vivado.pb -notrace -source hello_world_arty_a7.tcl

# Log file: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/synth_1/hello_world_arty_a7.vds

# Journal file: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/synth_1\vivado.jou

#-----------------------------------------------------------

source hello_world_arty_a7.tcl -notrace

Command: synth_design -top hello_world_arty_a7 -part xc7a100ticsg324-1L

Starting synth_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100ti'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100ti'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 37360

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Starting RTL Elaboration : Time (s): cpu = 00:00:00 ; elapsed = 00:00:01 . Memory (MB): peak = 431.664 ; gain = 99.523

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INFO: [Synth 8-6157] synthesizing module 'hello_world_arty_a7' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel_mcu' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mcu/rvsteel_mcu.v:8]

	Parameter CLOCK_FREQUENCY bound to: 50000000 - type: integer

Parameter UART_BAUD_RATE bound to: 9600 - type: integer

Parameter MEMORY_SIZE bound to: 8192 - type: integer

Parameter MEMORY_INIT_FILE bound to: hello_world.hex - type: string

Parameter BOOT_ADDRESS bound to: 0 - type: integer

Parameter GPIO_WIDTH bound to: 1 - type: integer

Parameter SPI_NUM_CHIP_SELECT bound to: 1 - type: integer

Parameter NUM_DEVICES bound to: 5 - type: integer

Parameter D0_RAM bound to: 0 - type: integer

Parameter D1_UART bound to: 1 - type: integer

Parameter D2_MTIMER bound to: 2 - type: integer

Parameter D3_GPIO bound to: 3 - type: integer

Parameter D4_SPI bound to: 4 - type: integer

INFO: [Synth 8-6157] synthesizing module 'rvsteel_core' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel_core.v:8]

Parameter BOOT_ADDRESS bound to: 0 - type: integer

Parameter MARCHID bound to: 12'b111100010010

Parameter MIMPID bound to: 12'b111100010011

Parameter CYCLE bound to: 12'b110000000000

Parameter TIME bound to: 12'b110000000001

Parameter INSTRET bound to: 12'b110000000010

Parameter CYCLEH bound to: 12'b110010000000

Parameter TIMEH bound to: 12'b110010000001

Parameter INSTRETH bound to: 12'b110010000010

Parameter MSTATUS bound to: 12'b001100000000

Parameter MSTATUSH bound to: 12'b001100010000

Parameter MISA bound to: 12'b001100000001

Parameter MIE bound to: 12'b001100000100

Parameter MTVEC bound to: 12'b001100000101

Parameter MSCRATCH bound to: 12'b001101000000

Parameter MEPC bound to: 12'b001101000001

Parameter MCAUSE bound to: 12'b001101000010

Parameter MTVAL bound to: 12'b001101000011

Parameter MIP bound to: 12'b001101000100

Parameter MCYCLE bound to: 12'b101100000000

Parameter MINSTRET bound to: 12'b101100000010

Parameter MCYCLEH bound to: 12'b101110000000

Parameter MINSTRETH bound to: 12'b101110000010

Parameter WB_ALU bound to: 3'b000

Parameter WB_LOAD_UNIT bound to: 3'b001

Parameter WB_UPPER_IMM bound to: 3'b010

Parameter WB_TARGET_ADDER bound to: 3'b011

Parameter WB_CSR bound to: 3'b100

Parameter WB_PC_PLUS_4 bound to: 3'b101

Parameter I_TYPE_IMMEDIATE bound to: 3'b001

Parameter S_TYPE_IMMEDIATE bound to: 3'b010

Parameter B_TYPE_IMMEDIATE bound to: 3'b011

Parameter U_TYPE_IMMEDIATE bound to: 3'b100

Parameter J_TYPE_IMMEDIATE bound to: 3'b101

Parameter CSR_TYPE_IMMEDIATE bound to: 3'b110

Parameter PC_BOOT bound to: 2'b00

Parameter PC_EPC bound to: 2'b01

Parameter PC_TRAP bound to: 2'b10

Parameter PC_NEXT bound to: 2'b11

Parameter LOAD_SIZE_BYTE bound to: 2'b00

Parameter LOAD_SIZE_HALF bound to: 2'b01

Parameter LOAD_SIZE_WORD bound to: 2'b10

Parameter CSR_RWX bound to: 2'b01

Parameter CSR_RSX bound to: 2'b10

Parameter CSR_RCX bound to: 2'b11

Parameter STATE_RESET bound to: 4'b0001

Parameter STATE_OPERATING bound to: 4'b0010

Parameter STATE_TRAP_TAKEN bound to: 4'b0100

Parameter STATE_TRAP_RETURN bound to: 4'b1000

Parameter NOP_INSTRUCTION bound to: 19 - type: integer

Parameter OPCODE_OP bound to: 7'b0110011

Parameter OPCODE_OP_IMM bound to: 7'b0010011

Parameter OPCODE_LOAD bound to: 7'b0000011

Parameter OPCODE_STORE bound to: 7'b0100011

Parameter OPCODE_BRANCH bound to: 7'b1100011

Parameter OPCODE_JAL bound to: 7'b1101111

Parameter OPCODE_JALR bound to: 7'b1100111

Parameter OPCODE_LUI bound to: 7'b0110111

Parameter OPCODE_AUIPC bound to: 7'b0010111

Parameter OPCODE_MISC_MEM bound to: 7'b0001111

Parameter OPCODE_SYSTEM bound to: 7'b1110011

Parameter FUNCT3_ADD bound to: 3'b000

Parameter FUNCT3_SUB bound to: 3'b000

Parameter FUNCT3_SLT bound to: 3'b010

Parameter FUNCT3_SLTU bound to: 3'b011

Parameter FUNCT3_AND bound to: 3'b111

Parameter FUNCT3_OR bound to: 3'b110

Parameter FUNCT3_XOR bound to: 3'b100

Parameter FUNCT3_SLL bound to: 3'b001

Parameter FUNCT3_SRL bound to: 3'b101

Parameter FUNCT3_SRA bound to: 3'b101

Parameter FUNCT3_ADDI bound to: 3'b000

Parameter FUNCT3_SLTI bound to: 3'b010

Parameter FUNCT3_SLTIU bound to: 3'b011

Parameter FUNCT3_ANDI bound to: 3'b111

Parameter FUNCT3_ORI bound to: 3'b110

Parameter FUNCT3_XORI bound to: 3'b100

Parameter FUNCT3_SLLI bound to: 3'b001

Parameter FUNCT3_SRLI bound to: 3'b101

Parameter FUNCT3_SRAI bound to: 3'b101

Parameter FUNCT3_BEQ bound to: 3'b000

Parameter FUNCT3_BNE bound to: 3'b001

Parameter FUNCT3_BLT bound to: 3'b100

Parameter FUNCT3_BGE bound to: 3'b101

Parameter FUNCT3_BLTU bound to: 3'b110

Parameter FUNCT3_BGEU bound to: 3'b111

Parameter FUNCT3_SB bound to: 3'b000

Parameter FUNCT3_SH bound to: 3'b001

Parameter FUNCT3_SW bound to: 3'b010

Parameter FUNCT3_ECALL bound to: 3'b000

Parameter FUNCT3_EBREAK bound to: 3'b000

Parameter FUNCT3_MRET bound to: 3'b000

Parameter FUNCT7_SUB bound to: 7'b0100000

Parameter FUNCT7_SRA bound to: 7'b0100000

Parameter FUNCT7_ADD bound to: 7'b0000000

Parameter FUNCT7_SLT bound to: 7'b0000000

Parameter FUNCT7_SLTU bound to: 7'b0000000

Parameter FUNCT7_AND bound to: 7'b0000000

Parameter FUNCT7_OR bound to: 7'b0000000

Parameter FUNCT7_XOR bound to: 7'b0000000

Parameter FUNCT7_SLL bound to: 7'b0000000

Parameter FUNCT7_SRL bound to: 7'b0000000

Parameter FUNCT7_SRAI bound to: 7'b0100000

Parameter FUNCT7_SLLI bound to: 7'b0000000

Parameter FUNCT7_SRLI bound to: 7'b0000000

Parameter FUNCT7_ECALL bound to: 7'b0000000

Parameter FUNCT7_EBREAK bound to: 7'b0000000

Parameter FUNCT7_MRET bound to: 7'b0011000

Parameter RS1_ECALL bound to: 5'b00000

Parameter RS1_EBREAK bound to: 5'b00000

Parameter RS1_MRET bound to: 5'b00000

Parameter RS2_ECALL bound to: 5'b00000

Parameter RS2_EBREAK bound to: 5'b00001

Parameter RS2_MRET bound to: 5'b00010

Parameter RD_ECALL bound to: 5'b00000

Parameter RD_EBREAK bound to: 5'b00000

Parameter RD_MRET bound to: 5'b00000

INFO: [Synth 8-6155] done synthesizing module 'rvsteel_core' (1#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel_core.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel_bus' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/bus/rvsteel_bus.v:8]

Parameter NUM_DEVICES bound to: 5 - type: integer

INFO: [Synth 8-6155] done synthesizing module 'rvsteel_bus' (2#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/bus/rvsteel_bus.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel_ram' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/ram/rvsteel_ram.v:8]

Parameter MEMORY_SIZE bound to: 8192 - type: integer

Parameter MEMORY_INIT_FILE bound to: hello_world.hex - type: string

INFO: [Synth 8-3876] $readmem data file 'hello_world.hex' is read successfully [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/ram/rvsteel_ram.v:53]

INFO: [Synth 8-6155] done synthesizing module 'rvsteel_ram' (3#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/ram/rvsteel_ram.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel_uart' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/uart/rvsteel_uart.v:8]

Parameter CLOCK_FREQUENCY bound to: 50000000 - type: integer

Parameter UART_BAUD_RATE bound to: 9600 - type: integer

Parameter CYCLES_PER_BAUD bound to: 5208 - type: integer

Parameter REG_WDATA bound to: 5'b00000

Parameter REG_RDATA bound to: 5'b00100

Parameter REG_READY bound to: 5'b01000

INFO: [Synth 8-6155] done synthesizing module 'rvsteel_uart' (4#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/uart/rvsteel_uart.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel_mtimer' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mtimer/rvsteel_mtimer.v:8]

Parameter REG_ADDR_WIDTH bound to: 2'b11

Parameter REG_CR bound to: 3'b000

Parameter REG_MTIMEL bound to: 3'b001

Parameter REG_MTIMEH bound to: 3'b010

Parameter REG_MTIMECMPL bound to: 3'b011

Parameter REG_MTIMECMPH bound to: 3'b100

Parameter BIT_CR_EN bound to: 5'b00000

Parameter BIT_CR_WIDTH bound to: 5'b00001

Parameter CR_PADDING bound to: 31'b0000000000000000000000000000000

INFO: [Synth 8-6155] done synthesizing module 'rvsteel_mtimer' (5#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mtimer/rvsteel_mtimer.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel_gpio' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/gpio/rvsteel_gpio.v:8]

Parameter GPIO_WIDTH bound to: 1 - type: integer

Parameter REG_ADDR_WIDTH bound to: 2'b11

Parameter REG_IN bound to: 3'b000

Parameter REG_OE bound to: 3'b001

Parameter REG_OUT bound to: 3'b010

Parameter REG_CLR bound to: 3'b011

Parameter REG_SET bound to: 3'b100

INFO: [Synth 8-6155] done synthesizing module 'rvsteel_gpio' (6#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/gpio/rvsteel_gpio.v:8]

INFO: [Synth 8-6157] synthesizing module 'rvsteel_spi' [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/spi/rvsteel_spi.v:8]

Parameter SPI_NUM_CHIP_SELECT bound to: 1 - type: integer

Parameter SPI_READY bound to: 4'b0001

Parameter SPI_IDLE bound to: 4'b0010

Parameter SPI_CPOL bound to: 4'b0100

Parameter SPI_CPOL_N bound to: 4'b1000

Parameter REG_CPOL bound to: 5'b00000

Parameter REG_CPHA bound to: 5'b00100

Parameter REG_CHIP_SELECT bound to: 5'b01000

Parameter REG_CLOCK_CONF bound to: 5'b01100

Parameter REG_WDATA bound to: 5'b10000

Parameter REG_RDATA bound to: 5'b10100

Parameter REG_BUSY bound to: 5'b11000

INFO: [Synth 8-6155] done synthesizing module 'rvsteel_spi' (7#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/spi/rvsteel_spi.v:8]

INFO: [Synth 8-6155] done synthesizing module 'rvsteel_mcu' (8#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mcu/rvsteel_mcu.v:8]

INFO: [Synth 8-6155] done synthesizing module 'hello_world_arty_a7' (9#1) [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7.v:8]

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Finished RTL Elaboration : Time (s): cpu = 00:00:00 ; elapsed = 00:00:03 . Memory (MB): peak = 496.117 ; gain = 163.977

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Report Check Netlist:

+------+------------------+-------+---------+-------+-----------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+-----------------+

|1 |multi_driven_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+-----------------+

WARNING: [Synth 8-3295] tying undriven pin rvsteel_mcu_instance:uart_rx to constant 0 [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7.v:34]

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:00 ; elapsed = 00:00:03 . Memory (MB): peak = 496.117 ; gain = 163.977

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:00 ; elapsed = 00:00:03 . Memory (MB): peak = 496.117 ; gain = 163.977

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INFO: [Device 21-403] Loading part xc7a100ticsg324-1L

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

Finished Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/hello_world_arty_a7_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/hello_world_arty_a7_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 863.000 ; gain = 0.000

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 863.000 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 863.000 ; gain = 0.000

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.006 . Memory (MB): peak = 863.000 ; gain = 0.000

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Finished Constraint Validation : Time (s): cpu = 00:00:02 ; elapsed = 00:00:11 . Memory (MB): peak = 863.000 ; gain = 530.859

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Start Loading Part and Timing Information

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Loading part: xc7a100ticsg324-1L

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:02 ; elapsed = 00:00:11 . Memory (MB): peak = 863.000 ; gain = 530.859

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Start Applying 'set_property' XDC Constraints

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Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:02 ; elapsed = 00:00:11 . Memory (MB): peak = 863.000 ; gain = 530.859

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INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel_core.v:1341]

INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel_core.v:1339]

INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel_core.v:1630]

INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel_core.v:459]

INFO: [Synth 8-802] inferred FSM for state register 'current_state_reg' in module 'rvsteel_core'

INFO: [Synth 8-5546] ROM "integer_file_reg[31]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[30]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[29]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[28]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[27]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[26]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[25]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[24]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[23]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[22]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[21]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[20]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[19]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[18]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[17]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[16]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[15]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[14]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[13]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[12]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[11]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[10]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[9]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[8]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[7]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[6]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[5]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[4]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[3]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[2]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[1]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5544] ROM "program_counter_source" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_mstatus_mpie" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_mcause" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "next_state" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5546] ROM "integer_file_reg[31]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[30]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[29]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[28]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[27]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[26]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[25]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[24]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[23]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[22]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[21]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[20]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[19]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[18]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[17]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[16]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[15]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[14]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[13]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[12]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[11]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[10]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[9]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[8]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[7]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[6]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[5]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[4]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[3]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[2]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "integer_file_reg[1]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5544] ROM "program_counter_source" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_mstatus_mpie" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_mcause" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "next_state" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_mepc" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_mtvec" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "rx_data0" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "rx_data0" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "tx_bit_counter" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "rx_bit_counter" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "rx_bit_counter0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "read_data" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-802] inferred FSM for state register 'curr_state_reg' in module 'rvsteel_spi'

INFO: [Synth 8-5545] ROM "cs0" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5544] ROM "next_state1" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "next_state1" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "next_state1" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "next_state1" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

---

State | New Encoding | Previous Encoding

---

*

STATE_RESET | 0001 | 0001

STATE_OPERATING | 0010 | 0010

STATE_TRAP_TAKEN | 0100 | 0100

STATE_TRAP_RETURN | 1000 | 1000

---

INFO: [Synth 8-3898] No Re-encoding of one hot register 'current_state_reg' in module 'rvsteel_core'

---

State | New Encoding | Previous Encoding

---

*

SPI_READY | 0001 | 0001

SPI_CPOL | 0100 | 0100

SPI_CPOL_N | 1000 | 1000

SPI_IDLE | 0010 | 0010

---

INFO: [Synth 8-3898] No Re-encoding of one hot register 'curr_state_reg' in module 'rvsteel_spi'

---

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:12 . Memory (MB): peak = 863.000 ; gain = 530.859

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

---

Start RTL Component Statistics

---

Detailed RTL Component Info :

+---Adders :

2 Input 64 Bit Adders := 4

3 Input 32 Bit Adders := 1

2 Input 32 Bit Adders := 8

2 Input 8 Bit Adders := 1

2 Input 4 Bit Adders := 3

+---XORs :

2 Input 32 Bit XORs := 1

2 Input 1 Bit XORs := 3

+---Registers :

64 Bit Registers := 5

32 Bit Registers := 46

16 Bit Registers := 2

10 Bit Registers := 1

8 Bit Registers := 7

5 Bit Registers := 2

4 Bit Registers := 4

1 Bit Registers := 40

+---RAMs :

64K Bit RAMs := 1

+---Muxes :

2 Input 64 Bit Muxes := 11

2 Input 32 Bit Muxes := 85

4 Input 32 Bit Muxes := 23

23 Input 32 Bit Muxes := 1

6 Input 32 Bit Muxes := 1

7 Input 32 Bit Muxes := 1

2 Input 31 Bit Muxes := 2

2 Input 24 Bit Muxes := 1

2 Input 16 Bit Muxes := 2

2 Input 10 Bit Muxes := 2

4 Input 8 Bit Muxes := 1

2 Input 8 Bit Muxes := 2

8 Input 5 Bit Muxes := 1

25 Input 5 Bit Muxes := 1

2 Input 5 Bit Muxes := 1

26 Input 5 Bit Muxes := 1

5 Input 4 Bit Muxes := 4

2 Input 4 Bit Muxes := 26

4 Input 4 Bit Muxes := 5

3 Input 4 Bit Muxes := 4

7 Input 3 Bit Muxes := 3

3 Input 3 Bit Muxes := 1

2 Input 3 Bit Muxes := 2

2 Input 2 Bit Muxes := 4

5 Input 2 Bit Muxes := 1

2 Input 1 Bit Muxes := 76

19 Input 1 Bit Muxes := 1

6 Input 1 Bit Muxes := 8

3 Input 1 Bit Muxes := 1

5 Input 1 Bit Muxes := 6

---

Finished RTL Component Statistics

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Start RTL Hierarchical Component Statistics

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Hierarchical RTL Component report

Module hello_world_arty_a7

Detailed RTL Component Info :

+---Registers :

1 Bit Registers := 2

Module rvsteel_core

Detailed RTL Component Info :

+---Adders :

2 Input 64 Bit Adders := 3

3 Input 32 Bit Adders := 1

2 Input 32 Bit Adders := 3

+---XORs :

2 Input 32 Bit XORs := 1

2 Input 1 Bit XORs := 2

+---Registers :

64 Bit Registers := 3

32 Bit Registers := 41

16 Bit Registers := 2

5 Bit Registers := 1

4 Bit Registers := 1

1 Bit Registers := 13

+---Muxes :

2 Input 64 Bit Muxes := 9

2 Input 32 Bit Muxes := 79

4 Input 32 Bit Muxes := 22

23 Input 32 Bit Muxes := 1

2 Input 31 Bit Muxes := 2

2 Input 24 Bit Muxes := 1

2 Input 16 Bit Muxes := 2

4 Input 8 Bit Muxes := 1

8 Input 5 Bit Muxes := 1

25 Input 5 Bit Muxes := 1

2 Input 5 Bit Muxes := 1

26 Input 5 Bit Muxes := 1

5 Input 4 Bit Muxes := 1

2 Input 4 Bit Muxes := 8

4 Input 4 Bit Muxes := 4

7 Input 3 Bit Muxes := 2

2 Input 2 Bit Muxes := 4

5 Input 2 Bit Muxes := 1

2 Input 1 Bit Muxes := 48

19 Input 1 Bit Muxes := 1

6 Input 1 Bit Muxes := 1

3 Input 1 Bit Muxes := 1

Module rvsteel_bus

Detailed RTL Component Info :

+---Adders :

2 Input 32 Bit Adders := 5

+---Registers :

5 Bit Registers := 1

+---Muxes :

2 Input 1 Bit Muxes := 1

Module rvsteel_ram

Detailed RTL Component Info :

+---Registers :

32 Bit Registers := 1

1 Bit Registers := 3

+---RAMs :

64K Bit RAMs := 1

+---Muxes :

2 Input 32 Bit Muxes := 6

2 Input 8 Bit Muxes := 1

Module rvsteel_uart

Detailed RTL Component Info :

+---Adders :

2 Input 4 Bit Adders := 2

+---Registers :

32 Bit Registers := 1

10 Bit Registers := 1

8 Bit Registers := 2

4 Bit Registers := 2

1 Bit Registers := 5

+---Muxes :

4 Input 32 Bit Muxes := 1

2 Input 10 Bit Muxes := 2

2 Input 8 Bit Muxes := 1

5 Input 4 Bit Muxes := 1

3 Input 4 Bit Muxes := 1

2 Input 4 Bit Muxes := 6

4 Input 4 Bit Muxes := 1

3 Input 3 Bit Muxes := 1

2 Input 1 Bit Muxes := 14

Module rvsteel_mtimer

Detailed RTL Component Info :

+---Adders :

2 Input 64 Bit Adders := 1

+---Registers :

64 Bit Registers := 2

32 Bit Registers := 1

1 Bit Registers := 4

+---Muxes :

2 Input 64 Bit Muxes := 2

6 Input 1 Bit Muxes := 6

2 Input 1 Bit Muxes := 2

Module rvsteel_gpio

Detailed RTL Component Info :

+---Registers :

32 Bit Registers := 1

1 Bit Registers := 4

+---Muxes :

6 Input 32 Bit Muxes := 1

6 Input 1 Bit Muxes := 1

5 Input 1 Bit Muxes := 4

2 Input 1 Bit Muxes := 4

Module rvsteel_spi

Detailed RTL Component Info :

+---Adders :

2 Input 8 Bit Adders := 1

2 Input 4 Bit Adders := 1

+---XORs :

2 Input 1 Bit XORs := 1

+---Registers :

32 Bit Registers := 1

8 Bit Registers := 5

4 Bit Registers := 1

1 Bit Registers := 9

+---Muxes :

7 Input 32 Bit Muxes := 1

3 Input 4 Bit Muxes := 3

2 Input 4 Bit Muxes := 12

5 Input 4 Bit Muxes := 2

2 Input 3 Bit Muxes := 2

7 Input 3 Bit Muxes := 1

2 Input 1 Bit Muxes := 7

5 Input 1 Bit Muxes := 2

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Finished RTL Hierarchical Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Warning: Parallel synthesis criteria is not met

INFO: [Synth 8-5544] ROM "csr_mcause" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "p_0_out" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "csr_minstret" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "rx_data0" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5545] ROM "cs0" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-3333] propagating constant 1 across sequential element (\rvsteel_mcu_instance/rvsteel_uart_instance/tx_register_reg[9] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[7] )

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[6]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[7]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[34] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[2] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[36] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[4] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[37] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[5] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[38] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[6] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[40] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[8] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[41] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[9] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[42] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[10] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[44] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[12] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[45] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[13] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[46] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[14] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[47] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[15] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[32] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[0] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[33] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[1] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[0] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[43] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[11] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[39] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[7] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[35] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[3] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[48] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[16] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[49] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[17] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[50] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[18] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[51] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[19] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[52] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[20] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[53] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[21] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[54] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[22] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[55] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[23] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[56] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[24] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[57] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[25] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[58] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[26] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[59] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[27] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[60] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[28] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[61] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[29] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[62] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[30] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[63] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_utime_reg[31] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mtvec_reg[1] )

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[30]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[28]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[30]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[31]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[28]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[29]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[28]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[31]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[29]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[27]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[29]' (FDR) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[24]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[27]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[31]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[27]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[31]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[31]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[26]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[31]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[26]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[26]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[25]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[26]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[25]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[25]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[21]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[25]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[23]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[21]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[23]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[21]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[23]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[23]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[24]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[23]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[19]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[24]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[22]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[24]' (FDR) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[22]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[22]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[20]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[22]' (FDR) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[20]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[20]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[19]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[20]' (FDR) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[17]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[19]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[18]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[19]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[18]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[18]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[17]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[18]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[16]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[17]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[15]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[17]' (FDR) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[14]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[15]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[16]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[15]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[16]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[16]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[11]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[16]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[13]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[11]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[10]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[11]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[13]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[10]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[9]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[10]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[13]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[9]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[8]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[9]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[13]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[8]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[13]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[8]' (FDR) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[14]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[13]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[14]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[13]' (FDS) to 'rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[12]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[14]' (FDR) to 'rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[12]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_spi_instance/read_data_reg[14] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_uart_instance/read_data_reg[12] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /csr_mip_meip_reg)

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /csr_mip_msip_reg)

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[1] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[2] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[3] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[4] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[5] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[6] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[7] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[8] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[9] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[10] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[11] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[12] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[13] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[14] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_core_instance /\csr_mip_mfip_reg[15] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[7] )

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[5]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[7]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[7]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[6]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[0]' (FD) to 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[1]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[1] )

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[2]' (FD) to 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[1]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[7] )

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[4]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[7]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[6]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[5]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[1] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[7] )

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[1]' (FD) to 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[3]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[3] )

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[5]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[4]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[4]' (FD) to 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[3]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[7]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[1]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[3]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[1]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[2]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[1]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[1] )

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[0]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[1]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[2]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[1]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[3]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[1]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[4]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[1]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[3] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_uart_instance/rx_register_reg[1] )

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[1]' (FDRE) to 'rvsteel_mcu_instance/rvsteel_uart_instance/rx_data_reg[0]'

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[3]' (FD) to 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[5]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[5] )

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[5]' (FD) to 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[6]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[6] )

INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[6]' (FD) to 'rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[7]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\rvsteel_mcu_instance/rvsteel_spi_instance/rx_reg_reg[7] )

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:30 ; elapsed = 00:02:09 . Memory (MB): peak = 938.801 ; gain = 606.660

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Start ROM, RAM, DSP and Shift Register Reporting

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Block RAM: Preliminary Mapping  Report (see note below)

+------------+-----------+----------------------+---+---+----------------------+---+---+-----------------+--------+--------+

|Module Name  | RTL Object | PORT A (Depth x Width) | W | R | PORT B (Depth x Width) | W | R | Ports driving FF | RAMB18 | RAMB36 |

+------------+-----------+----------------------+---+---+----------------------+---+---+-----------------+--------+--------+

|rvsteel_ram: | ram_reg    | 2 K x 32(READ_FIRST)   | W |   | 2 K x 32(WRITE_FIRST)  |   | R | Port A and B     | 0      | 2      |

+------------+-----------+----------------------+---+---+----------------------+---+---+-----------------+--------+--------+

Note: The table above is a preliminary report that shows the Block RAMs at the current stage of the synthesis flow. Some Block RAMs may be reimplemented as non Block RAM primitives later in the synthesis flow. Multiple instantiated Block RAMs are reported only once.

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Finished ROM, RAM, DSP and Shift Register Reporting

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INFO: [Synth 8-6837] The timing for the instance i_1/rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_0 (implemented as a Block RAM) might be

sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing.

INFO: [Synth 8-6837] The timing for the instance i_1/rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_1 (implemented as a Block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing.

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:33 ; elapsed = 00:02:15 . Memory (MB): peak = 938.801 ; gain = 606.660

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:40 ; elapsed = 00:02:33 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Start ROM, RAM, DSP and Shift Register Reporting

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Block RAM: Final Mapping  Report

+------------+------------+----------------------+---+---+----------------------+---+---+-----------------+--------+-----+

|Module Name | RTL Object | PORT A (Depth x Width) | W | R | PORT B (Depth x Width) | W | R | Ports driving FF | RAMB18 | RAMB36 |

+------------+-----------+----------------------+---+---+----------------------+---+---+-----------------+--------+--------+

|rvsteel_ram: | ram_reg | 2 K x 32(READ_FIRST) | W | | 2 K x 32(WRITE_FIRST) | | R | Port A and B | 0 | 2 |

+------------+-----------+----------------------+---+---+----------------------+---+---+-----------------+--------+--------+

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Finished ROM, RAM, DSP and Shift Register Reporting

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Report RTL Partitions:

+-+--------------+-----------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+-----------+----------+

+-+--------------+-----------+----------+

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Start Technology Mapping

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INFO: [Synth 8-3886] merging instance 'rvsteel_mcu_instance/rvsteel_ram_instance/reset_reg_reg' (FD) to 'rvsteel_mcu_instance/rvsteel_core_instance/reset_reg_reg'

INFO: [Synth 8-6837] The timing for the instance rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_0 (implemented as a Block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing.

INFO: [Synth 8-6837] The timing for the instance rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_1 (implemented as a Block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing.

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Finished Technology Mapping : Time (s): cpu = 00:00:43 ; elapsed = 00:02:42 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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---

Finished IO Insertion : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

|      |Item              |Errors |Warnings |Status |Description       |

+------+------------------+-------+---------+-------+------------------+

|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |

+------+-----------------+-------+---------+-------+-----------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Start Renaming Generated Ports

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---

Finished Renaming Generated Ports : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

---

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Start Handling Custom Attributes

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---

Finished Handling Custom Attributes : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Start Renaming Generated Nets

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---

Finished Renaming Generated Nets : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Start Writing Synthesis Report

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Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+----------+------+

| |Cell |Count |

+------+----------+------+

|1 |BUFG | 2|

|2 |CARRY4 | 158|

|3 |LUT1 | 11|

|4 |LUT2 | 94|

|5 |LUT3 | 263|

|6 |LUT4 | 416|

|7 |LUT5 | 584|

|8 |LUT6 | 1270|

|9 |MUXF7 | 339|

|10 |RAMB36E1 | 1|

|11 |RAMB36E1_1 | 1|

|12 |FDRE | 1680|

|13 |FDSE | 88|

|14 |IBUF | 2|

|15 |OBUF | 1|

+------+----------+------+

Report Instance Areas:

+------+--------------------------+--------------+------+

| |Instance |Module |Cells |

+------+--------------------------+--------------+------+

|1 |top | | 4910|

|2 | rvsteel_mcu_instance |rvsteel_mcu | 4902|

|3 | rvsteel_bus_instance |rvsteel_bus | 84|

|4 | rvsteel_core_instance |rvsteel_core | 4336|

|5 | rvsteel_gpio_instance |rvsteel_gpio | 5|

|6 | rvsteel_mtimer_instance |rvsteel_mtimer | 253|

|7 | rvsteel_ram_instance |rvsteel_ram | 4|

|8 | rvsteel_spi_instance |rvsteel_spi | 94|

|9 | rvsteel_uart_instance |rvsteel_uart | 124|

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:42 ; elapsed = 00:02:38 . Memory (MB): peak = 1157.637 ; gain = 458.613

Synthesis Optimization Complete : Time (s): cpu = 00:00:43 ; elapsed = 00:02:43 . Memory (MB): peak = 1157.637 ; gain = 825.496

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 499 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 1157.637 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

305 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth_design completed successfully

synth_design: Time (s): cpu = 00:00:44 ; elapsed = 00:02:46 . Memory (MB): peak = 1157.637 ; gain = 838.520

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1157.637 ; gain = 0.000

WARNING: [Constraints 18-5210] No constraints selected for write.

Resolution: This message can indicate that there are no constraints for the design, or it can indicate that the used_in flags are set such that the constraints are ignored. This later case is used when running synth_design to not write synthesis constraints to the resulting checkpoint. Instead, project constraints are read when the synthesized design is opened.

INFO: [Common 17-1381] The checkpoint 'C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/synth_1/hello_world_arty_a7.dcp' has been generated.

INFO: [runtcl-4] Executing : report_utilization -file hello_world_arty_a7_utilization_synth.rpt -pb hello_world_arty_a7_utilization_synth.pb

INFO: [Common 17-206] Exiting Vivado at Wed Oct 16 15:25:47 2024...