OPT DESIGN:

Design Rule Check (DRC) Report
Design Name: hello_world_arty_a7
Tool Version: Vivado v.2018.3 (64-bit)
Date: October 17, 2024
Host: Samuel (64-bit)
Device: xc7a100ticsg324-1L
Design State: Synthesized

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1. Introduction

This report documents the results of the Design Rule Check (DRC) performed on the synthesized design, "hello_world_arty_a7," using the Xilinx Vivado tool version 2018.3. The DRC ensures that the design meets all the necessary design rules and is ready for further stages, such as implementation and deployment.

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2. Tool and Environment Overview

- **Tool Version**: Vivado v.2018.3 (64-bit)
    - Build: 2405991
    - Build Date: December 6, 2018
- **Host System**: Samuel (64-bit operating system)
    - Build: 9200
- **Command Executed**:
    - report_drc -file hello_world_arty_a7_drc_opted.rpt -pb hello_world_arty_a7_drc_opted.pb -rpx hello_world_arty_a7_drc_opted.rpx

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3. Design Overview

- **Design Name**: hello_world_arty_a7
- **Device**: xc7a100ticsg324-1L
- **Design State**: Synthesized
- **Speed Grade**: -1L
- **Netlist**: netlist
- **Floorplan**: design_1

- **Design Limits**: The entire design was considered.

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4. DRC Summary

- **Ruledeck**: Default
- **Max Violations Allowed**: Unlimited
- **Violations Found**: 0 violations

The Design Rule Check (DRC) for the "hello_world_arty_a7" design was executed with the default ruledeck, which enforces all relevant design rules for the selected device (xc7a100ticsg324-1L). The DRC found no violations in the design, indicating that it complies with all applicable design rules.

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5. Report Details

There are no specific rule violations to report. The table below would typically summarize any issues, but since there were no violations, the table is empty.

Rule	Severity	Description	Violations
-	-	-	0

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6. Conclusion

The DRC for the design "hello_world_arty_a7" has successfully passed without any violations. This indicates that the design meets all the necessary design constraints and can proceed to the next stages of the design flow.

Pinout Report

1. Introduction

This report presents the pinout details for an FPGA device, summarizing the available pins, their electrical range, I/O assignments, and other relevant attributes. The data presented is useful for hardware engineers working on PCB designs or system integrations involving this FPGA.

2. Pinout Table

The following table provides a detailed description of each pin, including its name, range, I/O assignment, electrical characteristics, and any special notes where applicable.

Pinout Summary

Pin Name	Range	Pin Function	I/O Assignment	Associated Bank	Notes
P1	High Range	IO_L6P_T0_D05_14	User I/O	Bank 14	General purpose user I/O
P2	High Range	IO_L6N_T0_D04_14	User I/O	Bank 14	General purpose user I/O
P3	High Range	IO_L3N_T0_DQS_14	User I/O	Bank 14	Data strobe signal
P4	High Range	IO_L3P_T0_DQS_14	User I/O	Bank 14	Data strobe signal
P5	GND	GND	Ground	-	Ground pin
P6	High Range	IO_L1N_T0_AD0N_14	User I/O	Bank 14	Analog/Digital signal pin
P7	High Range	IO_L1P_T0_AD0P_14	User I/O	Bank 14	Analog/Digital signal pin
P8	VCCO_14	VCCO	Power	Bank 14	Any special VCCO requirements

Pin Name	Range	Pin Function	I/O Assignment	Associated Bank	Notes
P9	High Range	IO_L24N_T3_A00_D16_14	User I/O	Bank 14	Data signal pin
P10	High Range	IO_L24P_T3_A01_D17_14	User I/O	Bank 14	Data signal pin
P11	High Range	IO_L25N_T3_DQS_14	User I/O	Bank 14	Data strobe signal
P12	High Range	IO_L25P_T3_DQS_14	User I/O	Bank 14	Data strobe signal
P13	High Range	IO_L26N_T3_A02_D18_14	User I/O	Bank 14	Data signal pin
P14	GND	GND	Ground	-	Ground pin
P15	High Range	IO_L27P_T3_A03_D19_14	User I/O	Bank 14	Data signal pin
P16	High Range	IO_L27N_T3_A04_D20_14	User I/O	Bank 14	Data signal pin
P17	High Range	IO_L28P_T3_A05_D21_14	User I/O	Bank 14	Data signal pin
P18	High Range	IO_L9N_T1_DQS_D13_14	User I/O	Bank 14	Data strobe signal
R1	High Range	IO_L17P_T2_34	User I/O	Bank 34	General purpose user I/O
R2	High Range	IO_L15N_T2_DQS_34	User I/O	Bank 34	Data strobe signal
R3	High Range	IO_L11P_T1_SRCC_34	User I/O	Bank 34	Clock signal pin
R4	GND	GND	Ground	-	Ground pin

Pin Name	Range	Pin Function	I/O Assignment	Associated Bank	Notes
R5	High Range	IO_L19N_T3_VREF_34	User I/O	Bank 34	Voltage reference pin
R6	High Range	IO_L19P_T3_34	User I/O	Bank 34	General purpose user I/O
R7	High Range	IO_L23P_T3_34	User I/O	Bank 34	General purpose user I/O
R8	High Range	IO_L24P_T3_34	User I/O	Bank 34	General purpose user I/O
R9	Dedicated	VCCO_0	VCCO	Bank 0	Power supply for I/O banks
R10	High Range	IO_25_14	User I/O	Bank 14	General purpose user I/O
R11	High Range	IO_0_14	User I/O	Bank 14	General purpose user I/O
R12	High Range	IO_L5P_T0_D06_14	User I/O	Bank 14	Data signal pin
R13	High Range	IO_L5N_T0_D07_14	User I/O	Bank 14	Data signal pin
R14	GND	GND	Ground	-	Ground pin
R15	High Range	IO_L13N_T2_MRCC_14	User I/O	Bank 14	Clock signal pin
R16	High Range	IO_L15P_T2_DQS_RDWR_B_14	User I/O	Bank 14	Data strobe signal

Pin Name	Range	Pin Function	I/O Assignment	Associated Bank	Notes
R17	High Range	IO_L12N_T1_MRCC_14	User I/O	Bank 14	Clock signal pin
R18	High Range	IO_L7P_T1_D09_14	User I/O	Bank 14	Data signal pin
T1	High Range	IO_L17N_T2_34	User I/O	Bank 34	General purpose user I/O
T2	High Range	VCCO_34	VCCO	Bank 34	Power supply for I/O banks
T3	High Range	IO_L11N_T1_SRCC_34	User I/O	Bank 34	Clock signal pin
T4	High Range	IO_L12N_T1_MRCC_34	User I/O	Bank 34	Clock signal pin
T5	High Range	IO_L12P_T1_MRCC_34	User I/O	Bank 34	Clock signal pin
T6	High Range	IO_L23N_T3_34	User I/O	Bank 34	General purpose user I/O
T7	GND	GND	Ground	-	Ground pin
T8	High Range	IO_L24N_T3_34	User I/O	Bank 34	General purpose user I/O
T9	High Range	IO_L24P_T3_A01_D17_14	User I/O	Bank 14	Data signal pin
T10	High Range	IO_L24N_T3_A00_D16_14	User I/O	Bank 14	Data signal pin
T11	High Range	IO_L19P_T3_A10_D26_14	User I/O	Bank 14	Data signal pin

Pin Name	Range	Pin Function	I/O Assignment	Associated Bank	Notes
T12	High Range	VCCO_14	VCCO	Bank 14	Power supply for I/O banks
T13	High Range	IO_L23P_T3_A03_D19_14	User I/O	Bank 14	Data signal pin
T14	High Range	IO_L14P_T2_SRCC_14	User I/O	Bank 14	Clock signal pin
T15	High Range	IO_L14N_T2_SRCC_14	User I/O	Bank 14	Clock signal pin
T16	High Range	IO_L16P_T2_A07_D23_14	User I/O	Bank 14	Data signal pin
T17	GND	GND	Ground	-	Ground pin
T18	High Range	VCCO_34	VCCO	Bank 34	Power supply for I/O banks

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3. Special Considerations

- **VCCO Requirements:** Some VCCO pins are marked with special requirements. These pins should be treated with care to ensure the proper functioning of the corresponding I/O bank.
- **Ground (GND):** Pins marked as GND should be connected to the system ground. These pins are critical for maintaining the device's electrical stability.
- **Clock Signal Pins:** Certain pins are designated for clock signals (e.g., IO_L11P_T1_SRCC_34). It is essential to use these pins correctly in timing-sensitive applications.
- **Data Strobe (DQS) Pins:** Pins labelled as DQS are data strobe signals, used in certain memory and data bus interfaces for synchronizing data transfer.

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4. Conclusion

- This report provides an exhaustive view of the pin configuration for the FPGA device, offering guidance on how each pin should be used in a design. For more detailed electrical specifications, please refer to the device datasheet or family documentation. Proper assignment of I/O, power, and ground pins is essential for the stable and efficient operation of the FPGA in any embedded or hardware system.

Vivado Bus Skew and DRC Report

Tool Information

- **Tool Version:** Vivado v.2018.3 (win64)
- **Build Date:** December 6, 2018
- **Date of Report:** October 17, 2024

- **Host:** Samuel (64-bit major release)
- **Design:** hello_world_arty_a7
- **Device:** xc7a100ti

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1. Bus Skew Report

- **Bus Skew Constraints:** None specified
- **Result:** No violations or issues found related to bus skew.

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2. DRC Report Summary

- **Netlist:** netlist
- **Floorplan:** design_1
- **Design Limits:** Entire design considered
- **Ruledeck:** default
- **Max Violations:** Unlimited
- **Violations Found:** 0

DRC Violations Summary

Rule	Severity	Description	Violations
(none)	(none)	(none)	0

Vivado Methodology and Power Report Summary

Tool Information

- **Tool Version:** Vivado v.2018.3 (win64)
- **Build Date:** December 6, 2018
- **Date of Report:** October 17, 2024
- **Host:** Samuel (64-bit major release)
- **Design:** hello_world_arty_a7
- **Device:** xc7a100ti

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1. Methodology Report

Summary

- **Netlist:** netlist

- **Floorplan:** design_1
- **Design Limits:** Entire design considered
- **Violations Found:** 2

Violations Summary

Rule	Severity	Description	Violations
SYNTH-6	Warning	Timing of a block RAM might be sub-optimal	2

Details of Violations

1. **SYNTH-6#1**: The timing for rvsteel_ram_instance/ram_reg_0 might be sub-optimal as no output register was merged into the block.
2. **SYNTH-6#2**: The timing for rvsteel_ram_instance/ram_reg_1 might be sub-optimal for the same reason.

Design Route Status

- Total Logical Nets: 5418
- Fully Routed Nets: 3877
- Routing Errors: 0

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2. Power Report

Summary

- **Total On-Chip Power:** 0.080 W
- **Dynamic Power:** 0.009 W
- **Static Power:** 0.071 W
- **Max Ambient Temperature:** 99.6 °C
- **Junction Temperature:** 25.4 °C
- **Confidence Level:** Medium

On-Chip Components Power Consumption

Component	Power (W)	Used	Utilization (%)
Clocks	0.003	4	-
Slice Logic	0.002	4916	-

Component	Power (W)	Used	Utilization (%)
Block RAM	0.002	2	1.48
I/O	<0.001	3	1.43
Total	**0.080**		

Power Supply Summary

Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	0.950	0.019	0.010	0.009
Vccaux	1.800	0.016	0.000	0.016
Vccadc	1.800	0.018	0.000	0.018

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3. Confidence Level

- **Design Implementation State:** High (Design is routed)
- **Clock Nodes Activity:** High (More than 95% of clocks specified)
- **I/O Nodes Activity:** Medium (Missing specification for >5% of inputs)
- **Internal Nodes Activity:** Medium (Specified for <25% of internal nodes)
- **Overall Confidence Level:** Medium

Conclusion

The design **hello_world_arty_a7** has some warnings related to block RAM timing, which might affect performance. However, the power consumption is low, and the overall design state is acceptable with no routing errors.

Implementation Report

Project Overview

Project Name: Hello World
Target Device: XC7A100T-1CSG324
Location: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscvsteel/examples/hello_world/boards/arty_a7/

Implementation Phases

1. Synthesis Phase

- **Start Time:** 00:00:00
- **End Time:** 00:00:05
- **Elapsed Time:** 5 seconds
- **Peak Memory Usage:** 1493.020 MB
- **Warnings:** 0
- **Errors:** 0

2. Placement Phase

2.1 Pipeline Register Optimization

- **Elapsed Time:** 7 seconds
- **Peak Memory Usage:** 1493.020 MB

2.2 Post Placement Optimization

- **Elapsed Time:** 10 seconds
- **Peak Memory Usage:** 1493.020 MB
- **Post Placement Timing Summary:**
    - **WNS:** 0.652

3. Routing Phase

- **Start Time:** 00:00:20
- **End Time:** 00:00:44
- **Elapsed Time:** 24 seconds
- **Peak Memory Usage:** 1592.492 MB

3.1 Routing Initialization

- **Elapsed Time:** 20 seconds
- **Nodes with overlaps:**
    - Initial: 2219
    - Final: 0
- **Intermediate Timing Summary:**
    - **WNS:** 0.512

    - **TNS:** 0.000

4. Post Routing Analysis

- **DRC Report Location:** C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscvsteel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/runs/impl_1/hello_world_arty_a7_drc_routed.rpt
- **Methodology Report Location:** C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscvsteel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/runs/impl_1/hello_world_arty_a7_methodology_drc_routed.rpt
- **Power Report Location:** C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscvsteel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/runs/impl_1/hello_world_arty_a7_power_routed.rpt

Summary of Results

- **Total Implementation Time:** 44 seconds
- **Total Warnings:** 0
- **Total Errors:** 0
- **Final Timing Summary:**
    - **WNS:** 0.512
    - **TNS:** 0.000

Conclusion

The design implementation for the Hello World project targeting the XC7A100T-1CSG324 FPGA was completed successfully without any warnings or errors. The timing analysis indicates that the design meets the required specifications, with the worst negative slack (WNS) being positive.

FPGA Utilization Report

Tool Version: Vivado v.2018.3
Design: hello_world_arty_a7
Device: 7a100ticsg324-1L
Design State: Fully Placed
Date: Thu Oct 17 09:48:08 2024
Host: Samuel running 64-bit major release (build 9200)

1. Slice Logic

Summary of Utilization

Site Type	Used	Available	Util%
Slice LUTs	2394	63400	3.78
Slice Registers	1768	126800	1.39
F7 Muxes	339	31700	1.07
F8 Muxes	0	15850	0.00

Summary of Registers by Type

Total Registers	Clock Enable	Synchronous	Asynchronous
0	-	-	-
0	-	-	Set
0	-	-	Reset
0	Yes	-	-
88	Yes	Set	-

Total Registers	Clock Enable	Synchronous	Asynchronous
1680	Yes	Reset	-

2. Slice Logic Distribution

Site Type	Used	Available	Util%
Slice	843	15850	5.32
LUT as Logic	2394	63400	3.78
Slice Registers	1768	126800	1.39
Unique Control Sets	62	15850	0.39

3. Memory

Site Type	Used	Available	Util%
Block RAM Tile	2	135	1.48

4. DSP

Site Type	Used	Available	Util%
DSPs	0	240	0.00

5. I/O and GT Specific

Site Type	Used	Available	Util%
Bonded IOB	3	210	1.43

6. Clocking

Site Type	Used	Available	Util%
BUFGCTRL	2	32	6.25

7. Specific Feature

Site Type	Used	Available	Util%
BSCANE2	0	4	0.00

8. Primitives

Ref Name	Used	Functional Category
FDRE	1680	Flop & Latch
LUT6	1270	LUT
MUXF7	339	MuxFx
RAMB36E1	2	Block Memory

9. Black Boxes

Ref Name	Used
-	0

10. Instantiated Netlists

Ref Name	Used
-	0

Conclusion

The FPGA design demonstrates efficient utilization, with most resources well below their limits. This indicates that there is significant room for expansion or optimization in your design. You may also consider evaluating the usage of DSPs and Block RAM, as their utilization is currently low.

Vivado Control Set Report

Tool Information

- **Tool Version:** Vivado v.2018.3 (win64)
- **Build Date:** December 6, 2018
- **Date of Report:** October 17, 2024
- **Host:** Samuel (64-bit major release)
- **Design:** hello_world_arty_a7
- **Device:** xc7a100ti

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1. Summary

- **Number of Unique Control Sets:** 62
- **Unused Register Locations in Slices Containing Registers:** 72

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2. Histogram of Control Sets by Fanout

Fanout	Control Sets
1	1
4	3
5	2
6	1
8	3
9	2
13	1
14	1
16+	**48**

3. Flip-Flop Distribution

Clock Enable	Synchronous Set/Reset	Asynchronous Set/Reset	Total Registers	Total Slices
No	No	No	23	16
No	No	Yes	0	0
No	Yes	No	188	70
Yes	No	No	9	5
Yes	No	Yes	0	0
Yes	Yes	No	1548	565

4. Detailed Control Set Information

Clock Signal	Enable Signal	Set/Reset Signal	Slice Load Count	Bel Load Count
clock_IBUF_BUFG			1	1
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/current_state[3]_i_2_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	1	4
clock_50mhz_BUFG		rvsteel_mcu_instance/rvsteel_spi_instance/curr_state0	3	4
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_spi_instance/bit_count[3]_i_2_n_0	rvsteel_mcu_instance/rvsteel_spi_instance/cycle_counter1	1	4

Clock Signal	Enable Signal	Set/Reset Signal	Slice Load Count	Bel Load Count
clock_50mhz_BUFG		rvsteel_mcu_instance/rvsteel_core_instance/prev_write_request_reg_1[0]	5	5
clock_50mhz_BUFG		rvsteel_mcu_instance/rvsteel_uart_instance/reset_internal	3	5
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/csr_mcause[31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	6	6
clock_50mhz_BUFG		rvsteel_mcu_instance/rvsteel_spi_instance/cycle_counter[7]_i_1_n_0	2	8
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/mtimecmp[31]_i_2_0[0]	reset_debounced	2	8
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/prev_rw_address_reg[3]_0[0]	reset_debounced	3	8
clock_50mhz_BUFG		rvsteel_mcu_instance/rvsteel_core_instance/SR[0]	3	9
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_uart_instance/tx_register		5	9
clock_50mhz_BUFG		rvsteel_mcu_instance/rvsteel_uart_instance/tx_register	4	13

Clock Signal	Enable Signal	Set/Reset Signal	Slice Load Count	Bel Load Count
clock_50mhz_BUFG		reset_debounced	7	14
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/csr_mie_mfie0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	7	19
clock_50mhz_BUFG			15	22
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/csr_mcause[31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/csr_mcause[30]_i_1_n_0	18	26
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/csr_mepc[31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	8	30
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_bus_instance/E[0]	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	15	31
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/csr_mtvec1	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	18	31
clock_50mhz_BUFG		rvsteel_mcu_instance/rvsteel_uart_instance/rx_cycle_counter[0]_i_1_n_0	8	32
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/integer_file[15][31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	13	32

Clock Signal	Enable Signal	Set/Reset Signal	Slice Load Count	Bel Load Count
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/csr_minstret[31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	8	32
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval[31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	19	32
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/integer_file[23][31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	11	32
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/csr_minstret[63]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	8	32
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/csr_mscratch0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	19	32
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/integer_file[3][31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	9	32
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/integer_file[21][31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	14	32
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/integer_file[11][31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	12	32
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/integer_file[17][31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	12	32

Clock Signal	Enable Signal	Set/Reset Signal	Slice Load Count	Bel Load Count
clock_50mhz_BUFG	rvsteel_mcu_instance/rvsteel_core_instance/integer_file[10][31]_i_1_n_0	rvsteel_mcu_instance/rvsteel_core_instance/reset_internal_1	9	32

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5. Conclusion

This report provides a comprehensive overview of the control set information for the hello_world_arty_a7 design. The detailed analysis of control sets by fanout, flip-flop distribution, and clock, enable, and reset signals can help in further optimization and design validation processes.