Tool Version : Vivado v.2018.3 (win64) Build 2405991 Thu Dec 6 23:38:27 MST 2018
Date : Thu Oct 17 09:45:18 2024
Host : Samuel running 64-bit major release (build 9200)
Command : report_utilization -file hello_world_arty_a7_utilization_synth.rpt -pb hello_world_arty_a7_utilization_synth.pb
Design : hello_world_arty_a7
Device : 7a100ticsg324-1L
Design State : Synthesized
Utilization Design Information
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1.1 Summary of Registers by Type

```
+-----+
```

| Total | Clock Enable | Synchronous | Asynchronous |

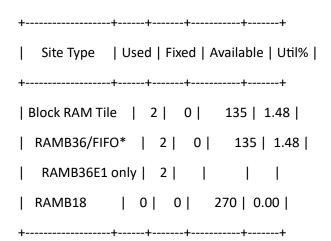
+-----+

```
|0 | _| -| -|
|0 | _| -| Set |
| 0 | _ | - | Reset |
| 0 | _ | Set | |
|---|---|---|---|
| 0 | _ | Reset | - |
0 |
       Yes |
           - | - |
0 |
       Yes |
           - | Set |
0 |
       Yes |
             - |
                 Reset |
| 88 |
       Yes
             Set | - |
| 1680 |
             Reset | - |
        Yes |
```

^{*} Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

+----+

2. Memory



^{*} Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

4. IO and GT Specific

```
Site Type | Used | Fixed | Available | Util% |
| Bonded IOB
             | 3 | 0 | 210 | 1.43 |
| Bonded IPADs
            | 0 | 0 | 2 | 0.00 |
             | 0 | 0 | 6 | 0.00 |
| PHY_CONTROL
| PHASER_REF
             | 0 | 0 | 6 | 0.00 |
OUT_FIFO
            | 0 | 0 | 24 | 0.00 |
| IN_FIFO
           | 0 | 0 | 24 | 0.00 |
| IDELAYCTRL
           | 0 | 0 | 6 | 0.00 |
| IBUFDS
            | 0 | 0 | 202 | 0.00 |
| PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 24 | 0.00 |
| ILOGIC
       | 0 | 0 | 210 | 0.00 |
| OLOGIC
          | 0 | 0 | 210 | 0.00 |
```

5. Clocking

```
+----+
| Site Type | Used | Fixed | Available | Util% |
+-----+
| BUFGCTRL | 2 | 0 | 32 | 6.25 |
| BUFIO | 0 | 0 | 24 | 0.00 |
| MMCME2_ADV | 0 | 0 | 6 | 0.00 |
| PLLE2_ADV | 0 | 0 | 6 | 0.00 |
| BUFMRCE | 0 | 0 | 12 | 0.00 |
```

```
| BUFR | 0 | 0 | 24 | 0.00 |
+----+
6. Specific Feature
+----+
| Site Type | Used | Fixed | Available | Util% |
+----+
| BSCANE2 | 0 | 0 | 4 | 0.00 |
| CAPTUREE2 | 0 | 0 | 1 | 0.00 |
| DNA_PORT | 0 | 0 | 1 | 0.00 |
| EFUSE_USR | 0 | 0 | 1 | 0.00 |
| FRAME_ECCE2 | 0 | 0 | 1 | 0.00 |
| ICAPE2 | 0 | 0 | 2 | 0.00 |
| PCIE_2_1 | 0 | 0 | 1 | 0.00 |
| STARTUPE2 | 0 | 0 | 1 | 0.00 |
| XADC | 0 | 0 | 1 | 0.00 |
+-----+
7. Primitives
-----
+----+
| Ref Name | Used | Functional Category |
+----+
| FDRE | 1680 | Flop & Latch |
```

| LUT6 | 1270 |

| LUT5 | 584 | LUT |

LUT |

```
| LUT4 | 416 | LUT |
| MUXF7 | 339 |
                 MuxFx |
| LUT3 | 263 |
                LUT |
| CARRY4 | 158 | CarryLogic |
| LUT2 | 94 |
                LUT |
| FDSE | 88 | Flop & Latch |
|LUT1 | 11 | LUT |
| RAMB36E1 | 2 |
                Block Memory |
| IBUF | 2 |
                10 |
| BUFG | 2 |
               Clock |
| OBUF | 1 |
                10 |
+----+
```



+----+

| Ref Name | Used |

+----+

9. Instantiated Netlists

+----+

| Ref Name | Used |

+----+