start_gui

source "C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/create_project_arty_a7_100t.tcl"

cd [file normalize [file dirname [info script]]]

create_project hello_world_arty_a7_100t ./hello_world_arty_a7_100t -part xc7a100ticsg324-1L -force

INFO: [ProjectBase 1-489] The host OS only allows 260 characters in a normal path. The project is stored in a path with more than 80 characters. If you experience issues with IP, Block Designs, or files not being found, please consider moving the project to a location with a shorter path. Alternately consider using the OS subst command to map part of the path to a drive letter.

Current project path is 'C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t'

INFO: [IP_Flow 19-234] Refreshing IP repositories

INFO: [IP_Flow 19-1704] No user IP repositories specified

INFO: [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.3/data/ip'.

create_project: Time (s): cpu = 00:00:06 ; elapsed = 00:00:11 . Memory (MB): peak = 818.469 ; gain = 221.898

set_msg_config -suppress -id {Synth 8-7080}

set_msg_config -suppress -id {Power 33-332}

set_msg_config -suppress -id {Pwropt 34-321}

set_msg_config -suppress -id {Synth 8-6841}

set_msg_config -suppress -id {Netlist 29-101}

set_property simulator_language Verilog [current_project]

add_files -fileset constrs_1 -norecurse { ./hello_world_arty_a7_constraints.xdc }

add_files -norecurse .

add_files -norecurse { ../../../../hardware/mcu/ }

add_files -norecurse { ../../software/build/hello_world.hex }

set_property file_type {Memory Initialization Files} [get_files ../../software/build/hello_world.hex]

update_compile_order -fileset sources_1

update_compile_order -fileset sources_1

add_files -norecurse {{C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/gpio/rvsteel_gpio.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/spi/rvsteel_spi.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/bus/rvsteel_bus.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mcu/rvsteel_mcu.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mtimer/rvsteel_mtimer.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel_core.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/ram/rvsteel_ram.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/uart/rvsteel_uart.v}}

WARNING: [filemgmt 56-12] File 'C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mcu/rvsteel_mcu.v' cannot be added to the project because it already exists in the project, skipping this file

update_compile_order -fileset sources_1

launch_runs synth_1 -jobs 8

[Fri Oct 18 10:06:39 2024] Launched synth_1...

Run output will be captured here: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/synth_1/runme.log

open_run synth_1 -name synth_1

Design is defaulting to impl run constrset: constrs_1

Design is defaulting to synth run part: xc7a100ticsg324-1L

INFO: [Netlist 29-17] Analyzing 499 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100ticsg324-1L

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

Finished Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1130.594 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

open_run: Time (s): cpu = 00:00:05 ; elapsed = 00:00:08 . Memory (MB): peak = 1317.855 ; gain = 479.656

report_power -name {power_1}

Command: report_power -name power_1

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

1 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

report_power completed successfully

launch_runs impl_1 -jobs 8

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 1858.746 ; gain = 0.000

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.045 . Memory (MB): peak = 1858.746 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1863.742 ; gain = 0.000

[Fri Oct 18 10:23:47 2024] Launched impl_1...

Run output will be captured here: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/impl_1/runme.log

close_design

open_run impl_1

INFO: [Netlist 29-17] Analyzing 499 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.286 . Memory (MB): peak = 1879.430 ; gain = 0.000

Restored from archive | CPU: 1.000000 secs | Memory: 0.000000 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.286 . Memory (MB): peak = 1879.430 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1879.430 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

open_run synth_1 -name synth_1

Design is defaulting to impl run constrset: constrs_1

Design is defaulting to synth run part: xc7a100ticsg324-1L

INFO: [Netlist 29-17] Analyzing 499 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

Finished Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 2179.188 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

report_timing_summary -delay_type min_max -report_unconstrained -check_timing_verbose -max_paths 10 -input_pins -routable_nets -name timing_1

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

report_timing -max_paths 1 -nworst 1 -delay_type max -sort_by slack

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

INFO: [Timing 38-78] ReportTimingParams: -max_paths 1 -nworst 1 -delay_type max -sort_by slack.

| Tool Version : Vivado v.2018.3 (win64) Build 2405991 Thu Dec 6 23:38:27 MST 2018

| Date   : Fri Oct 18 10:31:17 2024

| Host   : Samuel running 64-bit major release (build 9200)

| Command   : report_timing -max_paths 1 -nworst 1 -delay_type max -sort_by slack

| Design   : hello_world_arty_a7

| Device   : 7a100ti-csg324

| Speed File   : -1L PRODUCTION 1.23 2018-06-13

Timing Report

Slack (MET) : 2.584ns (required time - arrival time)

Source: rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_0/CLKBWRCLK

(rising edge-triggered cell RAMB36E1 clocked by clkdiv2 {rise@0.000ns fall@10.000ns period=20.000ns})

Destination: rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save_reg[0]/R

(rising edge-triggered cell FDRE clocked by clkdiv2 {rise@0.000ns fall@10.000ns period=20.000ns})

Path Group: clkdiv2

Path Type: Setup (Max at Slow Process Corner)

Requirement: 20.000ns (clkdiv2 rise@20.000ns - clkdiv2 rise@0.000ns)

Data Path Delay: 16.679ns (logic 6.708ns (40.219%) route 9.971ns (59.781%))

Logic Levels: 24 (CARRY4=7 LUT2=2 LUT3=2 LUT4=2 LUT5=5 LUT6=6)

Clock Path Skew: -0.145ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 4.523ns = (24.523 - 20.000)

Source Clock Delay (SCD): 5.101ns

Clock Pessimism Removal (CPR): 0.433ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
	(clock clkdiv2 rise edge)	0.000	0.000 r	
E3		0.000	0.000 r	clock (IN)
	net (fo=0)	0.000	0.000	clock
E3	IBUF (Prop_ibuf_I_O)	1.482	1.482 r	clock_IBUF_inst/O
	net (fo=1, unplaced)	0.803	2.285	clock_IBUF
	BUFG (Prop_bufg_I_O)	0.096	2.381 r	clock_IBUF_BUFG_inst/O
	net (fo=1, unplaced)	0.584	2.965	clock_IBUF_BUFG
	FDRE (Prop_fdre_C_Q)	0.478	3.443 r	clock_50mhz_reg/Q
	net (fo=2, unplaced)	0.803	4.246	clock_50mhz

BUFG (Prop_bufg_I_O) 0.271 4.517 r clock_50mhz_BUFG_inst/O

net (fo=1771, unplaced) 0.584 5.101 rvsteel_mcu_instance/rvsteel_ram_instance/clock_50mhz_BUFG

RAMB36E1 r rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_0/CLKBWRCLK

RAMB36E1 (Prop_ramb36e1_CLKBWRCLK_DOBDO[1])

2.454 7.555 f rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_0/DOBDO[1]

net (fo=1, unplaced) 0.803 8.357 rvsteel_mcu_instance/rvsteel_bus_instance/device_read_data[1]

LUT6 (Prop_lut6_I1_O) 0.124 8.481 f rvsteel_mcu_instance/rvsteel_bus_instance/prev_instruction[1]_i_2/O

net (fo=4, unplaced) 0.756 9.237 rvsteel_mcu_instance/rvsteel_core_instance/manager_read_data[1]

LUT6 (Prop_lut6_I1_O) 0.124 9.361 r rvsteel_mcu_instance/rvsteel_core_instance/integer_file[30][31]_i_21/O

net (fo=8, unplaced) 0.487 9.848 rvsteel_mcu_instance/rvsteel_core_instance/integer_file[30][31]_i_21_n_0

LUT5 (Prop_lut5_I4_O) 0.124 9.972 f rvsteel_mcu_instance/rvsteel_core_instance/current_state[3]_i_23/O

net (fo=4, unplaced) 0.473 10.445 rvsteel_mcu_instance/rvsteel_core_instance/current_state[3]_i_23_n_0

LUT5 (Prop_lut5_I2_O) 0.124 10.569 f rvsteel_mcu_instance/rvsteel_core_instance/current_state[3]_i_12/O

net (fo=9, unplaced) 0.490 11.059 rvsteel_mcu_instance/rvsteel_core_instance/system_type

LUT3 (Prop_lut3_I0_O) 0.124 11.183 f rvsteel_mcu_instance/rvsteel_core_instance/csr_mie_msie_i_10/O

net (fo=5, unplaced) 0.477 11.660 rvsteel_mcu_instance/rvsteel_core_instance/csrxxx

LUT6 (Prop_lut6_I2_O) 0.124 11.784 r rvsteel_mcu_instance/rvsteel_core_instance/csr_mie_msie_i_11/O

net (fo=33, unplaced) 0.521 12.305 rvsteel_mcu_instance/rvsteel_core_instance/immediate_type[0]

LUT4 (Prop_lut4_I2_O) 0.124 12.429 r rvsteel_mcu_instance/rvsteel_core_instance/csr_mscratch[0]_i_5/O

net (fo=1, unplaced) 0.449 12.878 rvsteel_mcu_instance/rvsteel_core_instance/csr_mscratch[0]_i_5_n_0

LUT5 (Prop_lut5_I0_O) 0.124 13.002 r rvsteel_mcu_instance/rvsteel_core_instance/csr_mscratch[0]_i_2/O

net (fo=5, unplaced) 0.477 13.479 rvsteel_mcu_instance/rvsteel_core_instance/immediate[0]

LUT5 (Prop_lut5_I3_O) 0.124 13.603 r rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval[3]_i_6/O

net (fo=1, unplaced) 0.000 13.603
rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval[3]_i_6_n_0

CARRY4 (Prop_carry4_S[0]_CO[3])

0.513 14.116 r
rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[3]_i_2/CO[3]

net (fo=1, unplaced) 0.000 14.116
rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[3]_i_2_n_0

CARRY4 (Prop_carry4_CI_CO[3])

0.117 14.233 r
rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[7]_i_2/CO[3]

net (fo=1, unplaced) 0.000 14.233
rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[7]_i_2_n_0

CARRY4 (Prop_carry4_CI_CO[3])

0.117 14.350 r
rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[11]_i_2/CO[3]

net (fo=1, unplaced) 0.000 14.350
rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[11]_i_2_n_0

CARRY4 (Prop_carry4_CI_O[1])

0.337 14.687 f
rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[15]_i_2/O[1]

net (fo=4, unplaced) 0.635 15.322
rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[15]_i_2_n_6

LUT5 (Prop_lut5_I0_O) 0.306 15.628 f
rvsteel_mcu_instance/rvsteel_core_instance/program_counter[13]_i_2/O

net (fo=1, unplaced) 0.449 16.077
rvsteel_mcu_instance/rvsteel_core_instance/program_counter[13]_i_2_n_0

LUT6 (Prop_lut6_I0_O) 0.124 16.201 f
rvsteel_mcu_instance/rvsteel_core_instance/program_counter[13]_i_1/O

net (fo=2, unplaced) 0.460 16.661
rvsteel_mcu_instance/rvsteel_core_instance/next_program_counter[13]

LUT4 (Prop_lut4_I0_O) 0.124 16.785 f
rvsteel_mcu_instance/rvsteel_core_instance/prev_instruction_address[13]_i_1/O

net (fo=2, unplaced) 0.460 17.245
rvsteel_mcu_instance/rvsteel_core_instance/prev_instruction_address[13]_i_1_n_0

LUT6 (Prop_lut6_I0_O) 0.124 17.369 f
rvsteel_mcu_instance/rvsteel_core_instance/prev_rw_address[13]_i_1/O

net (fo=2, unplaced) 0.430 17.799
rvsteel_mcu_instance/rvsteel_core_instance/prev_rw_address[13]_i_1_n_0

LUT2 (Prop_lut2_I0_O) 0.124 17.923 f
rvsteel_mcu_instance/rvsteel_core_instance/ram_reg_0_i_6/O

net (fo=6, unplaced) 0.481 18.404
rvsteel_mcu_instance/rvsteel_core_instance/ram_reg_0_i_6_n_0

LUT2 (Prop_lut2_I0_O) 0.124 18.528 r
rvsteel_mcu_instance/rvsteel_core_instance/i__carry_i_1__2/O

net (fo=1, unplaced) 0.000 18.528
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry__0_0[3]

CARRY4 (Prop_carry4_S[3]_CO[3])

0.376 18.904 r
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry/CO[3]

net (fo=1, unplaced) 0.000 18.904
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry_n_0

CARRY4 (Prop_carry4_CI_CO[3])

0.117 19.021 r
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry__0/CO[3]

net (fo=1, unplaced) 0.000 19.021
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry__0_n_0

CARRY4 (Prop_carry4_CI_CO[1])

0.179 19.200 f
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry__1/CO[1]

net (fo=9, unplaced) 1.038 20.238 rvsteel_mcu_instance/rvsteel_bus_instance/device_sel[3]

LUT6 (Prop_lut6_I0_O) 0.332 20.570 r
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save[4]_i_2/O

net (fo=1, unplaced) 0.449 21.019
rvsteel_mcu_instance/rvsteel_core_instance/device_sel_save_reg[4]

LUT3 (Prop_lut3_I2_O) 0.124 21.143 r
rvsteel_mcu_instance/rvsteel_core_instance/device_sel_save[4]_i_1/O

net (fo=5, unplaced) 0.636 21.779 rvsteel_mcu_instance/rvsteel_bus_instance/SR[0]

FDRE r rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save_reg[0]/R

(clock clkdiv2 rise edge) 20.000 20.000 r

E3 0.000 20.000 r clock (IN)

net (fo=0) 0.000 20.000 clock

E3 IBUF (Prop_ibuf_I_O) 1.411 21.411 r clock_IBUF_inst/O

net (fo=1, unplaced) 0.763 22.174 clock_IBUF

BUFG (Prop_bufg_I_O) 0.091 22.265 r clock_IBUF_BUFG_inst/O

net (fo=1, unplaced) 0.439 22.704 clock_IBUF_BUFG

FDRE (Prop_fdre_C_Q) 0.385 23.089 r clock_50mhz_reg/Q

net (fo=2, unplaced) 0.763 23.852 clock_50mhz

BUFG (Prop_bufg_I_O) 0.232 24.084 r clock_50mhz_BUFG_inst/O

net (fo=1771, unplaced) 0.439 24.523 rvsteel_mcu_instance/rvsteel_bus_instance/clock_50mhz_BUFG

FDRE r rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save_reg[0]/C

clock pessimism 0.433 24.956

clock uncertainty -0.035 24.920

FDRE (Setup_fdre_C_R) -0.557 24.363 rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save_reg[0]

---

required time 24.363

arrival time -21.779

---

slack 2.584

start_gui

source "C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/create_project_arty_a7_100t.tcl"

cd [file normalize [file dirname [info script]]]

create_project hello_world_arty_a7_100t ./hello_world_arty_a7_100t -part xc7a100ticsg324-1L -force

INFO: [ProjectBase 1-489] The host OS only allows 260 characters in a normal path. The project is stored in a path with more than 80 characters. If you experience issues with IP, Block Designs, or files not being found, please consider moving the project to a location with a shorter path. Alternately consider using the OS subst command to map part of the path to a drive letter.

Current project path is 'C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t'

INFO: [IP_Flow 19-234] Refreshing IP repositories

INFO: [IP_Flow 19-1704] No user IP repositories specified

INFO: [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.3/data/ip'.

create_project: Time (s): cpu = 00:00:06 ; elapsed = 00:00:11 . Memory (MB): peak = 818.469 ; gain = 221.898

set_msg_config -suppress -id {Synth 8-7080}

set_msg_config -suppress -id {Power 33-332}

set_msg_config -suppress -id {Pwropt 34-321}

set_msg_config -suppress -id {Synth 8-6841}

set_msg_config -suppress -id {Netlist 29-101}

set_property simulator_language Verilog [current_project]

add_files -fileset constrs_1 -norecurse { ./hello_world_arty_a7_constraints.xdc }

add_files -norecurse .

add_files -norecurse { ../../../../hardware/mcu/ }

add_files -norecurse { ../../software/build/hello_world.hex }

set_property file_type {Memory Initialization Files} [get_files ../../software/build/hello_world.hex]

update_compile_order -fileset sources_1

update_compile_order -fileset sources_1

add_files -norecurse {{C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/gpio/rvsteel_gpio.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/spi/rvsteel_spi.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/bus/rvsteel_bus.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mcu/rvsteel_mcu.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mtimer/rvsteel_mtimer.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/core/rvsteel_core.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/ram/rvsteel_ram.v} {C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/uart/rvsteel_uart.v}}

WARNING: [filemgmt 56-12] File 'C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/hardware/mcu/rvsteel_mcu.v' cannot be added to the project because it already exists in the project, skipping this file

update_compile_order -fileset sources_1

launch_runs synth_1 -jobs 8

[Fri Oct 18 10:06:39 2024] Launched synth_1...

Run output will be captured here: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/synth_1/runme.log

open_run synth_1 -name synth_1

Design is defaulting to impl run constrset: constrs_1

Design is defaulting to synth run part: xc7a100ticsg324-1L

INFO: [Netlist 29-17] Analyzing 499 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Device 21-403] Loading part xc7a100ticsg324-1L

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

Finished Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1130.594 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

open_run: Time (s): cpu = 00:00:05 ; elapsed = 00:00:08 . Memory (MB): peak = 1317.855 ; gain = 479.656

report_power -name {power_1}

Command: report_power -name power_1

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

1 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

report_power completed successfully

launch_runs impl_1 -jobs 8

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 1858.746 ; gain = 0.000

INFO: [Timing 38-480] Writing timing data to binary archive.

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.045 . Memory (MB): peak = 1858.746 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1863.742 ; gain = 0.000

[Fri Oct 18 10:23:47 2024] Launched impl_1...

Run output will be captured here: C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_100t/hello_world_arty_a7_100t.runs/impl_1/runme.log

close_design

open_run impl_1

INFO: [Netlist 29-17] Analyzing 499 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Timing 38-478] Restoring timing data from binary archive.

INFO: [Timing 38-479] Binary timing data restore complete.

INFO: [Project 1-856] Restoring constraints from binary archive.

INFO: [Project 1-853] Binary constraint restore complete.

Reading XDEF placement.

Reading placer database...

Reading XDEF routing.

Read XDEF File: Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.286 . Memory (MB): peak = 1879.430 ; gain = 0.000

Restored from archive | CPU: 1.000000 secs | Memory: 0.000000 MB |

Finished XDEF File Restore: Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.286 . Memory (MB): peak = 1879.430 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1879.430 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

open_run synth_1 -name synth_1

Design is defaulting to impl run constrset: constrs_1

Design is defaulting to synth run part: xc7a100ticsg324-1L

INFO: [Netlist 29-17] Analyzing 499 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2018.3

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

Finished Parsing XDC File [C:/Users/sabolu samuel jason/riscv-gnu-toolchain/riscv-steel/examples/hello_world/boards/arty_a7/hello_world_arty_a7_constraints.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 2179.188 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

report_timing_summary -delay_type min_max -report_unconstrained -check_timing_verbose -max_paths 10 -input_pins -routable_nets -name timing_1

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

report_timing -max_paths 1 -nworst 1 -delay_type max -sort_by slack

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

INFO: [Timing 38-78] ReportTimingParams: -max_paths 1 -nworst 1 -delay_type max -sort_by slack.

| Tool Version : Vivado v.2018.3 (win64) Build 2405991 Thu Dec 6 23:38:27 MST 2018

| Date   : Fri Oct 18 10:31:17 2024

| Host   : Samuel running 64-bit major release (build 9200)

| Command   : report_timing -max_paths 1 -nworst 1 -delay_type max -sort_by slack

| Design   : hello_world_arty_a7

| Device   : 7a100ti-csg324

| Speed File   : -1L PRODUCTION 1.23 2018-06-13

Timing Report

Slack (MET) : 2.584ns (required time - arrival time)

  Source: rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_0/CLKBWRCLK

  (rising edge-triggered cell RAMB36E1 clocked by clkdiv2 {rise@0.000ns fall@10.000ns period=20.000ns})

  Destination: rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save_reg[0]/R

  (rising edge-triggered cell FDRE clocked by clkdiv2 {rise@0.000ns fall@10.000ns period=20.000ns})

  Path Group: clkdiv2

  Path Type: Setup (Max at Slow Process Corner)

  Requirement: 20.000ns (clkdiv2 rise@20.000ns - clkdiv2 rise@0.000ns)

  Data Path Delay: 16.679ns (logic 6.708ns (40.219%) route 9.971ns (59.781%))

  Logic Levels: 24 (CARRY4=7 LUT2=2 LUT3=2 LUT4=2 LUT5=5 LUT6=6)

  Clock Path Skew: -0.145ns (DCD - SCD + CPR)

    Destination Clock Delay (DCD): 4.523ns = (24.523 - 20.000)

    Source Clock Delay (SCD): 5.101ns

    Clock Pessimism Removal (CPR): 0.433ns

Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

(clock clkdiv2 rise edge) 0.000 0.000 r

E3 0.000 0.000 r clock (IN)

net (fo=0) 0.000 0.000 clock

E3 IBUF (Prop_ibuf_I_O) 1.482 1.482 r clock_IBUF_inst/O

net (fo=1, unplaced) 0.803 2.285 clock_IBUF

BUFG (Prop_bufg_I_O) 0.096 2.381 r clock_IBUF_BUFG_inst/O

net (fo=1, unplaced) 0.584 2.965 clock_IBUF_BUFG

FDRE (Prop_fdre_C_Q) 0.478 3.443 r clock_50mhz_reg/Q

net (fo=2, unplaced) 0.803 4.246 clock_50mhz

BUFG (Prop_bufg_I_O) 0.271 4.517 r clock_50mhz_BUFG_inst/O

net (fo=1771, unplaced) 0.584 5.101 rvsteel_mcu_instance/rvsteel_ram_instance/clock_50mhz_BUFG

RAMB36E1 r rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_0/CLKBWRCLK

RAMB36E1 (Prop_ramb36e1_CLKBWRCLK_DOBDO[1]) 2.454 7.555 f rvsteel_mcu_instance/rvsteel_ram_instance/ram_reg_0/DOBDO[1]

net (fo=1, unplaced) 0.803 8.357 rvsteel_mcu_instance/rvsteel_bus_instance/device_read_data[1]

LUT6 (Prop_lut6_I1_O) 0.124 8.481 f rvsteel_mcu_instance/rvsteel_bus_instance/prev_instruction[1]_i_2/O

net (fo=4, unplaced) 0.756 9.237 rvsteel_mcu_instance/rvsteel_core_instance/manager_read_data[1]

LUT6 (Prop_lut6_I1_O) 0.124 9.361 r rvsteel_mcu_instance/rvsteel_core_instance/integer_file[30][31]_i_21/O

net (fo=8, unplaced) 0.487 9.848 rvsteel_mcu_instance/rvsteel_core_instance/integer_file[30][31]_i_21_n_0

LUT5 (Prop_lut5_I4_O) 0.124 9.972 f rvsteel_mcu_instance/rvsteel_core_instance/current_state[3]_i_23/O

net (fo=4, unplaced) 0.473 10.445 rvsteel_mcu_instance/rvsteel_core_instance/current_state[3]_i_23_n_0

LUT5 (Prop_lut5_I2_O) 0.124 10.569 f rvsteel_mcu_instance/rvsteel_core_instance/current_state[3]_i_12/O

net (fo=9, unplaced) 0.490 11.059 rvsteel_mcu_instance/rvsteel_core_instance/system_type

LUT3 (Prop_lut3_I0_O) 0.124 11.183 f rvsteel_mcu_instance/rvsteel_core_instance/csr_mie_msie_i_10/O

net (fo=5, unplaced) 0.477 11.660 rvsteel_mcu_instance/rvsteel_core_instance/csrxxx

LUT6 (Prop_lut6_I2_O) 0.124 11.784 r rvsteel_mcu_instance/rvsteel_core_instance/csr_mie_msie_i_11/O

net (fo=33, unplaced) 0.521 12.305 rvsteel_mcu_instance/rvsteel_core_instance/immediate_type[0]

LUT4 (Prop_lut4_I2_O) 0.124 12.429 r rvsteel_mcu_instance/rvsteel_core_instance/csr_mscratch[0]_i_5/O

net (fo=1, unplaced) 0.449 12.878 rvsteel_mcu_instance/rvsteel_core_instance/csr_mscratch[0]_i_5_n_0

LUT5 (Prop_lut5_I0_O) 0.124 13.002 r rvsteel_mcu_instance/rvsteel_core_instance/csr_mscratch[0]_i_2/O

net (fo=5, unplaced) 0.477 13.479 rvsteel_mcu_instance/rvsteel_core_instance/immediate[0]

LUT5 (Prop_lut5_I3_O) 0.124 13.603 r rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval[3]_i_6/O

net (fo=1, unplaced) 0.000 13.603 rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval[3]_i_6_n_0

CARRY4 (Prop_carry4_S[0]_CO[3])

0.513 14.116 r rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[3]_i_2/CO[3]

net (fo=1, unplaced) 0.000 14.116 rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[3]_i_2_n_0

CARRY4 (Prop_carry4_CI_CO[3])

0.117 14.233 r rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[7]_i_2/CO[3]

net (fo=1, unplaced) 0.000 14.233 rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[7]_i_2_n_0

CARRY4 (Prop_carry4_CI_CO[3])

0.117 14.350 r rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[11]_i_2/CO[3]

net (fo=1, unplaced) 0.000 14.350 rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[11]_i_2_n_0

CARRY4 (Prop_carry4_CI_O[1])

0.337 14.687 f
rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[15]_i_2/O[1]

net (fo=4, unplaced) 0.635 15.322
rvsteel_mcu_instance/rvsteel_core_instance/csr_mtval_reg[15]_i_2_n_6

LUT5 (Prop_lut5_I0_O) 0.306 15.628 f
rvsteel_mcu_instance/rvsteel_core_instance/program_counter[13]_i_2/O

net (fo=1, unplaced) 0.449 16.077
rvsteel_mcu_instance/rvsteel_core_instance/program_counter[13]_i_2_n_0

LUT6 (Prop_lut6_I0_O) 0.124 16.201 f
rvsteel_mcu_instance/rvsteel_core_instance/program_counter[13]_i_1/O

net (fo=2, unplaced) 0.460 16.661
rvsteel_mcu_instance/rvsteel_core_instance/next_program_counter[13]

LUT4 (Prop_lut4_I0_O) 0.124 16.785 f
rvsteel_mcu_instance/rvsteel_core_instance/prev_instruction_address[13]_i_1/O

net (fo=2, unplaced) 0.460 17.245
rvsteel_mcu_instance/rvsteel_core_instance/prev_instruction_address[13]_i_1_n_0

LUT6 (Prop_lut6_I0_O) 0.124 17.369 f
rvsteel_mcu_instance/rvsteel_core_instance/prev_rw_address[13]_i_1/O

net (fo=2, unplaced) 0.430 17.799
rvsteel_mcu_instance/rvsteel_core_instance/prev_rw_address[13]_i_1_n_0

LUT2 (Prop_lut2_I0_O) 0.124 17.923 f
rvsteel_mcu_instance/rvsteel_core_instance/ram_reg_0_i_6/O

net (fo=6, unplaced) 0.481 18.404
rvsteel_mcu_instance/rvsteel_core_instance/ram_reg_0_i_6_n_0

LUT2 (Prop_lut2_I0_O) 0.124 18.528 r
rvsteel_mcu_instance/rvsteel_core_instance/i__carry_i_1__2/O

net (fo=1, unplaced) 0.000 18.528
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry__0_0[3]

CARRY4 (Prop_carry4_S[3]_CO[3])

0.376 18.904 r
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry/CO[3]

net (fo=1, unplaced) 0.000 18.904
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry_n_0

CARRY4 (Prop_carry4_CI_CO[3])

0.117 19.021 r
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry__0/CO[3]

net (fo=1, unplaced) 0.000 19.021
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry__0_n_0

CARRY4 (Prop_carry4_CI_CO[1])

0.179 19.200 f
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save0_inferred__2/i__carry__1/CO[1]

net (fo=9, unplaced) 1.038 20.238 rvsteel_mcu_instance/rvsteel_bus_instance/device_sel[3]

LUT6 (Prop_lut6_I0_O) 0.332 20.570 r
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save[4]_i_2/O

net (fo=1, unplaced) 0.449 21.019
rvsteel_mcu_instance/rvsteel_core_instance/device_sel_save_reg[4]

LUT3 (Prop_lut3_I2_O) 0.124 21.143 r
rvsteel_mcu_instance/rvsteel_core_instance/device_sel_save[4]_i_1/O

net (fo=5, unplaced) 0.636 21.779 rvsteel_mcu_instance/rvsteel_bus_instance/SR[0]

FDRE r rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save_reg[0]/R

(clock clkdiv2 rise edge) 20.000 20.000 r

E3 0.000 20.000 r clock (IN)

net (fo=0) 0.000 20.000 clock

E3 IBUF (Prop_ibuf_I_O) 1.411 21.411 r clock_IBUF_inst/O

net (fo=1, unplaced) 0.763 22.174 clock_IBUF

BUFG (Prop_bufg_I_O) 0.091 22.265 r clock_IBUF_BUFG_inst/O

net (fo=1, unplaced) 0.439 22.704 clock_IBUF_BUFG

FDRE (Prop_fdre_C_Q) 0.385 23.089 r clock_50mhz_reg/Q

net (fo=2, unplaced) 0.763 23.852 clock_50mhz

BUFG (Prop_bufg_I_O) 0.232 24.084 r clock_50mhz_BUFG_inst/O

net (fo=1771, unplaced) 0.439 24.523
rvsteel_mcu_instance/rvsteel_bus_instance/clock_50mhz_BUFG

FDRE r rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save_reg[0]/C

clock pessimism 0.433 24.956

clock uncertainty -0.035 24.920

FDRE (Setup_fdre_C_R) -0.557 24.363
rvsteel_mcu_instance/rvsteel_bus_instance/device_sel_save_reg[0]

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required time 24.363

arrival time -21.779

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slack 2.584