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No. TFC/60.2/Misc

Dated: 10.09.2020

TO WHOMSOEVER IT MAY CONCERN

This is to certify that Mr. Ramesht Shukla and Ms. Aditi Singhal, B.Tech final year scholar in Electronics Engineering from Bharati Vidyapeeth College of Engineering, Pune (Deemed to be University), have successfully completed their Engineering Project "Train Delay Analysis and Prediction Methodology for Indian Railways" under Traffic Directorate of Research Designs & Standards Organization, Manak Nagar, Lucknow-226011, India.

We wish them the best of luck.


10.09.2020
(K.K. Chowdhury)
For Director General (Traffic)