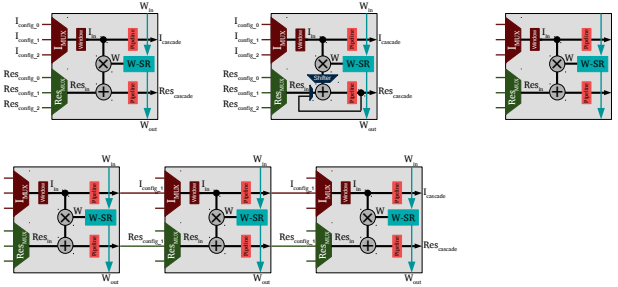
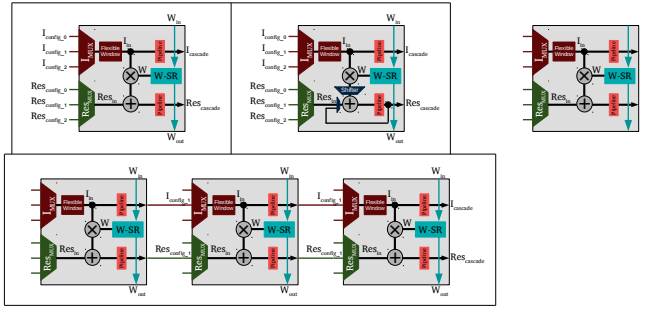
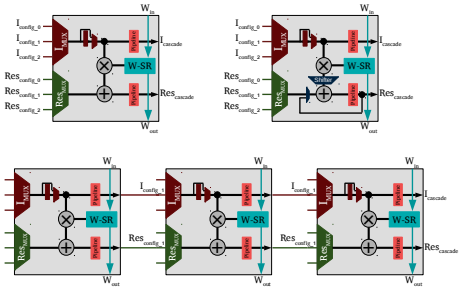


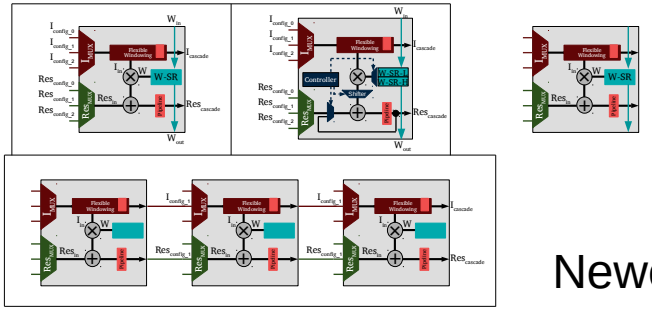
New



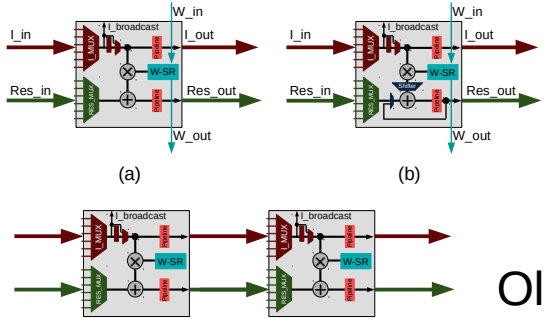
Newer



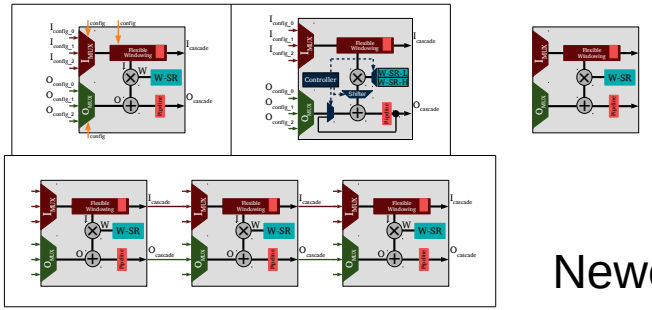
Old



Newest



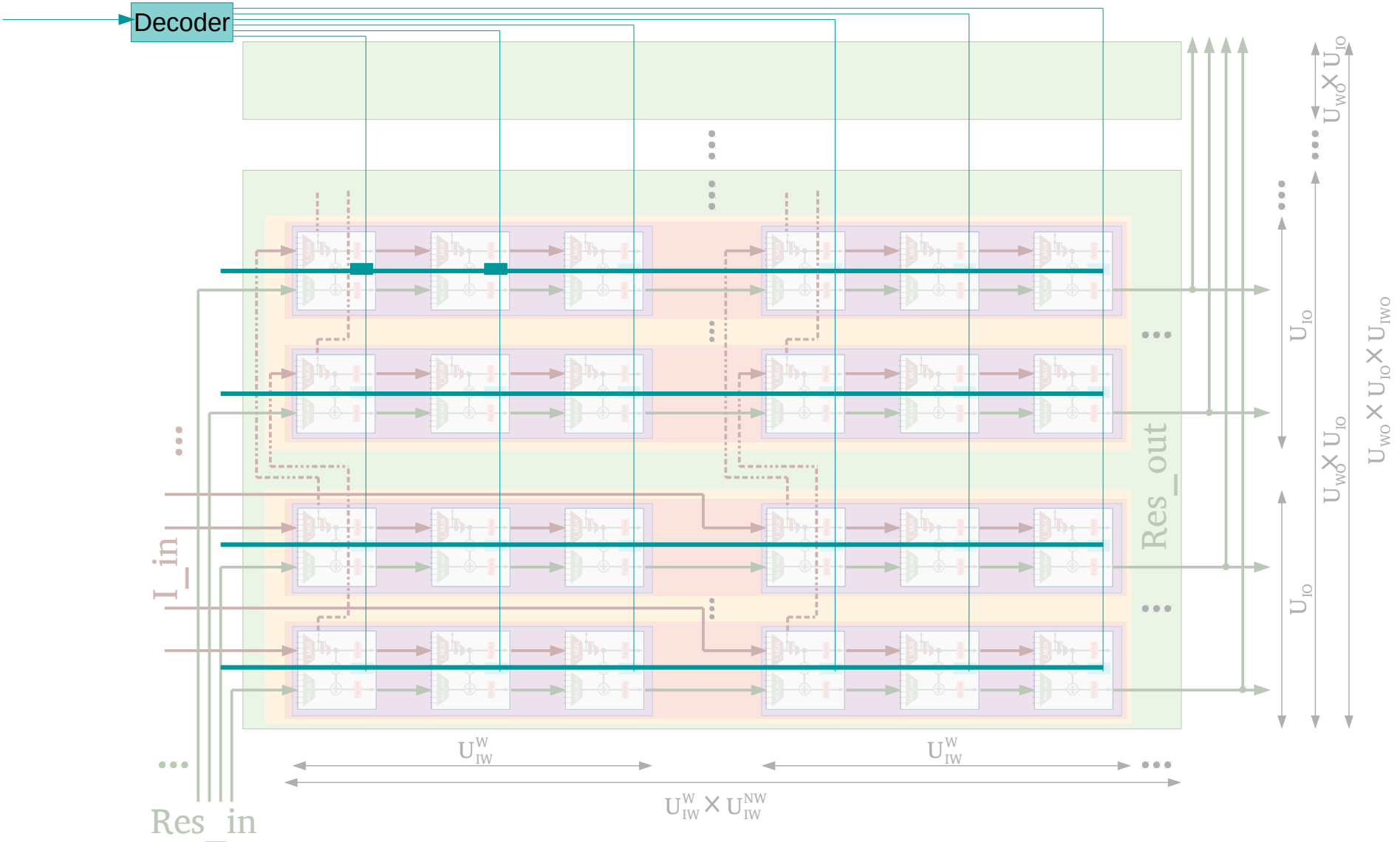
Older



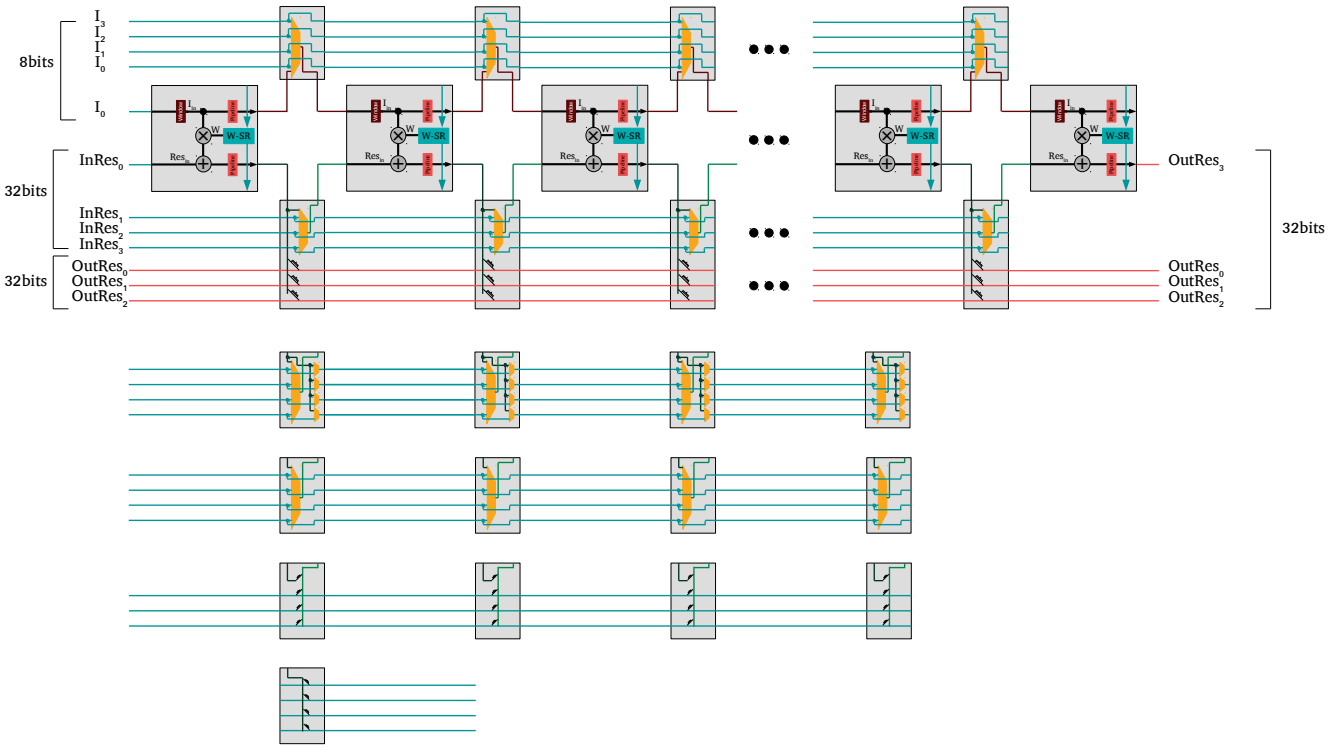
Newest2

I_in
Res_in
Res_out
U_{IW}^{W}
U_{IW}^{W}
$U_{IW}^{W} \times U_{IW}^{NW}$
U_{IO}
U_{IO}
$U_{WO} \times U_{IO}$
$U_{WO} \times U_{IO} \times U_{IWO}$
$U_{WO} \times U_{IO}$
L_MUX
RES_MUX
W-RF
Buffer

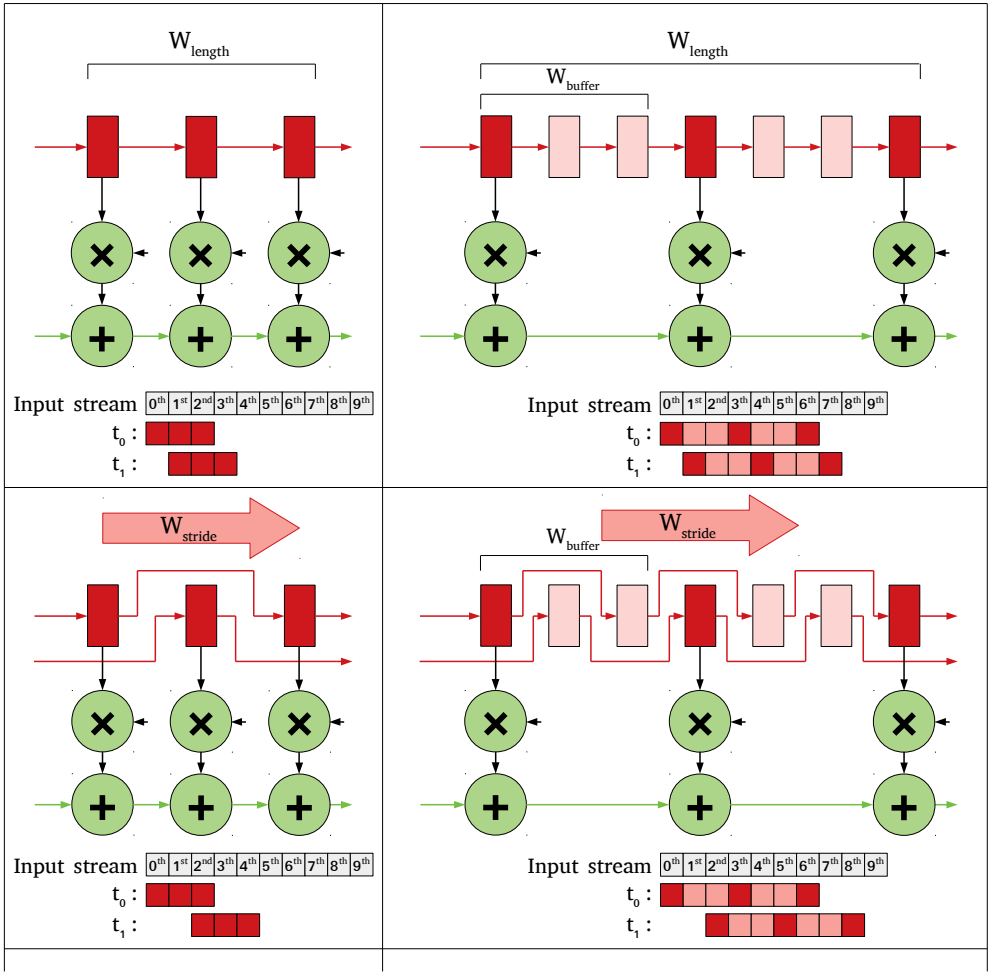
I_{in}
O_{in}
O_{out}
U_{IW}^{W}
U_{IW}^{W}
$U_{IW}^{W} \times U_{IW}^{NW}$
U_{IO}
U_{IO}
$U_{WO} \times U_{IO}$
$U_{WO} \times U_{IO}$
$U_{WO} \times U_{IO} \times U_{IWO}$


Decoder
I_in
Res_in
Res_out
U_{IW}^{W}
U_{IW}^{W}
$U_{IW}^{W} \times U_{IW}^{NW}$
U_{IO}
$U_{WO} \times U_{IO}$
U_{IO}
$U_{WO} \times U_{IO}$
$U_{WO} \times U_{IO} \times U_{IWO}$

1D Super Flex arch.



Windowed param: fx (filter

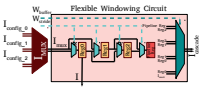


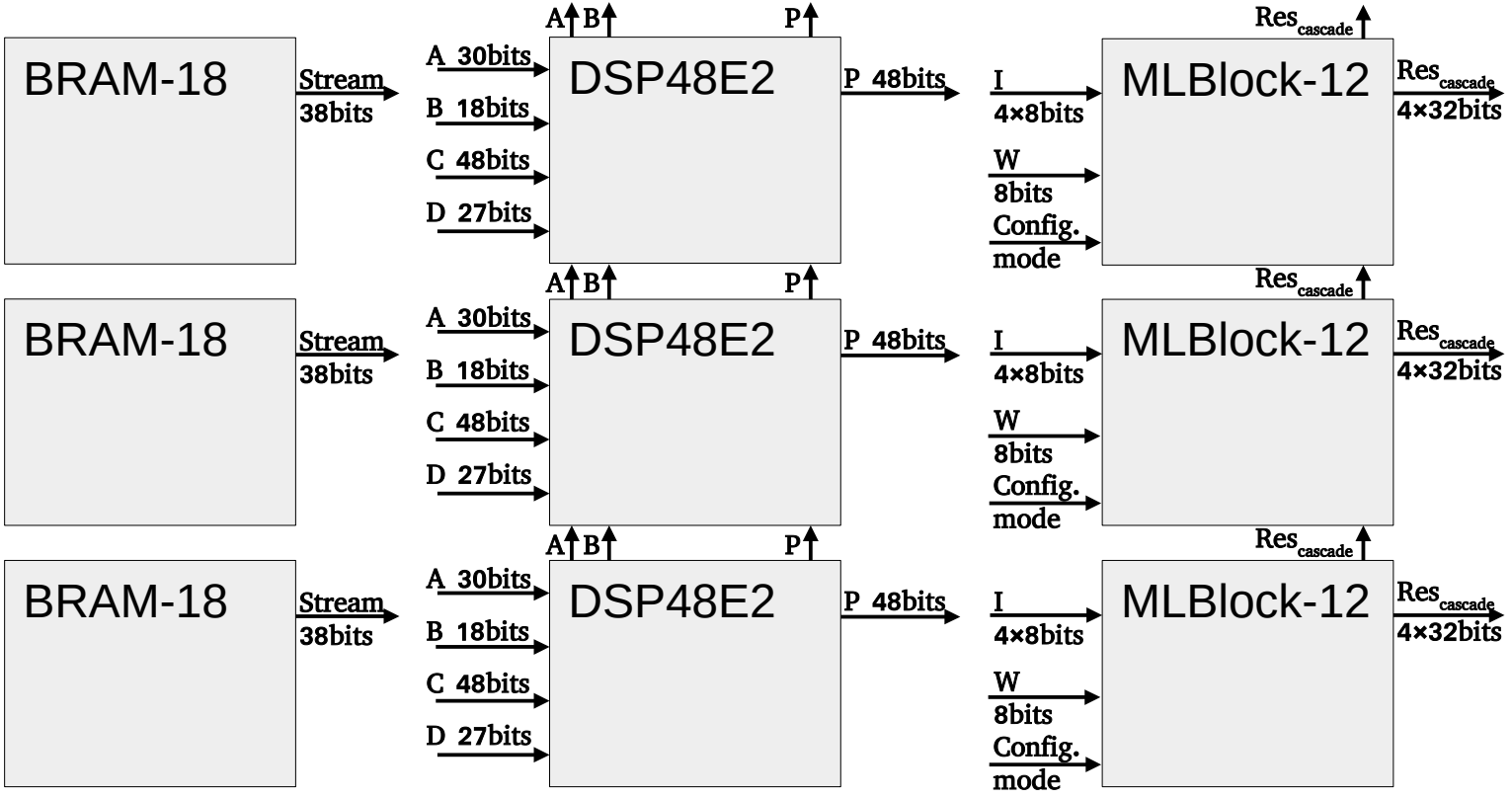
Iteration step may affects:
1- window size
2- speed of windowing
3- sample rate (dilated convolutions)

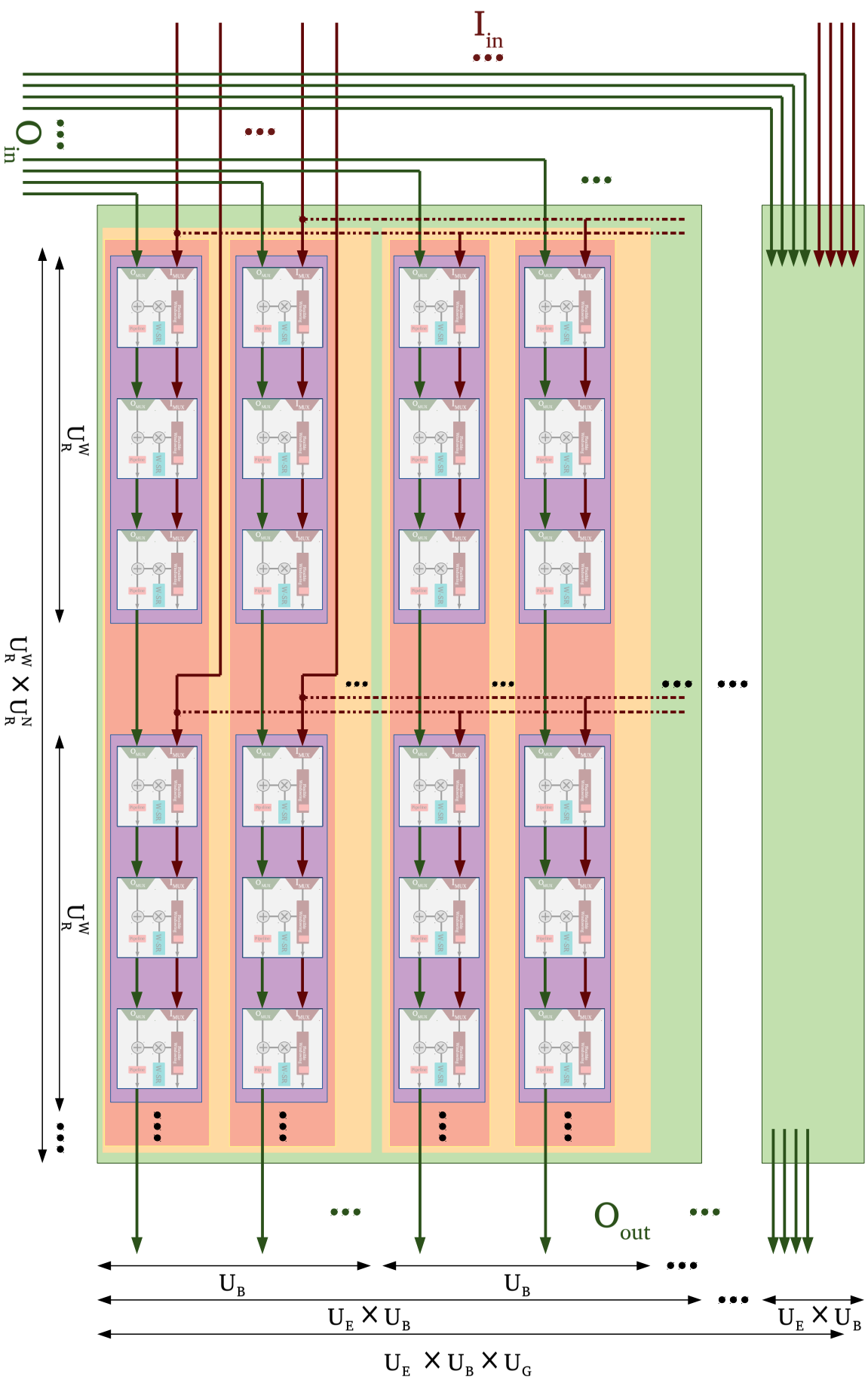
W_{stride}

Accompany of Windowed param: x (input param)

Both: X & fx


Flexible Windowing Circuit
W_{config}
W_{config}
I_{config_0}
I_{config_1}
I_{config_2}
MUX 3:1
I
I
I
Pipeline Regs
Pipeline Regs
Pipeline Regs
Pipeline Regs
Pipeline Regs
Pipeline Regs
MUX
W_{out}


BRAM-18
Stream
38bits
A
B
P
A 30bits
B 18bits
C 48bits
D 27bits
DSP48E2
P 48bits
I
4×8bits
W
8bits
Config.
mode
Res cascade
MLBlock-12
Res cascade
4×32bits
BRAM-18
Stream
38bits
A
B
P
A 30bits
B 18bits
C 48bits
D 27bits
DSP48E2
P 48bits
I
4×8bits
W
8bits
Config.
mode
Res cascade
MLBlock-12
Res cascade
4×32bits
BRAM-18
Stream
38bits
A
B
P
A 30bits
B 18bits
C 48bits
D 27bits
DSP48E2
P 48bits
I
4×8bits
W
8bits
Config.
mode
Res cascade
MLBlock-12
Res cascade
4×32bits


I_{in}
O_{in}
U_R^W
$U_R^W \times U_R^N$
U_R^W
O_{out}
U_B
U_B
$U_E \times U_B$
$U_E \times U_B$
$U_E \times U_B \times U_G$