

Design
constraints

```
graph LR; A([Design constraints]) --> C[Pick all configurations which are necessary to delivering the highest utilization]; B([Benchmarks]) --> C; C --> D[Generate Verilog model];
```

The diagram is a flowchart with three main components. At the top center is a red oval containing the text 'Design constraints'. To the left is another red oval containing the text 'Benchmarks'. Both of these ovals have black arrows pointing down to a central green rectangular box. This green box contains the text 'Pick all configurations which are necessary to delivering the highest utilization'. A black arrow points from the right side of this green box to an orange rectangular box on the right, which contains the text 'Generate Verilog model'.

Benchmarks

Pick all configurations which are
necessary to delivering the highest utilization

Generate
Verilog model