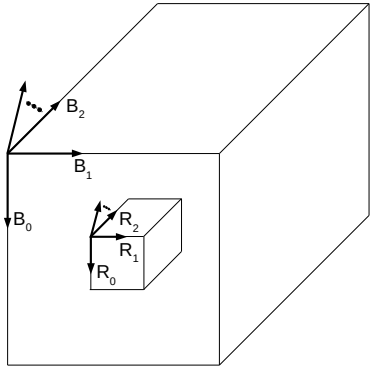
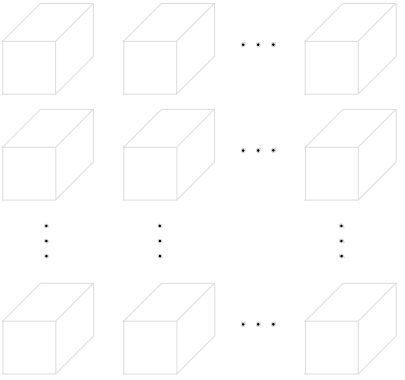
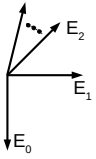
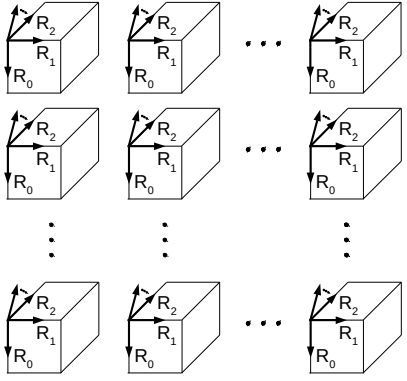
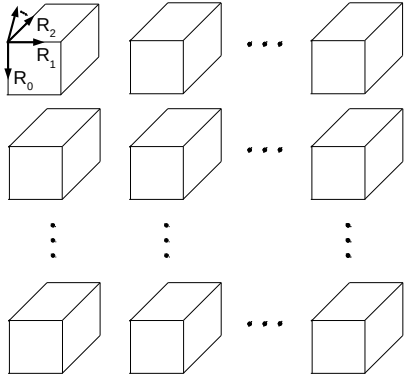
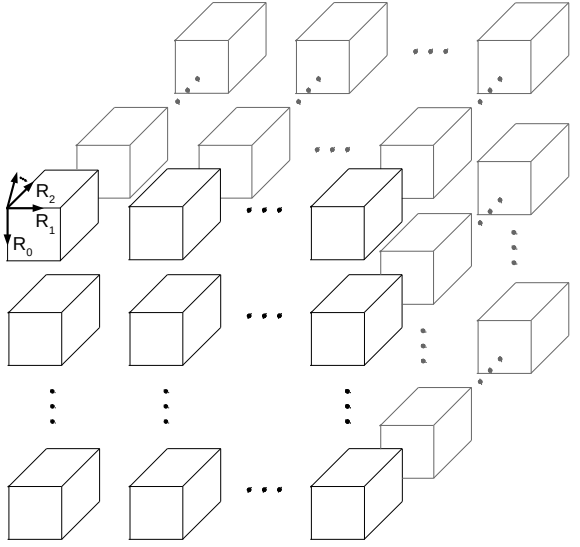

B2
B1
B0
R2
R1
R0

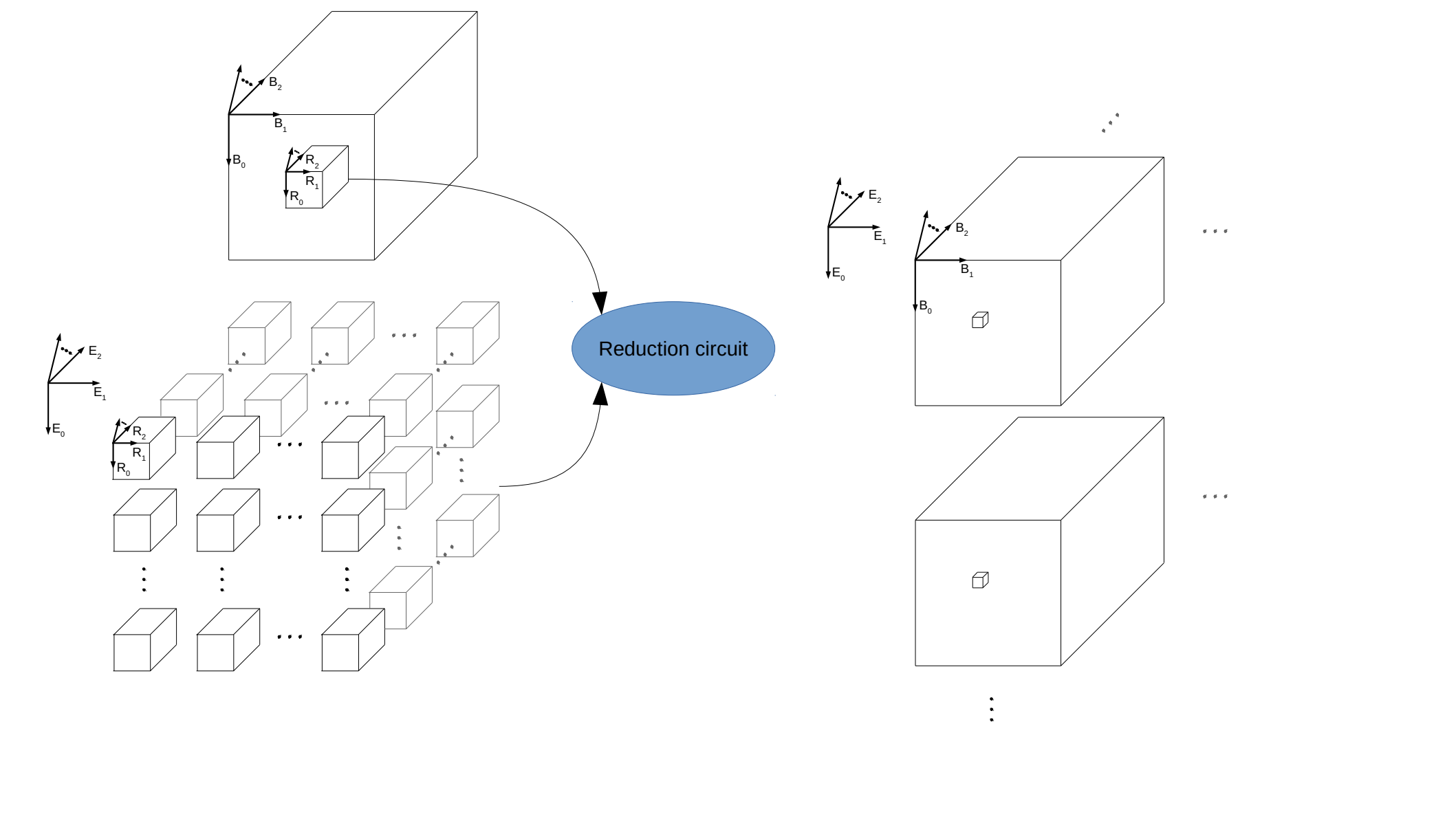


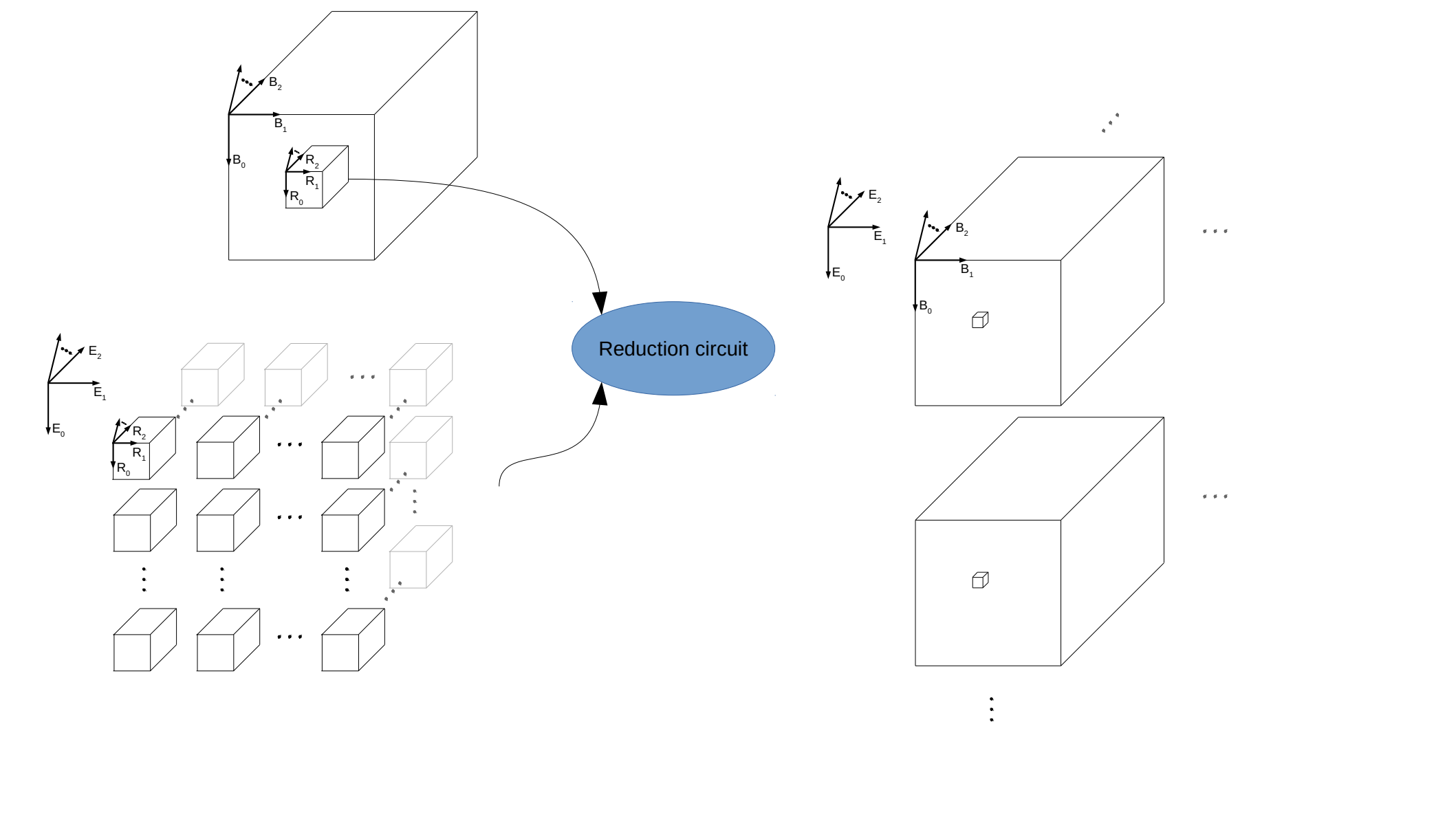

E2
E1
E0

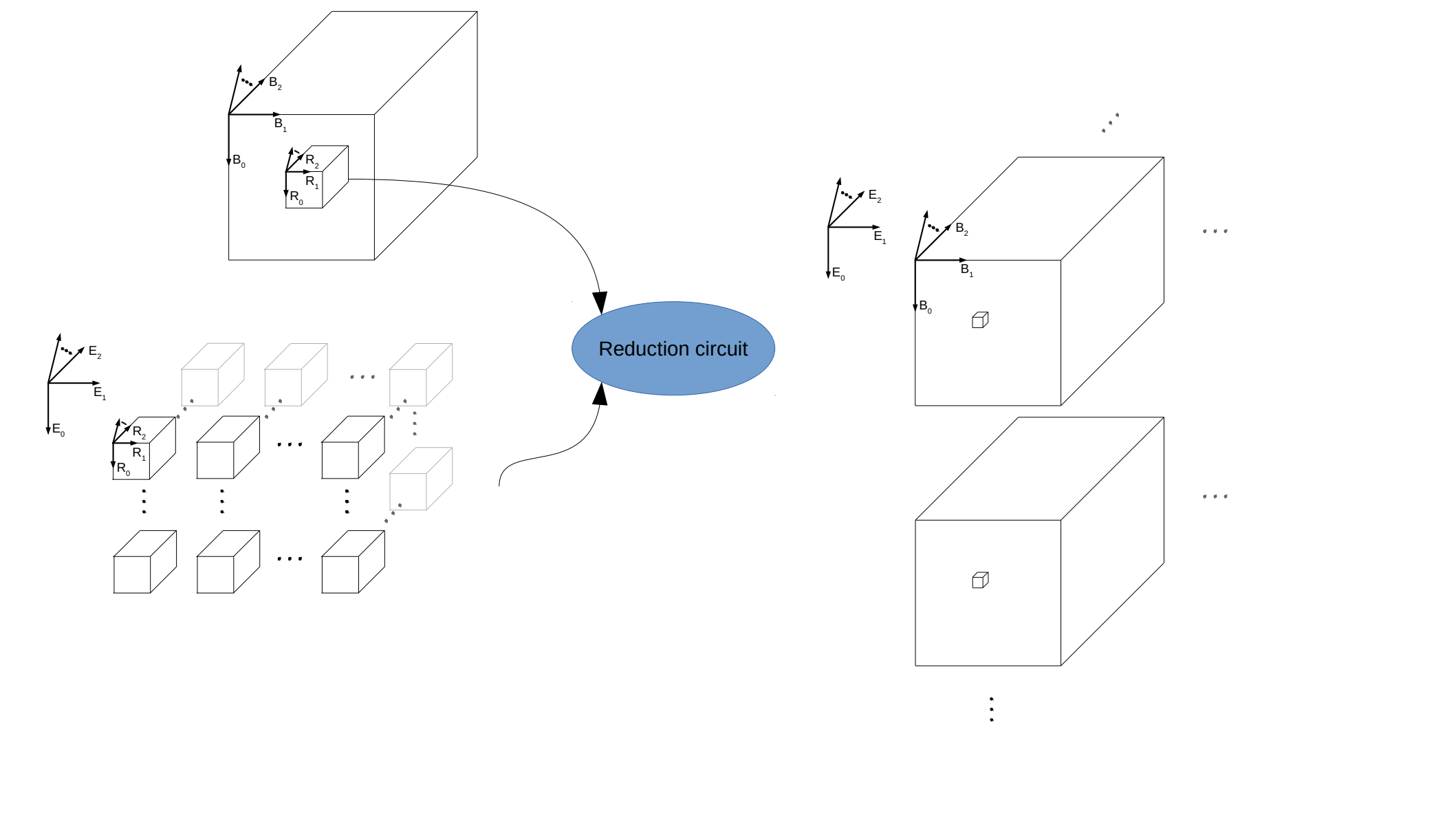

R2
R1
R0

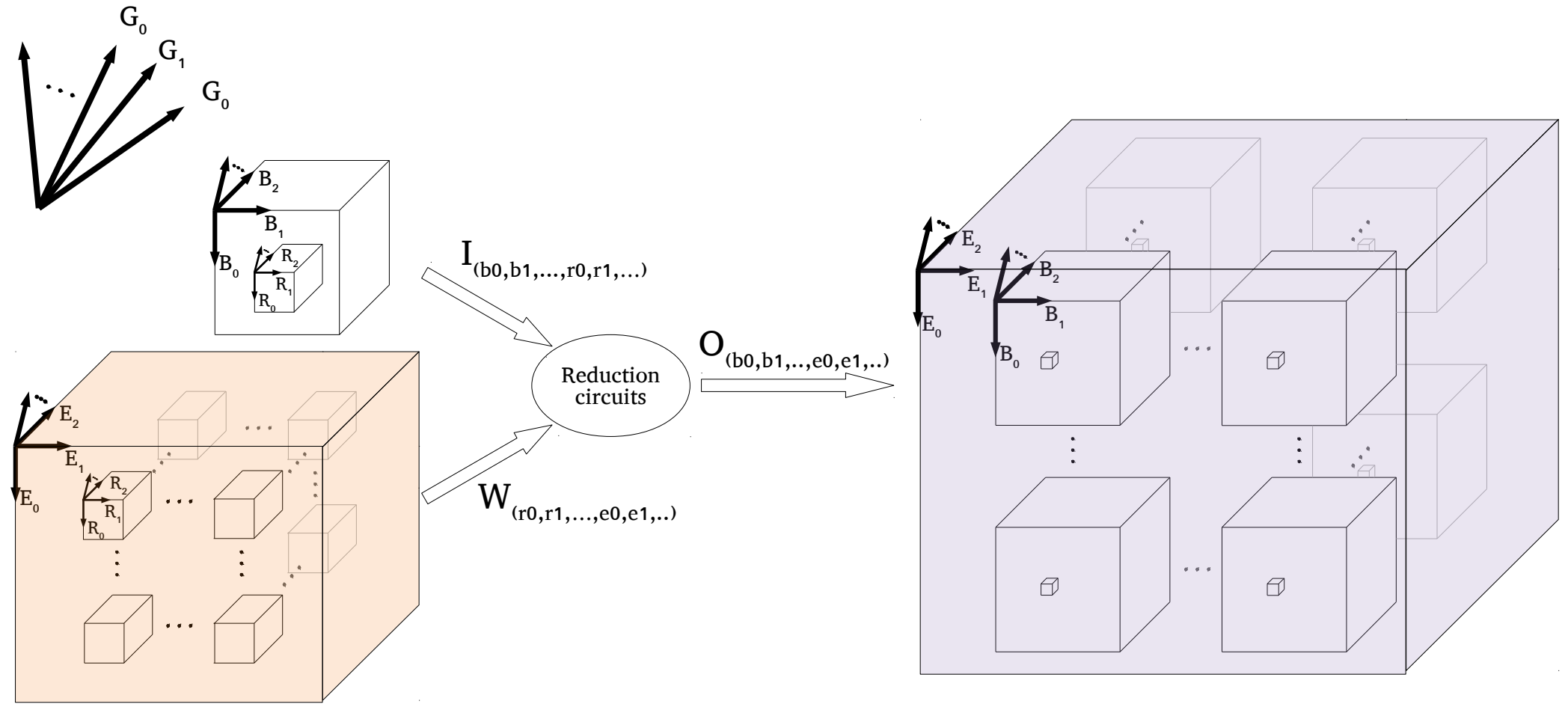

R2
R1
R0

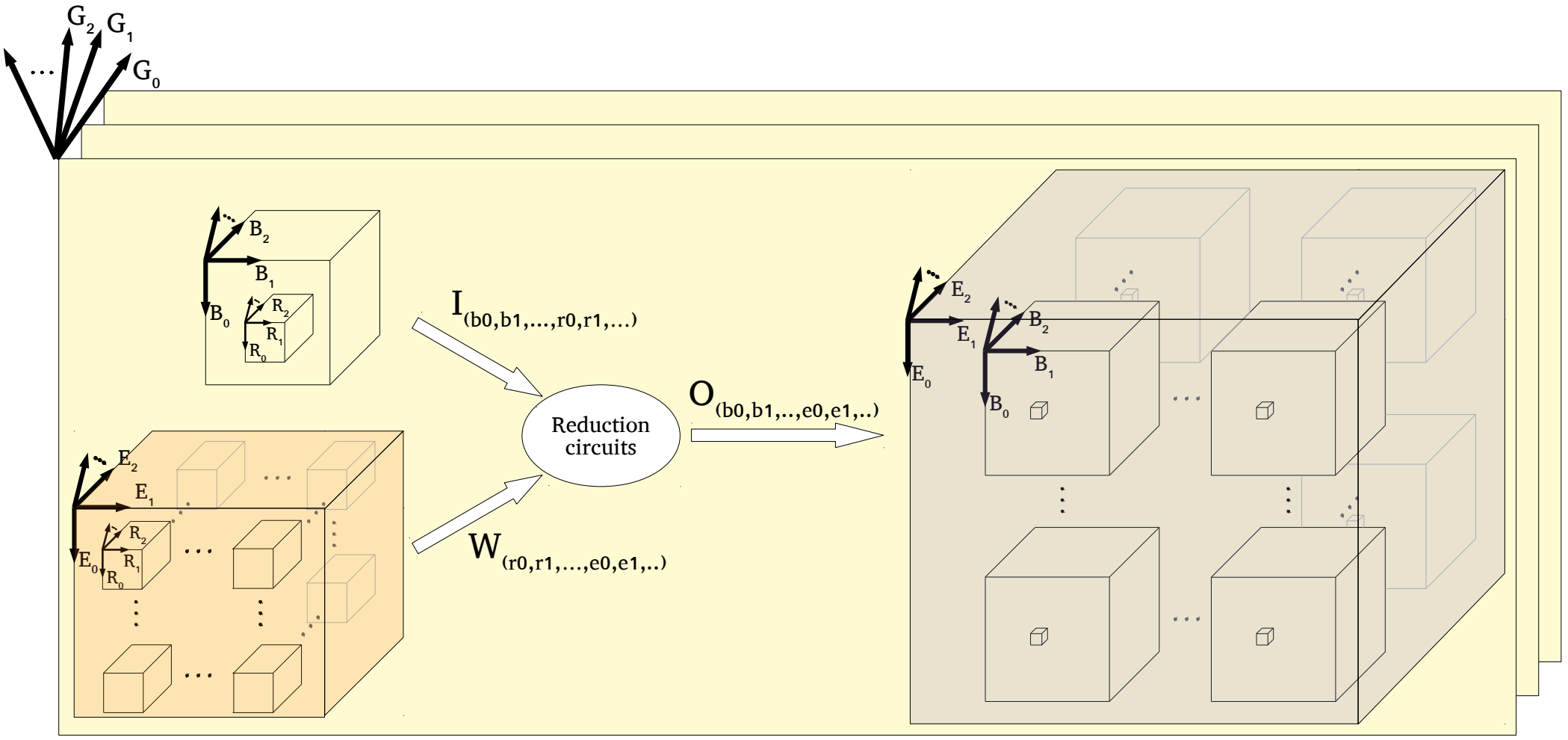

R2
R1
R0

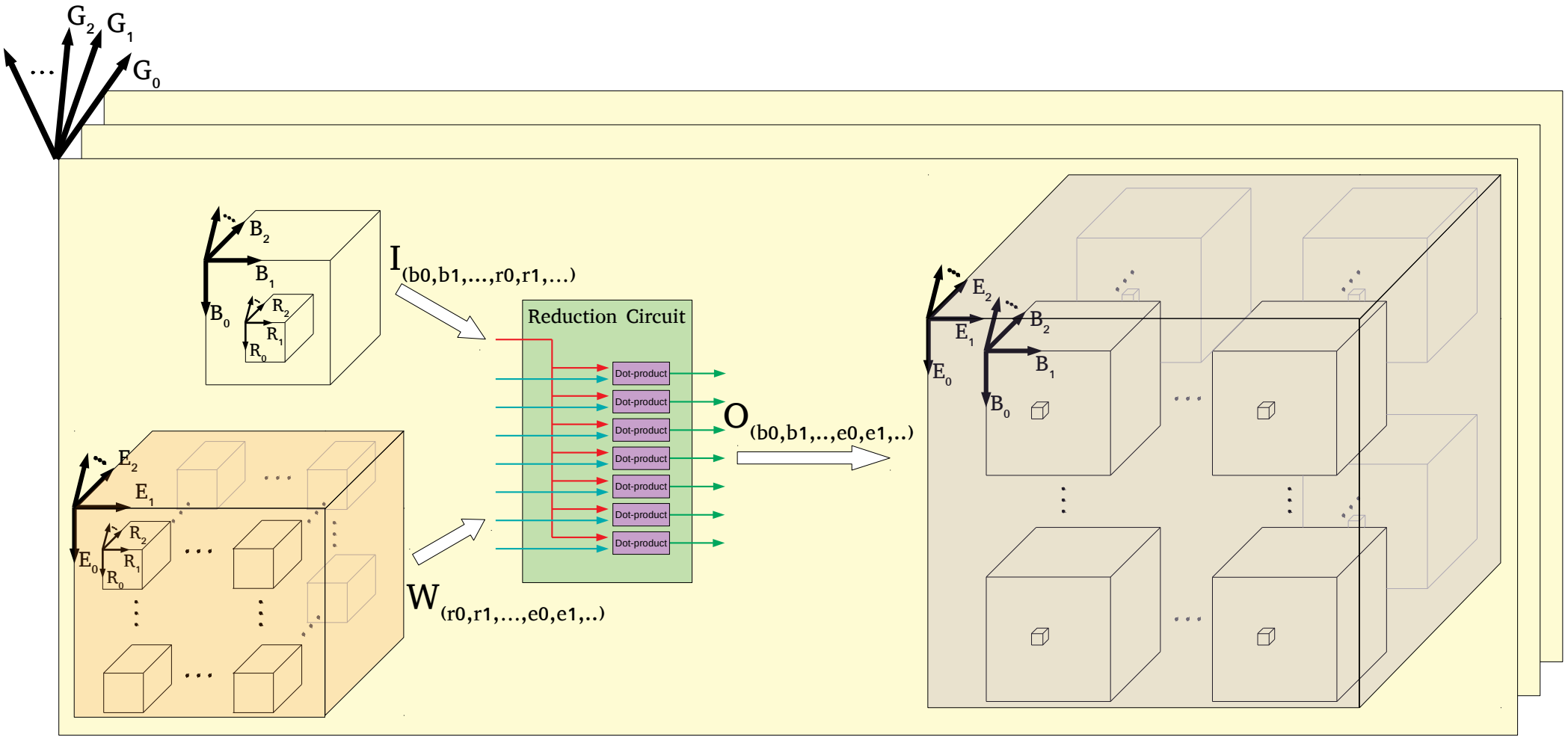

B2
B1
B0
R2
R1
R0
E2
E1
E0
Reduction circuit

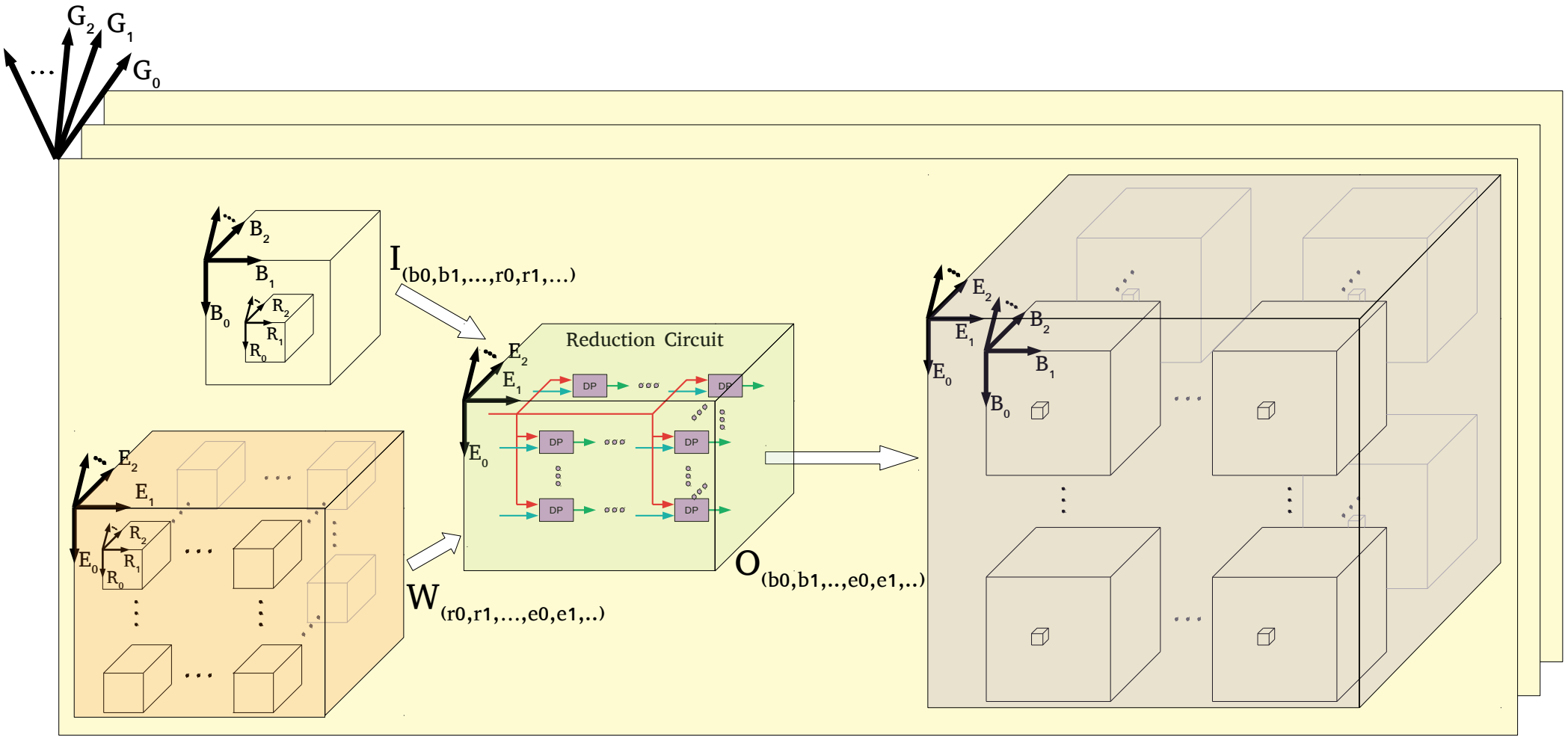

B2
B1
B0
R2
R1
R0
E2
E1
E0
Reduction circuit

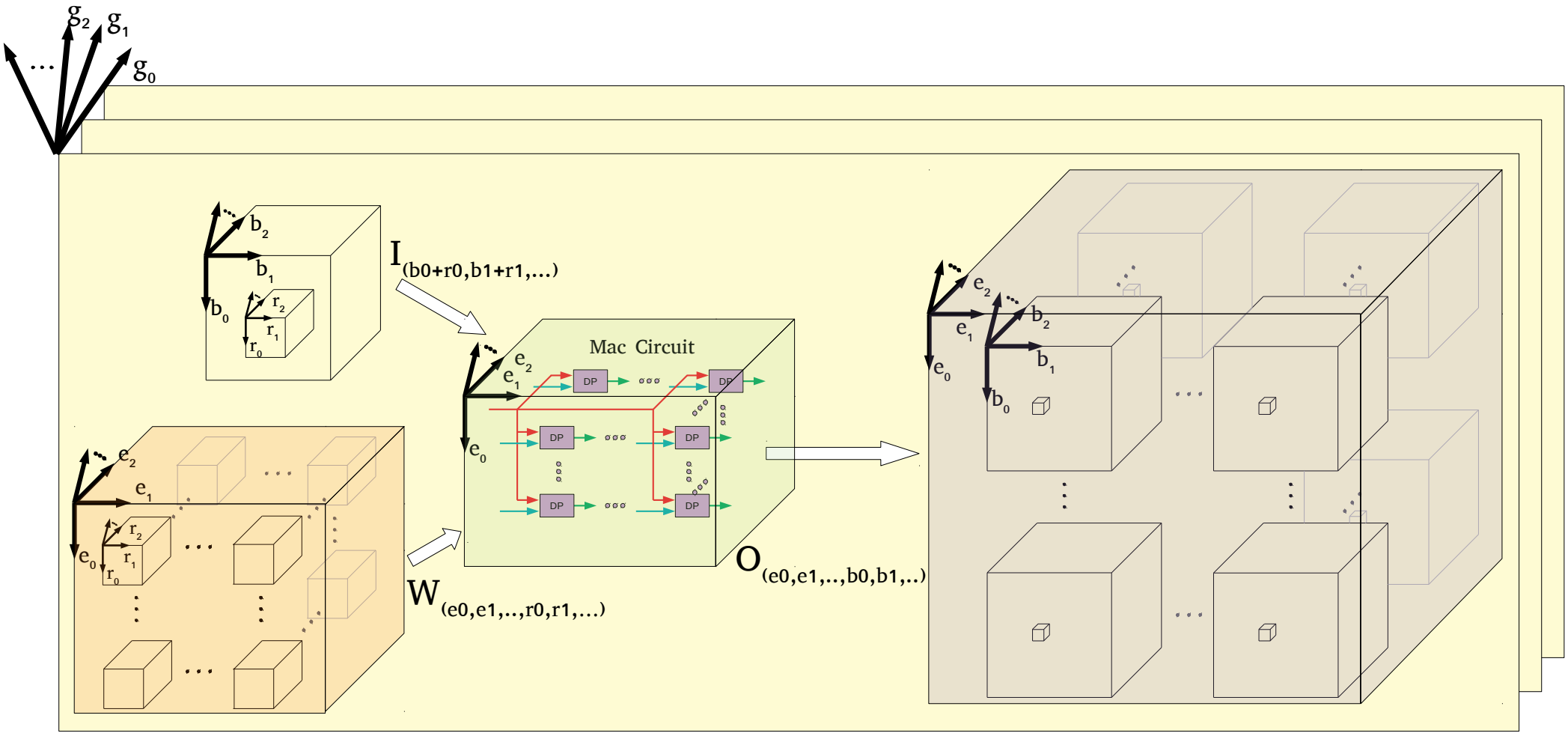

B2
B1
B0
R2
R1
R0
E2
E1
E0
Reduction circuit

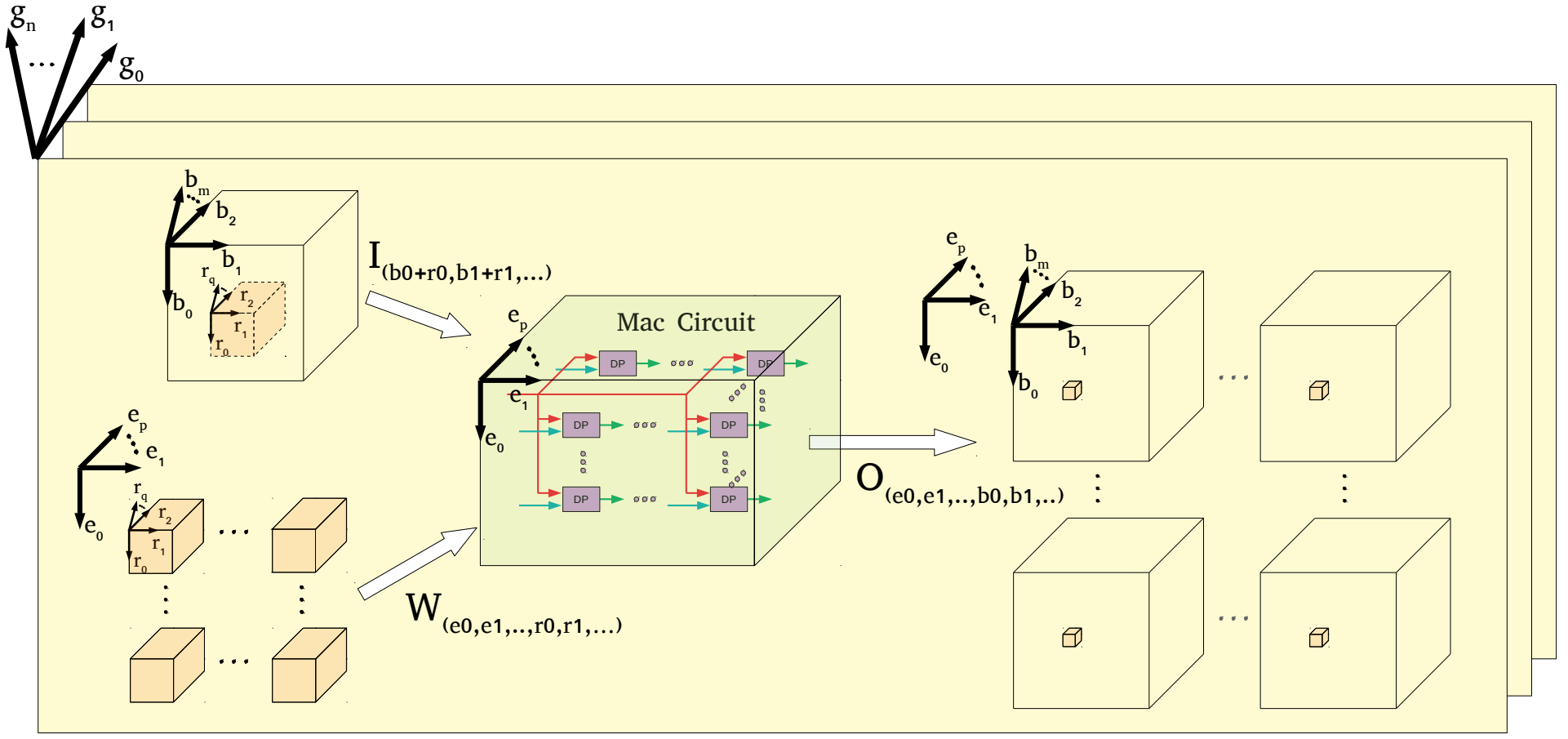

G0
G1
G0
B2
B1
B0
R2
R1
R0
I(b0,b1,...,r0,r1,...)
Reduction circuits
W(r0,r1,...,e0,e1,..)
O(b0,b1,..,e0,e1,..)
E2
E1
E0


G2
G1
G0
B2
B1
B0
R2
R1
R0
I(b0,b1,...,r0,r1,...)
Reduction circuits
W(r0,r1,...,e0,e1,..)
O(b0,b1,..,e0,e1,..)
E2
E1
E0


G2
G1
G0
B2
B1
B0
R2
R1
R0
I(b0,b1,...,r0,r1,...)
Reduction Circuit
Dot-product
Dot-product
Dot-product
Dot-product
Dot-product
Dot-product
Dot-product
O(b0,b1,..,e0,e1,..)
E2
E1
E0
R2
R1
R0
W(r0,r1,...,e0,e1,..)
E2
E1
E0
B2
B1
B0


G2
G1
G0
B2
B1
B0
R2
R1
R0
I(b0,b1,...,r0,r1,...)
Reduction Circuit
E2
E1
E0
DP
W(r0,r1,...,e0,e1,..)
O(b0,b1,..,e0,e1,..)


g2
g1
g0
b2
b1
b0
r2
r1
r0
I(b0+r0,b1+r1,...)
Mac Circuit
DP
e2
e1
e0
W(e0,e1,..,r0,r1,...)
O(e0,e1,..,b0,b1,..)


$g_n$
$g_1$
$g_0$
$b_m$
$b_2$
$b_1$
$b_0$
$r_q$
$r_2$
$r_1$
$r_0$
$I_{(b0+r0,b1+r1,...)}$
Mac Circuit
DP
$e_p$
$e_1$
$e_0$
$W_{(e0,e1,..,r0,r1,...)}$
$O_{(e0,e1,..,b0,b1,..)}$