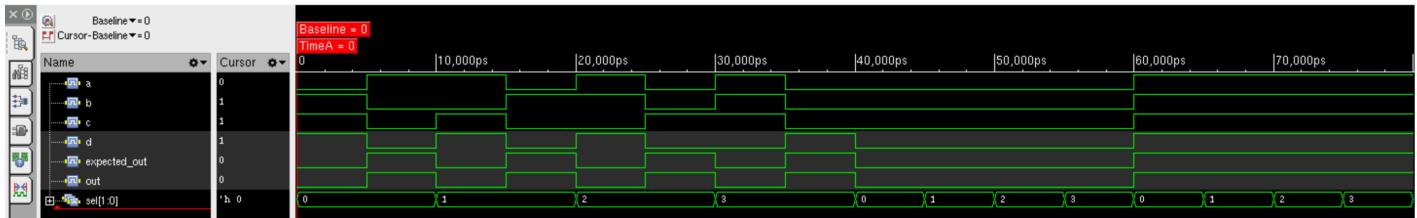


Appendix

Waveform Simulation and Test Cases Console Outputs:

Mux 4 to1



```
xcelium>
xcelium> # Run the simulation for 100 ns
xcelium> run 500 ns

===== Functional Verification of 4-to-1 MUX =====

----- Select input a -----
a=0 b=1 c=1 d=1 sel=00 → Expected out=0 | Obtained out=0
[PASS]

----- Select input a -----
a=1 b=0 c=0 d=0 sel=00 → Expected out=1 | Obtained out=1
[PASS]

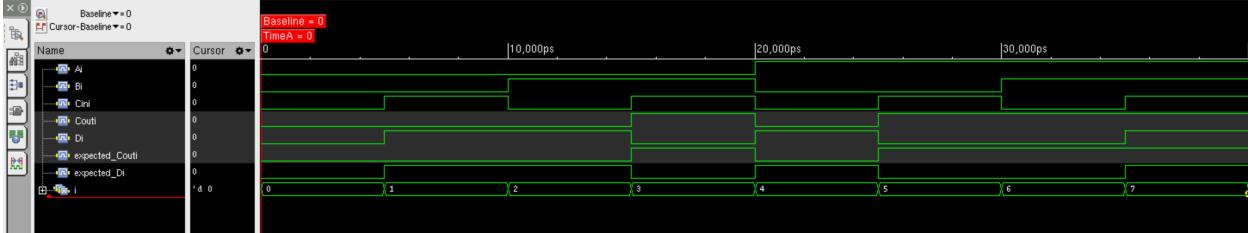
----- Select input b -----
a=1 b=0 c=1 d=1 sel=01 → Expected out=0 | Obtained out=0
[PASS]

----- Select input b -----
a=0 b=1 c=0 d=0 sel=01 → Expected out=1 | Obtained out=1
[PASS]

----- Select input c -----
a=1 b=1 c=0 d=1 sel=10 → Expected out=0 | Obtained out=0
[PASS]
```

```
-----  
          Select input c  
a=0 b=0 c=1 d=0 sel=10 → Expected out=1 | Obtained out=1  
[PASS]  
-----  
  
          Select input d  
a=1 b=1 c=1 d=0 sel=11 → Expected out=0 | Obtained out=0  
[PASS]  
-----  
  
          Select input d  
a=0 b=0 c=0 d=1 sel=11 → Expected out=1 | Obtained out=1  
[PASS]  
-----  
  
          All inputs zero  
a=0 b=0 c=0 d=0 sel=00 → Expected out=0 | Obtained out=0  
[PASS]  
-----  
  
          All inputs zero  
a=0 b=0 c=0 d=0 sel=01 → Expected out=0 | Obtained out=0  
[PASS]  
-----  
  
          All inputs zero  
a=0 b=0 c=0 d=0 sel=10 → Expected out=0 | Obtained out=0  
[PASS]  
-----  
  
          All inputs zero  
a=0 b=0 c=0 d=0 sel=11 → Expected out=0 | Obtained out=0  
[PASS]  
-----  
  
          All inputs one  
a=1 b=1 c=1 d=1 sel=00 → Expected out=1 | Obtained out=1  
[PASS]  
-----  
  
          All inputs one  
a=1 b=1 c=1 d=1 sel=01 → Expected out=1 | Obtained out=1  
[PASS]  
-----  
  
          All inputs one  
a=1 b=1 c=1 d=1 sel=10 → Expected out=1 | Obtained out=1  
[PASS]  
-----  
  
          All inputs one  
a=1 b=1 c=1 d=1 sel=11 → Expected out=1 | Obtained out=1  
[PASS]  
-----  
  
          All strategic functional verification tests completed.  
Simulation complete via $finish(1) at time 80 NS + 0  
../RTL/tb/tb_mux4tol.v:53      $finish;  
xcelium>
```

Full_adder:



```
xcelium>
xcelium> # Run the simulation for 100 ns
xcelium> run 500 ns

===== Functional Verification of Full Adder =====

-----
Inputs: Ai=0 Bi=0 Cini=0
Expected → Di=0 Couti=0 | Obtained → Di=0 Couti=0
[PASS]
-----

-----  
Inputs: Ai=0 Bi=0 Cini=1
Expected → Di=1 Couti=0 | Obtained → Di=1 Couti=0
[PASS]
-----  
Inputs: Ai=0 Bi=1 Cini=0
Expected → Di=1 Couti=0 | Obtained → Di=1 Couti=0
[PASS]
-----  
Inputs: Ai=0 Bi=1 Cini=1
Expected → Di=0 Couti=1 | Obtained → Di=0 Couti=1
[PASS]
```

```

-----
Inputs: Ai=1 Bi=0 Cini=0
Expected → Di=1 Couti=0 | Obtained → Di=1 Couti=0
[PASS]

-----
Inputs: Ai=1 Bi=0 Cini=1
Expected → Di=0 Couti=1 | Obtained → Di=0 Couti=1
[PASS]

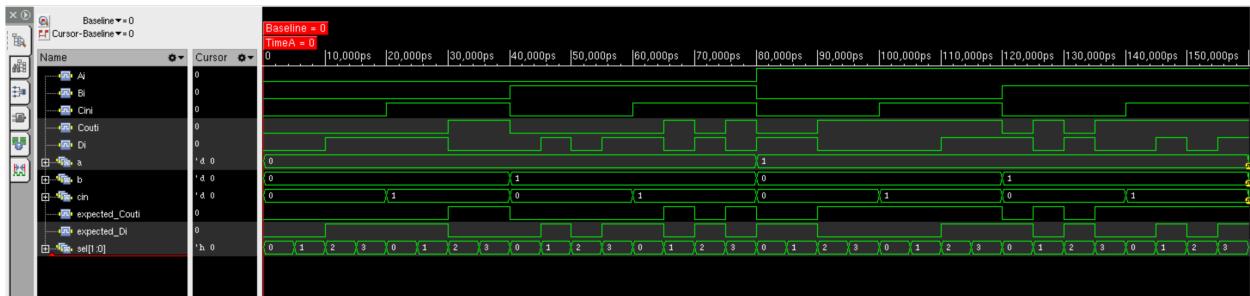
-----
Inputs: Ai=1 Bi=1 Cini=0
Expected → Di=0 Couti=1 | Obtained → Di=0 Couti=1
[PASS]

-----
Inputs: Ai=1 Bi=1 Cini=1
Expected → Di=1 Couti=1 | Obtained → Di=1 Couti=1
[PASS]

All Full Adder functional verification tests completed.

Simulation complete via $finish(1) at time 40 NS + 0
.../RTL/tb/tb_full_adder.v:44           $finish;
xcelium>
```

Arithmetic_unit



```

xcelium>
xcelium> # Run the simulation for 100 ns
xcelium> run 500 ns
=====
===== Functional Verification: Arithmetic Unit =====
-----
Operation: Transfer A (sel=00, Cin=0)
Ai=0, Bi=0, Cini=0, sel=00 → Expected Di=0, Couti=0 | Obtained Di=0, Couti=0
[PASS]
-----
Operation: Addition A+B (sel=01, Cin=0)
Ai=0, Bi=0, Cini=0, sel=01 → Expected Di=0, Couti=0 | Obtained Di=0, Couti=0
[PASS]
-----
Operation: ubtraction A-B-1 (sel=10, Cin=0)
Ai=0, Bi=0, Cini=0, sel=10 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]
-----
Operation: Decrement A (sel=11, Cin=0)
Ai=0, Bi=0, Cini=0, sel=11 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]
-----
Operation: Increment A (sel=00, Cin=1)
Ai=0, Bi=0, Cini=1, sel=00 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]
-----
Operation: Addition A+B+1 (sel=01, Cin=1)
Ai=0, Bi=0, Cini=1, sel=01 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]
-----
Operation: Subtraction A-B (sel=10, Cin=1)
Ai=0, Bi=0, Cini=1, sel=10 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]
-----
Operation: Transfer A (sel=11, Cin=1)
Ai=0, Bi=0, Cini=1, sel=11 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]
-----
Operation: Transfer A (sel=00, Cin=0)
Ai=0, Bi=1, Cini=0, sel=00 → Expected Di=0, Couti=0 | Obtained Di=0, Couti=0
[PASS]
-----
Operation: Addition A+B (sel=01, Cin=0)
Ai=0, Bi=1, Cini=0, sel=01 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]
-----
Operation: ubtraction A-B-1 (sel=10, Cin=0)
Ai=0, Bi=1, Cini=0, sel=10 → Expected Di=0, Couti=0 | Obtained Di=0, Couti=0
[PASS]
-----
Operation: Decrement A (sel=11, Cin=0)
Ai=0, Bi=1, Cini=0, sel=11 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]
-----
Operation: Increment A (sel=00, Cin=1)
Ai=0, Bi=1, Cini=1, sel=00 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]
-----
Operation: Addition A+B+1 (sel=01, Cin=1)
Ai=0, Bi=1, Cini=1, sel=01 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]
-----
Operation: Subtraction A-B (sel=10, Cin=1)
Ai=0, Bi=1, Cini=1, sel=10 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]
-----
Operation: Transfer A (sel=11, Cin=1)
Ai=0, Bi=1, Cini=1, sel=11 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]
-----
```

```

-----
Operation:      Transfer A (sel=00, Cin=0)
Ai=1, Bi=0, Cini=0, sel=00 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]

-----
Operation:      Addition A+B (sel=01, Cin=0)
Ai=1, Bi=0, Cini=0, sel=01 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]

-----
Operation:      ubtraction A-B-1 (sel=10, Cin=0)
Ai=1, Bi=0, Cini=0, sel=10 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]

-----
Operation:      Decrement A (sel=11, Cin=0)
Ai=1, Bi=0, Cini=0, sel=11 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]

-----
Operation:      Increment A (sel=00, Cin=1)
Ai=1, Bi=0, Cini=1, sel=00 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]

-----
Operation:      Addition A+B+1 (sel=01, Cin=1)
Ai=1, Bi=0, Cini=1, sel=01 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]

-----
Operation:      Subtraction A-B (sel=10, Cin=1)
Ai=1, Bi=0, Cini=1, sel=10 → Expected Di=1, Couti=1 | Obtained Di=1, Couti=1
[PASS]

-----
Operation:      Transfer A (sel=11, Cin=1)
Ai=1, Bi=0, Cini=1, sel=11 → Expected Di=1, Couti=1 | Obtained Di=1, Couti=1
[PASS]

-----
Operation:      Transfer A (sel=00, Cin=0)
Ai=1, Bi=1, Cini=0, sel=00 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]

-----
Operation:      Addition A+B (sel=01, Cin=0)
Ai=1, Bi=1, Cini=0, sel=01 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]

-----
Operation:      ubtraction A-B-1 (sel=10, Cin=0)
Ai=1, Bi=1, Cini=0, sel=10 → Expected Di=1, Couti=0 | Obtained Di=1, Couti=0
[PASS]

-----
Operation:      Decrement A (sel=11, Cin=0)
Ai=1, Bi=1, Cini=0, sel=11 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]

-----
Operation:      Increment A (sel=00, Cin=1)
Ai=1, Bi=1, Cini=1, sel=00 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]

-----
Operation:      Addition A+B+1 (sel=01, Cin=1)
Ai=1, Bi=1, Cini=1, sel=01 → Expected Di=1, Couti=1 | Obtained Di=1, Couti=1
[PASS]

-----
Operation:      Subtraction A-B (sel=10, Cin=1)
Ai=1, Bi=1, Cini=1, sel=10 → Expected Di=0, Couti=1 | Obtained Di=0, Couti=1
[PASS]

-----
Operation:      Transfer A (sel=11, Cin=1)
Ai=1, Bi=1, Cini=1, sel=11 → Expected Di=1, Couti=1 | Obtained Di=1, Couti=1
[PASS]

All functional verification tests completed.
Simulation complete via $finish(1) at time 160 NS + 0
../../../RTL/tb/tb_arithmetic_unit.v:39           $finish;

```

Logic_unit



```
xcelium>
xcelium> # Run the simulation for 100 ns
xcelium> run 500 ns
===== Functional Verification: Logic Unit =====

--- Logic AND Tests (sel=00) ---

Logic Operation: A AND B (sel=00)
Inputs: Ai=1, Bi=1
Expected → Ei=1
Obtained → Ei=1
[PASS]
-----
Logic Operation: A AND B (sel=00)
Inputs: Ai=1, Bi=0
Expected → Ei=0
Obtained → Ei=0
[PASS]
-----
Logic Operation: A AND B (sel=00)
Inputs: Ai=0, Bi=1
Expected → Ei=0
Obtained → Ei=0
[PASS]
```

```
-----  
Logic Operation: A AND B (sel=00)  
Inputs: Ai=0, Bi=0  
Expected → Ei=0  
Obtained → Ei=0  
[PASS]  
-----  
  
--- Logic OR Tests (sel=01) ---  
-----  
Logic Operation: A OR B (sel=01)  
Inputs: Ai=1, Bi=0  
Expected → Ei=1  
Obtained → Ei=1  
[PASS]  
-----  
  
-----  
Logic Operation: A OR B (sel=01)  
Inputs: Ai=0, Bi=1  
Expected → Ei=1  
Obtained → Ei=1  
[PASS]  
-----  
  
-----  
Logic Operation: A OR B (sel=01)  
Inputs: Ai=0, Bi=0  
Expected → Ei=0  
Obtained → Ei=0  
[PASS]  
-----  
  
-----  
Logic Operation: A OR B (sel=01)  
Inputs: Ai=1, Bi=1  
Expected → Ei=1  
Obtained → Ei=1  
[PASS]  
-----  
  
--- Logic XOR Tests (sel=10) ---  
-----  
Logic Operation: A XOR B (sel=10)  
Inputs: Ai=1, Bi=0  
Expected → Ei=1  
Obtained → Ei=1  
[PASS]  
-----  
  
-----  
Logic Operation: A XOR B (sel=10)  
Inputs: Ai=0, Bi=1  
Expected → Ei=1  
Obtained → Ei=1  
[PASS]  
-----  
  
-----  
Logic Operation: A XOR B (sel=10)  
Inputs: Ai=0, Bi=0  
Expected → Ei=0  
Obtained → Ei=0  
[PASS]  
-----
```

```
-----  
Logic Operation: A XOR B (sel=10)  
Inputs: Ai=1, Bi=1  
Expected → Ei=0  
Obtained → Ei=0  
[PASS]  
-----
```

```
--- Logic NOT Tests (sel=11) ---  
-----  
Logic Operation: NOT A (sel=11)  
Inputs: Ai=0, Bi=0  
Expected → Ei=1  
Obtained → Ei=1  
[PASS]  
-----
```

```
-----  
Logic Operation: NOT A (sel=11)  
Inputs: Ai=1, Bi=1  
Expected → Ei=0  
Obtained → Ei=0  
[PASS]  
-----
```

```
All functional verification tests for Logic Unit completed.  
Simulation complete via $finish(1) at time 70 NS + 0  
./RTL/tb/tb logic unit.v:85 $finish;
```

ALU_1bit



```

xcelium>
xcelium> # Run the simulation for 100 ns
xcelium> run 500 ns
===== Functional Verification: 1-bit ALU =====

--- Arithmetic Tests ---

Test: Transfer A (sel=0000, cin=0)
sel=0000 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=0 | Obtained Fi=0 Couti=0
[PASS] Arithmetic
-----

Test: Addition A+B (sel=0001, cin=0)
sel=0001 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=0 | Obtained Fi=0 Couti=0
[PASS] Arithmetic
-----

Test: Subtraction with borrow A-B-1 (sel=0010, cin=0)
sel=0010 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----

Test: Decrement A-1 (sel=0011, cin=0)
sel=0011 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----

Test: Increment A (sel=0000, cin=1)
sel=0000 Ai=0 Bi=0 Cin=1 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----

Test: Addition with carry A+B+1 (sel=0001, cin=1)
sel=0001 Ai=0 Bi=0 Cin=1 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----

Test: Subtraction A-B (sel=0010, cin=1)
sel=0010 Ai=0 Bi=0 Cin=1 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
-----

Test: Transfer A (sel=0011, cin=1)
sel=0011 Ai=0 Bi=0 Cin=1 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
-----

Test: Transfer A (sel=0000, cin=0)
sel=0000 Ai=0 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=0 | Obtained Fi=0 Couti=0
[PASS] Arithmetic
-----

Test: Addition A+B (sel=0001, cin=0)
sel=0001 Ai=0 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----
```

```
Test: Subtraction with borrow A-B-1 (sel=0010, cin=0)
sel=0010 Ai=0 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=0 | Obtained Fi=0 Couti=0
[PASS] Arithmetic
-----

Test: Decrement A-1 (sel=0011, cin=0)
sel=0011 Ai=0 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----

Test: Increment A (sel=0000, cin=1)
sel=0000 Ai=0 Bi=1 Cin=1 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----

Test: Addition with carry A+B+1 (sel=0001, cin=1)
sel=0001 Ai=0 Bi=1 Cin=1 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
-----

Test: Subtraction A-B (sel=0010, cin=1)
sel=0010 Ai=0 Bi=1 Cin=1 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----

Test: Transfer A (sel=0011, cin=1)
sel=0011 Ai=0 Bi=1 Cin=1 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
-----

Test: Transfer A (sel=0000, cin=0)
sel=0000 Ai=1 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----

Test: Addition A+B (sel=0001, cin=0)
sel=0001 Ai=1 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----

Test: Subtraction with borrow A-B-1 (sel=0010, cin=0)
sel=0010 Ai=1 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
-----

Test: Decrement A-1 (sel=0011, cin=0)
sel=0011 Ai=1 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
-----

Test: Increment A (sel=0000, cin=1)
sel=0000 Ai=1 Bi=0 Cin=1 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
```

```
Test: Addition with carry A+B+1 (sel=0001, cin=1)
sel=0001 Ai=1 Bi=0 Cin=1 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
-----

Test: Subtraction A-B (sel=0010, cin=1)
sel=0010 Ai=1 Bi=0 Cin=1 A_prev=0 A_next=0 → Expected Fi=1 Couti=1 | Obtained Fi=1 Couti=1
[PASS] Arithmetic
-----

Test: Transfer A (sel=0011, cin=1)
sel=0011 Ai=1 Bi=0 Cin=1 A_prev=0 A_next=0 → Expected Fi=1 Couti=1 | Obtained Fi=1 Couti=1
[PASS] Arithmetic
-----

Test: Transfer A (sel=0000, cin=0)
sel=0000 Ai=1 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----

Test: Addition A+B (sel=0001, cin=0)
sel=0001 Ai=1 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
-----

Test: Subtraction with borrow A-B-1 (sel=0010, cin=0)
sel=0010 Ai=1 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=0 | Obtained Fi=1 Couti=0
[PASS] Arithmetic
-----

Test: Decrement A-1 (sel=0011, cin=0)
sel=0011 Ai=1 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
-----

Test: Increment A (sel=0000, cin=1)
sel=0000 Ai=1 Bi=1 Cin=1 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
-----

Test: Addition with carry A+B+1 (sel=0001, cin=1)
sel=0001 Ai=1 Bi=1 Cin=1 A_prev=0 A_next=0 → Expected Fi=1 Couti=1 | Obtained Fi=1 Couti=1
[PASS] Arithmetic
-----

Test: Subtraction A-B (sel=0010, cin=1)
sel=0010 Ai=1 Bi=1 Cin=1 A_prev=0 A_next=0 → Expected Fi=0 Couti=1 | Obtained Fi=0 Couti=1
[PASS] Arithmetic
-----

Test: Transfer A (sel=0011, cin=1)
sel=0011 Ai=1 Bi=1 Cin=1 A_prev=0 A_next=0 → Expected Fi=1 Couti=1 | Obtained Fi=1 Couti=1
[PASS] Arithmetic
```

```
--- Logic Operation Tests ---

Test: Logic AND (sel=0100)
sel=0100 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=x | Obtained Fi=0 Couti=0
[PASS] Logic/Shift
-----

Test: Logic OR (sel=0101)
sel=0101 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=x | Obtained Fi=0 Couti=0
[PASS] Logic/Shift
-----

Test: Logic XOR (sel=0110)
sel=0110 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=x | Obtained Fi=0 Couti=0
[PASS] Logic/Shift
-----

Test: Logic NOT (sel=0111)
sel=0111 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=x | Obtained Fi=1 Couti=0
[PASS] Logic/Shift
-----

Test: Logic AND (sel=0100)
sel=0100 Ai=0 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=x | Obtained Fi=0 Couti=0
[PASS] Logic/Shift
-----

Test: Logic OR (sel=0101)
sel=0101 Ai=0 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=x | Obtained Fi=1 Couti=0
[PASS] Logic/Shift
-----

Test: Logic XOR (sel=0110)
sel=0110 Ai=0 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=x | Obtained Fi=1 Couti=0
[PASS] Logic/Shift
-----

Test: Logic NOT (sel=0111)
sel=0111 Ai=0 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=x | Obtained Fi=1 Couti=0
[PASS] Logic/Shift
-----

Test: Logic AND (sel=0100)
sel=0100 Ai=1 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=x | Obtained Fi=0 Couti=0
[PASS] Logic/Shift
-----

Test: Logic OR (sel=0101)
sel=0101 Ai=1 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=x | Obtained Fi=1 Couti=0
[PASS] Logic/Shift
-----

Test: Logic XOR (sel=0110)
sel=0110 Ai=1 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=x | Obtained Fi=1 Couti=1
[PASS] Logic/Shift
```

```

Test: Logic NOT (sel=0111)
sel=0111 Ai=1 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=x | Obtained Fi=0 Couti=1
[PASS] Logic/Shift
-----

Test: Logic AND (sel=0100)
sel=0100 Ai=1 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=x | Obtained Fi=1 Couti=0
[PASS] Logic/Shift
-----

Test: Logic OR (sel=0101)
sel=0101 Ai=1 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=1 Couti=x | Obtained Fi=1 Couti=1
[PASS] Logic/Shift
-----

Test: Logic XOR (sel=0110)
sel=0110 Ai=1 Bi=1 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=x | Obtained Fi=0 Couti=0
[PASS] Logic/Shift
-----
```

--- Shift Operation Tests ---

```

Test: Shift Right Operation (sel=10xx)
sel=1000 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=x | Obtained Fi=0 Couti=0
[PASS] Logic/Shift
-----
```

```

Test: Shift Left Operation (sel=11xx)
sel=1100 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=0 → Expected Fi=0 Couti=x | Obtained Fi=0 Couti=0
[PASS] Logic/Shift
-----
```

```

Test: Shift Right Operation (sel=10xx)
sel=1000 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=1 → Expected Fi=0 Couti=x | Obtained Fi=0 Couti=0
[PASS] Logic/Shift
-----
```

```

Test: Shift Left Operation (sel=11xx)
sel=1100 Ai=0 Bi=0 Cin=0 A_prev=0 A_next=1 → Expected Fi=1 Couti=x | Obtained Fi=1 Couti=0
[PASS] Logic/Shift
-----
```

```

Test: Shift Right Operation (sel=10xx)
sel=1000 Ai=0 Bi=0 Cin=0 A_prev=1 A_next=0 → Expected Fi=1 Couti=x | Obtained Fi=1 Couti=0
[PASS] Logic/Shift
-----
```

```

Test: Shift Left Operation (sel=11xx)
sel=1100 Ai=0 Bi=0 Cin=0 A_prev=1 A_next=0 → Expected Fi=0 Couti=x | Obtained Fi=0 Couti=0
[PASS] Logic/Shift
-----
```

```

All functional verification tests completed.
Simulation complete via $finish(1) at time 280 NS + 0
.../RTL/tb/tb_alu_1bit.v:108      $finish;
xcelium>
```

32bit ALU Modular



```
xcelium>
xcelium> # Run the simulation for 100 ns
xcelium> run 500 ns

===== Functional Verification of 32-bit Modular ALU =====

--- Arithmetic Operation Tests ---

----- Transfer A -----
sel=0x0 A=0x00000000 (0) B=0x00000000 (0) Cin=0 DinL=0 DinR=0
Expected → F=0x00000000 (0) Cout=0
Obtained → F=0x00000000 (0) Cout=0
[PASS] Arithmetic

----- Increment A -----
sel=0x0 A=0xffffffff (4294967295) B=0x00000000 (0) Cin=1 DinL=0 DinR=0
Expected → F=0x00000001 (0) Cout=1
Obtained → F=0x00000001 (0) Cout=1
[PASS] Arithmetic

----- Addition A+B -----
sel=0x1 A=0xffffffff (4294967295) B=0xffffffff (4294967295) Cin=0 DinL=0 DinR=0
Expected → F=0xfffffff (4294967294) Cout=1
Obtained → F=0xfffffff (4294967294) Cout=1
[PASS] Arithmetic
```

```
-----  
          Addition A+B+1  
sel=0x1 A=0x00000001 (1) B=0x00000001 (1) Cin=1 DinL=0 DinR=0  
Expected → F=0x00000003 (3) Cout=0  
Obtained → F=0x00000003 (3) Cout=0  
[PASS] Arithmetic  
-----  
  
-----  
          Subtraction A-B-1  
sel=0x2 A=0x00000004 (4) B=0x00000003 (3) Cin=0 DinL=0 DinR=0  
Expected → F=0x00000000 (0) Cout=1  
Obtained → F=0x00000000 (0) Cout=1  
[PASS] Arithmetic  
-----  
  
-----  
          Subtraction A-B  
sel=0x2 A=0x00000004 (4) B=0x00000003 (3) Cin=1 DinL=0 DinR=0  
Expected → F=0x00000001 (1) Cout=1  
Obtained → F=0x00000001 (1) Cout=1  
[PASS] Arithmetic  
-----  
  
-----  
          Subtraction A-B-1 (B>A)  
sel=0x2 A=0x00000003 (3) B=0x00000004 (4) Cin=0 DinL=0 DinR=0  
Expected → F=0xffffffe (4294967294) Cout=0  
Obtained → F=0xffffffe (4294967294) Cout=0  
[PASS] Arithmetic  
-----  
  
-----  
          Subtraction A-B (B>A)  
sel=0x2 A=0x00000003 (3) B=0x00000004 (4) Cin=1 DinL=0 DinR=0  
Expected → F=0xffffffff (4294967295) Cout=0  
Obtained → F=0xffffffff (4294967295) Cout=0  
[PASS] Arithmetic  
-----  
  
-----  
          Decrement A  
sel=0x3 A=0x00000000 (0) B=0x00000004 (4) Cin=0 DinL=0 DinR=0  
Expected → F=0xffffffff (4294967295) Cout=0  
Obtained → F=0xffffffff (4294967295) Cout=0  
[PASS] Arithmetic  
-----  
  
-----  
          Decrement A  
sel=0x3 A=0x00000001 (1) B=0x00000004 (4) Cin=0 DinL=0 DinR=0  
Expected → F=0x00000000 (0) Cout=1  
Obtained → F=0x00000000 (0) Cout=1  
[PASS] Arithmetic  
-----  
  
-----  
          Transfer A  
sel=0x3 A=0xffffffff (4294967295) B=0x00000004 (4) Cin=1 DinL=0 DinR=0  
Expected → F=0xffffffff (4294967295) Cout=1  
Obtained → F=0xffffffff (4294967295) Cout=1  
[PASS] Arithmetic  
-----
```

```
-----  
          Addition Overflow Case  
sel=0x1 A=0x80000000 (2147483648) B=0x7fffffff (2147483647) Cin=0 DinL=0 DinR=0  
Expected → F=0xffffffff (4294967295) Cout=0  
Obtained → F=0xffffffff (4294967295) Cout=0  
[PASS] Arithmetic  
-----  
  
--- Logic Operation Tests ---  
-----  
          AND Operation  
sel=0x4 A=0x0f0f0f0f (252645135) B=0xf0f0f0f0 (4042322160) Cin=0 DinL=0 DinR=0  
Expected → F=0x00000000 (0) Cout=0  
Obtained → F=0x00000000 (0) Cout=0  
[PASS] Logic/Shift  
-----  
  
          OR Operation  
sel=0x5 A=0x0f0f0f0f (252645135) B=0xf0f0f0f0 (4042322160) Cin=0 DinL=0 DinR=0  
Expected → F=0xffffffff (4294967295) Cout=0  
Obtained → F=0xffffffff (4294967295) Cout=0  
[PASS] Logic/Shift  
-----  
  
          XOR Operation  
sel=0x6 A=0aaaaaaaaa (2863311530) B=0x55555555 (1431655765) Cin=0 DinL=0 DinR=0  
Expected → F=0xffffffff (4294967295) Cout=0  
Obtained → F=0xffffffff (4294967295) Cout=0  
[PASS] Logic/Shift  
-----  
  
          NOT A Operation  
sel=0x7 A=0x00000000 (0) B=0x00000000 (0) Cin=0 DinL=0 DinR=0  
Expected → F=0xffffffff (4294967295) Cout=0  
Obtained → F=0xffffffff (4294967295) Cout=0  
[PASS] Logic/Shift  
-----  
  
--- Shift Operation Tests ---  
-----  
          Shift Right Operation  
sel=0x8 A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=0  
Expected → F=0x091a2b3c (152709948) Cout=0  
Obtained → F=0x091a2b3c (152709948) Cout=0  
[PASS] Logic/Shift  
-----  
  
          Shift Right Operation  
sel=0xb A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=0  
Expected → F=0x091a2b3c (152709948) Cout=0  
Obtained → F=0x091a2b3c (152709948) Cout=0  
[PASS] Logic/Shift  
-----  
  
          Shift Left Operation  
sel=0xc A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=0  
Expected → F=0x2468acf0 (610839792) Cout=0  
Obtained → F=0x2468acf0 (610839792) Cout=0  
[PASS] Logic/Shift
```

```
-----  
Shift Left Operation  
sel=0xd A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=0  
Expected → F=0x2468acf0 (610839792) Cout=0  
Obtained → F=0x2468acf0 (610839792) Cout=0  
[PASS] Logic/Shift  
-----  
  
-----  
Shift Right Operation  
sel=0x8 A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=1  
Expected → F=0x891a2b3c (2300193596) Cout=0  
Obtained → F=0x891a2b3c (2300193596) Cout=0  
[PASS] Logic/Shift  
-----  
  
-----  
Shift Right Operation  
sel=0xb A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=1  
Expected → F=0x891a2b3c (2300193596) Cout=0  
Obtained → F=0x891a2b3c (2300193596) Cout=0  
[PASS] Logic/Shift  
-----  
  
-----  
Shift Left Operation  
sel=0xc A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=1  
Expected → F=0x2468acf0 (610839792) Cout=0  
Obtained → F=0x2468acf0 (610839792) Cout=0  
[PASS] Logic/Shift  
-----  
  
-----  
Shift Left Operation  
sel=0xd A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=1  
Expected → F=0x2468acf0 (610839792) Cout=0  
Obtained → F=0x2468acf0 (610839792) Cout=0  
[PASS] Logic/Shift  
-----  
  
-----  
Shift Right Operation  
sel=0x8 A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=0  
Expected → F=0x091a2b3c (152709948) Cout=0  
Obtained → F=0x091a2b3c (152709948) Cout=0  
[PASS] Logic/Shift  
-----  
  
-----  
Shift Right Operation  
sel=0xb A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=0  
Expected → F=0x091a2b3c (152709948) Cout=0  
Obtained → F=0x091a2b3c (152709948) Cout=0  
[PASS] Logic/Shift  
-----  
  
-----  
Shift Left Operation  
sel=0xc A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=0  
Expected → F=0x2468acf1 (610839793) Cout=0  
Obtained → F=0x2468acf1 (610839793) Cout=0  
[PASS] Logic/Shift  
-----
```

```
    Shift Left Operation
sel=0xd A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=0
Expected → F=0x2468acf1 (610839793) Cout=0
Obtained → F=0x2468acf1 (610839793) Cout=0
[PASS] Logic/Shift
-----


    Shift Right Operation
sel=0x8 A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=1
Expected → F=0x891a2b3c (2300193596) Cout=0
Obtained → F=0x891a2b3c (2300193596) Cout=0
[PASS] Logic/Shift
-----


    Shift Right Operation
sel=0xb A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=1
Expected → F=0x891a2b3c (2300193596) Cout=0
Obtained → F=0x891a2b3c (2300193596) Cout=0
[PASS] Logic/Shift
-----


    Shift Left Operation
sel=0xc A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=1
Expected → F=0x2468acf1 (610839793) Cout=0
Obtained → F=0x2468acf1 (610839793) Cout=0
[PASS] Logic/Shift
-----


    Shift Left Operation
sel=0xd A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=1
Expected → F=0x2468acf1 (610839793) Cout=0
Obtained → F=0x2468acf1 (610839793) Cout=0
[PASS] Logic/Shift
-----


-- Random Directed Tests --


    Random Test
sel=0xd A=0x12153524 (303379748) B=0xc0895e81 (3230228097) Cin=1 DinL=1 DinR=1
Expected → F=0x242a6a49 (606759497) Cout=0
Obtained → F=0x242a6a49 (606759497) Cout=0
[PASS] Logic/Shift
-----


    Random Test
sel=0xd A=0xb2c28465 (2999092325) B=0x89375212 (2302104082) Cin=1 DinL=1 DinR=0
Expected → F=0x658508cb (1703217355) Cout=0
Obtained → F=0x658508cb (1703217355) Cout=0
[PASS] Logic/Shift
-----


    Random Test
sel=0xa A=0x76d457ed (1993627629) B=0x462df78c (1177417612) Cin=1 DinL=0 DinR=1
Expected → F=0xbb6a2bf6 (3144297462) Cout=0
Obtained → F=0xbb6a2bf6 (3144297462) Cout=0
[PASS] Logic/Shift
```

```
-----  
          Random Test  
sel=0xe A=0x72aff7e5 (1924134885) B=0xbbd27277 (3151131255) Cin=0 DinL=1 DinR=0  
Expected → F=0xe55fefcb (3848269771) Cout=0  
Obtained → F=0xe55fefcb (3848269771) Cout=0  
[PASS] Logic/Shift  
  
-----  
          Random Test  
sel=0x5 A=0xf4007ae8 (4093672168) B=0xe2ca4ec5 (3804909253) Cin=0 DinL=1 DinR=1  
Expected → F=0xf6ca7eed (4140465901) Cout=0  
Obtained → F=0xf6ca7eed (4140465901) Cout=0  
[PASS] Logic/Shift  
  
-----  
          Random Test  
sel=0xd A=0xb1ef6263 (2985255523) B=0x0573870a (91457290) Cin=0 DinL=0 DinR=0  
Expected → F=0x63dec4c6 (1675543750) Cout=0  
Obtained → F=0x63dec4c6 (1675543750) Cout=0  
[PASS] Logic/Shift  
  
-----  
          Random Test  
sel=0x5 A=0xcb203e96 (3407888022) B=0x8983b813 (2307110931) Cin=1 DinL=1 DinR=1  
Expected → F=0xcba3be97 (3416506007) Cout=0  
Obtained → F=0xcba3be97 (3416506007) Cout=0  
[PASS] Logic/Shift  
  
-----  
          Random Test  
sel=0xa A=0x81174a02 (2165787138) B=0xd7563eae (3612753582) Cin=1 DinL=1 DinR=1  
Expected → F=0xc08ba501 (3230377217) Cout=0  
Obtained → F=0xc08ba501 (3230377217) Cout=0  
[PASS] Logic/Shift  
  
-----  
          Random Test  
sel=0x8 A=0xe5730aca (3849521866) B=0x9e314c3c (2654030908) Cin=0 DinL=0 DinR=1  
Expected → F=0xf2b98565 (4072244581) Cout=0  
Obtained → F=0xf2b98565 (4072244581) Cout=0  
[PASS] Logic/Shift  
  
-----  
          Random Test  
sel=0xe A=0x3c20f378 (1008792440) B=0xc48a1289 (3297383049) Cin=1 DinL=0 DinR=0  
Expected → F=0x7841e6f0 (2017584880) Cout=0  
Obtained → F=0x7841e6f0 (2017584880) Cout=0  
[PASS] Logic/Shift  
  
-----  
          Random Test  
sel=0xf A=0xde7502bc (3732210364) B=0x150fdd2a (353361194) Cin=1 DinL=1 DinR=1  
Expected → F=0xbcea0579 (3169453433) Cout=0  
Obtained → F=0xbcea0579 (3169453433) Cout=0  
[PASS] Logic/Shift
```

```
-----  
          Random Test  
sel=0x9 A=0x9dcc603b (2647416891) B=0x1d06333a (486945594) Cin=0 DinL=1 DinR=1  
Expected → F=0xcee6301d (3471192093) Cout=0  
Obtained → F=0xcee6301d (3471192093) Cout=0  
[PASS] Logic/Shift  
-----
```

```
-----  
          Random Test  
sel=0x7 A=0x31230762 (824379234) B=0x2635fb4c (641071948) Cin=1 DinL=1 DinR=0  
Expected → F=0xcedcf89d (3470588061) Cout=0  
Obtained → F=0xcedcf89d (3470588061) Cout=0  
[PASS] Logic/Shift  
-----
```

```
-----  
          Random Test  
sel=0x0 A=0xcf4569f (3485750943) B=0xae7d945c (2927465564) Cin=1 DinL=1 DinR=1  
Expected → F=0xcf456a0 (3485750944) Cout=0  
Obtained → F=0xcf456a0 (3485750944) Cout=0  
[PASS] Arithmetic  
-----
```

```
-----  
          Random Test  
sel=0x8 A=0xebfec0d7 (3959341271) B=0xa8c7fc51 (2831678545) Cin=0 DinL=0 DinR=0  
Expected → F=0x75ff606b (1979670635) Cout=0  
Obtained → F=0x75ff606b (1979670635) Cout=0  
[PASS] Logic/Shift  
-----
```

```
-----  
          Random Test  
sel=0x9 A=0xbb825a77 (3145882231) B=0x1ef2ed3d (519236925) Cin=0 DinL=0 DinR=1  
Expected → F=0xddc12d3b (3720424763) Cout=0  
Obtained → F=0xddc12d3b (3720424763) Cout=0  
[PASS] Logic/Shift  
-----
```

```
-----  
          Random Test  
sel=0x9 A=0x0fd28f1f (265457439) B=0xe9ebf6d3 (3924555475) Cin=1 DinL=0 DinR=1  
Expected → F=0x87e9478f (2280212367) Cout=0  
Obtained → F=0x87e9478f (2280212367) Cout=0  
[PASS] Logic/Shift  
-----
```

```
-----  
          Random Test  
sel=0xc A=0x9ff2ae3f (2683481663) B=0x150caf2a (353152810) Cin=0 DinL=0 DinR=0  
Expected → F=0x3fe55c7e (1071996030) Cout=0  
Obtained → F=0x3fe55c7e (1071996030) Cout=0  
[PASS] Logic/Shift  
-----
```

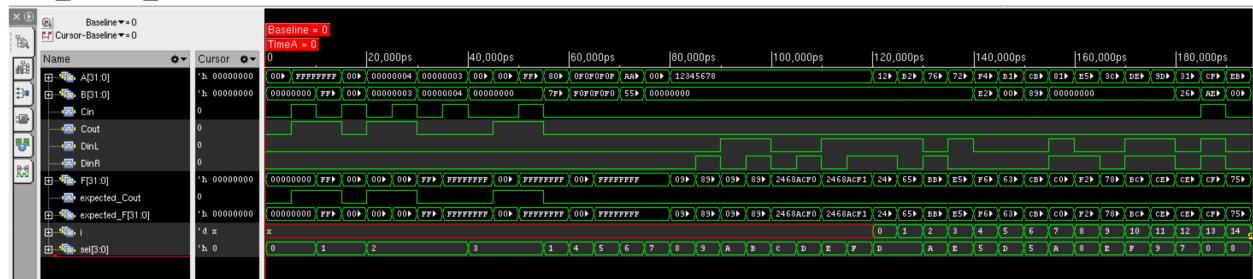
```
-----  
          Random Test  
sel=0x3 A=0x7d3599fa (2100664826) B=0x937dbc26 (2474490918) Cin=1 DinL=1 DinR=1  
Expected → F=0x7d3599fa (2100664826) Cout=1  
Obtained → F=0x7d3599fa (2100664826) Cout=1  
[PASS] Arithmetic  
-----
```

```

----- Random Test -----
sel=0xa A=0xaffd8565f (2950190687) B=0x22290d44 (573115716) Cin=1 DinL=1 DinR=0
Expected → F=0x57ec2b2f (1475095343) Cout=0
Obtained → F=0x57ec2b2f (1475095343) Cout=0
[PASS] Logic/Shift

----- All functional verification tests completed.
Simulation complete via $finish(1) at time 260 NS + 0
.../RTL/tb/tb_alu_32bit_modular.v:117           $finish;
xcelium>
```

Alu_32bit_behavioral



```

xcelium>
xcelium> # Run the simulation for 100 ns
xcelium> run 500 ns
===== Functional Verification of Behavioral 32-bit ALU =====

--- Arithmetic Operation Tests ---
----- Transfer A -----
sel=0x0 A=0x00000000 B=0x00000000 Cin=0 → Expected F=0x00000000 Cout=0 | Obtained F=0x00000000 Cout=0
[PASS]

----- Increment A -----
sel=0x0 A=0xffffffff B=0x00000000 Cin=1 → Expected F=0x00000000 Cout=1 | Obtained F=0x00000000 Cout=1
[PASS]

----- Addition A+B (Max values) -----
sel=0x1 A=0xffffffff B=0xffffffff Cin=0 → Expected F=0xfffffff8 Cout=1 | Obtained F=0xfffffff8 Cout=1
[PASS]

----- Addition A+B+1 -----
sel=0x1 A=0x00000001 B=0x00000001 Cin=1 → Expected F=0x00000003 Cout=0 | Obtained F=0x00000003 Cout=0
[PASS]
```

```
-----  
          Subtraction A-B-1  
sel=0x2 A=0x00000004 B=0x00000003 Cin=0 → Expected F=0x00000000 Cout=1 | Obtained F=0x00000000 Cout=1  
[PASS]  
-----  
  
          Subtraction A-B  
sel=0x2 A=0x00000004 B=0x00000003 Cin=1 → Expected F=0x00000001 Cout=1 | Obtained F=0x00000001 Cout=1  
[PASS]  
-----  
  
          Subtraction A-B-1 (B>A)  
sel=0x2 A=0x00000003 B=0x00000004 Cin=0 → Expected F=0xffffffffe Cout=0 | Obtained F=0xffffffffe Cout=0  
[PASS]  
-----  
  
          Subtraction A-B (B>A)  
sel=0x2 A=0x00000003 B=0x00000004 Cin=1 → Expected F=0xfffffffff Cout=0 | Obtained F=0xfffffffff Cout=0  
[PASS]  
-----  
  
          Decrement A (underflow)  
sel=0x3 A=0x00000000 B=0x00000000 Cin=0 → Expected F=0xfffffffff Cout=0 | Obtained F=0xfffffffff Cout=0  
[PASS]  
-----  
  
          Decrement A  
sel=0x3 A=0x00000001 B=0x00000000 Cin=0 → Expected F=0x00000000 Cout=1 | Obtained F=0x00000000 Cout=1  
[PASS]  
-----  
  
          Transfer A (sel=0011, Cin=1)  
sel=0x3 A=0xffffffff B=0x00000000 Cin=1 → Expected F=0xfffffffff Cout=1 | Obtained F=0xfffffffff Cout=1  
[PASS]  
-----  
  
          Addition Overflow Case  
sel=0x1 A=0x80000000 B=0x7fffffff Cin=0 → Expected F=0xfffffffff Cout=0 | Obtained F=0xfffffffff Cout=0  
[PASS]  
-----  
  
--- Logic Operation Tests ---  
-----  
          AND Operation  
sel=0x4 A=0xf0f0f0f0 B=0xf0f0f0f0 → Expected F=0x00000000 | Obtained F=0x00000000  
[PASS]  
-----  
  
          OR Operation  
sel=0x5 A=0xf0f0f0f0 B=0xf0f0f0f0 → Expected F=0xffffffff | Obtained F=0xffffffff  
[PASS]
```

```
XOR Operation
sel=0x6 A=0aaaaaaaaa B=0x55555555 → Expected F=0xffffffff | Obtained F=0xffffffff
[PASS]

NOT A Operation
sel=0x7 A=0x00000000 B=0x00000000 → Expected F=0xffffffff | Obtained F=0xffffffff
[PASS]

--- Shift Operation Tests ---
Shift Right Operation
sel=0x8 A=0x12345678 DinL=0 DinR=0 → Expected F=0x091a2b3c | Obtained F=0x091a2b3c
[PASS]

Shift Right Operation
sel=0x9 A=0x12345678 DinL=0 DinR=1 → Expected F=0x891a2b3c | Obtained F=0x891a2b3c
[PASS]

Shift Right Operation
sel=0xa A=0x12345678 DinL=1 DinR=0 → Expected F=0x091a2b3c | Obtained F=0x091a2b3c
[PASS]

Shift Right Operation
sel=0xb A=0x12345678 DinL=1 DinR=1 → Expected F=0x891a2b3c | Obtained F=0x891a2b3c
[PASS]

Shift Left Operation
sel=0xc A=0x12345678 DinL=0 DinR=0 → Expected F=0x2468acf0 | Obtained F=0x2468acf0
[PASS]

Shift Left Operation
sel=0xd A=0x12345678 DinL=0 DinR=1 → Expected F=0x2468acf0 | Obtained F=0x2468acf0
[PASS]

Shift Left Operation
sel=0xe A=0x12345678 DinL=1 DinR=0 → Expected F=0x2468acf1 | Obtained F=0x2468acf1
[PASS]

Shift Left Operation
sel=0xf A=0x12345678 DinL=1 DinR=1 → Expected F=0x2468acf1 | Obtained F=0x2468acf1
[PASS]
```

```
--- Random Directed Tests ---  
-----  
        Random Shift Test  
sel=0xd A=0x12153524 DinL=1 DinR=1 → Expected F=0x242a6a49 | Obtained F=0x242a6a49  
[PASS]  
-----  
        Random Shift Test  
sel=0xd A=0xb2c28465 DinL=1 DinR=0 → Expected F=0x658508cb | Obtained F=0x658508cb  
[PASS]  
-----  
        Random Shift Test  
sel=0xa A=0x76d457ed DinL=0 DinR=1 → Expected F=0xbb6a2bf6 | Obtained F=0xbb6a2bf6  
[PASS]  
-----  
        Random Shift Test  
sel=0xe A=0x72aff7e5 DinL=1 DinR=0 → Expected F=0xe55fefcb | Obtained F=0xe55fefcb  
[PASS]  
-----  
        Random Logic Test  
sel=0x5 A=0xf4007ae8 B=0xe2ca4ec5 → Expected F=0xf6ca7eed | Obtained F=0xf6ca7eed  
[PASS]  
-----  
        Random Shift Test  
sel=0xd A=0xb1ef6263 DinL=0 DinR=0 → Expected F=0x63dec4c6 | Obtained F=0x63dec4c6  
[PASS]  
-----  
        Random Logic Test  
sel=0x5 A=0xcb203e96 B=0x8983b813 → Expected F=0xcba3be97 | Obtained F=0xcba3be97  
[PASS]  
-----  
        Random Shift Test  
sel=0xa A=0x81174a02 DinL=1 DinR=1 → Expected F=0xc08ba501 | Obtained F=0xc08ba501  
[PASS]  
-----  
        Random Shift Test  
sel=0x8 A=0xe5730aca DinL=0 DinR=1 → Expected F=0xf2b98565 | Obtained F=0xf2b98565  
[PASS]  
-----  
        Random Shift Test  
sel=0xe A=0x3c20f378 DinL=0 DinR=0 → Expected F=0x7841e6f0 | Obtained F=0x7841e6f0  
[PASS]  
-----  
        Random Shift Test  
sel=0xf A=0xde7502bc DinL=1 DinR=1 → Expected F=0xbcea0579 | Obtained F=0xbcea0579  
[PASS]
```

```

-----
Random Shift Test
sel=0x9 A=0x9dcc603b DinL=1 DinR=1 → Expected F=0xcee6301d | Obtained F=0xcee6301d
[PASS]

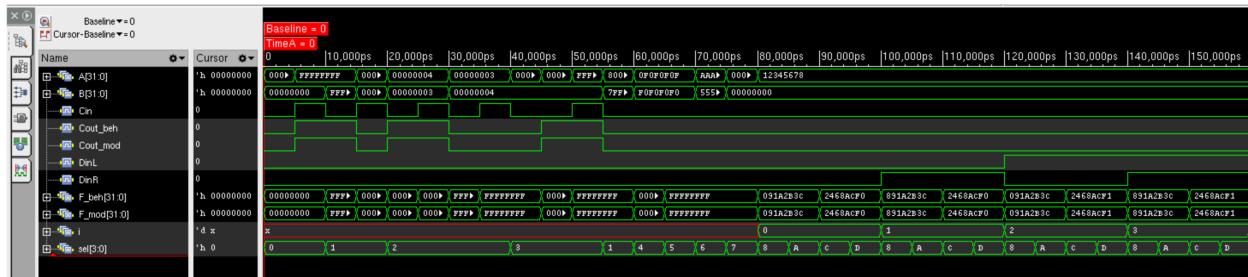
-----
Random Logic Test
sel=0x7 A=0x31230762 B=0x2635fb4c → Expected F=0xcedcf89d | Obtained F=0xcedcf89d
[PASS]

-----
Random Arithmetic Test
sel=0x0 A=0xcf4569f B=0xae7d945c Cin=1 → Expected F=0xcf456a0 Cout=0 | Obtained F=0xcf456a0 Cout=0
[PASS]

-----
Random Shift Test
sel=0x8 A=0xebfec0d7 DinL=0 DinR=0 → Expected F=0x75ff606b | Obtained F=0x75ff606b
[PASS]

-----
All functional verification tests completed.
Simulation complete via $finish(1) at time 195 NS + 0
../RTL/tb/tb_alu_32bit_behavioral.v:88      $finish;
xcelium>
```

ALU_32bit_Modular_VS_Behavioral



```

xcelium>
xcelium> # Run the simulation for 100 ns
xcelium> run 500 ns

===== Modular vs Behavioral 32-bit ALU Comparison =====

-- Arithmetic Operation Tests --
----- Transfer A -----
sel=0x0 A=0x00000000 (0) B=0x00000000 (0) Cin=0 DinL=0 DinR=0
Modular → F=0x00000000 (0) Cout=0
Behavioral→ F=0x00000000 (0) Cout=0
[PASS] Arithmetic Match
-----

----- Increment A -----
sel=0x0 A=0xffffffff (4294967295) B=0x00000000 (0) Cin=1 DinL=0 DinR=0
Modular → F=0x00000000 (0) Cout=1
Behavioral→ F=0x00000000 (0) Cout=1
[PASS] Arithmetic Match
-----

----- Addition A+B -----
sel=0x1 A=0xffffffff (4294967295) B=0xffffffff (4294967295) Cin=0 DinL=0 DinR=0
Modular → F=0xfffffff (4294967294) Cout=1
Behavioral→ F=0xfffffff (4294967294) Cout=1
[PASS] Arithmetic Match
-----

----- Addition A+B+1 -----
sel=0x1 A=0x00000001 (1) B=0x00000001 (1) Cin=1 DinL=0 DinR=0
Modular → F=0x00000003 (3) Cout=0
Behavioral→ F=0x00000003 (3) Cout=0
[PASS] Arithmetic Match
-----

----- Subtraction A-B-1 -----
sel=0x2 A=0x00000004 (4) B=0x00000003 (3) Cin=0 DinL=0 DinR=0
Modular → F=0x00000000 (0) Cout=1
Behavioral→ F=0x00000000 (0) Cout=1
[PASS] Arithmetic Match
-----

----- Subtraction A-B -----
sel=0x2 A=0x00000004 (4) B=0x00000003 (3) Cin=1 DinL=0 DinR=0
Modular → F=0x00000001 (1) Cout=1
Behavioral→ F=0x00000001 (1) Cout=1
[PASS] Arithmetic Match
-----

----- Subtraction A-B-1 (B>A) -----
sel=0x2 A=0x00000003 (3) B=0x00000004 (4) Cin=0 DinL=0 DinR=0
Modular → F=0xfffffff (4294967294) Cout=0
Behavioral→ F=0xfffffff (4294967294) Cout=0
[PASS] Arithmetic Match
-----
```

```

-----  

      Subtraction A-B (B>A)  

sel=0x2 A=0x00000003 (3) B=0x00000004 (4) Cin=1 DinL=0 DinR=0  

Modular   → F=0xffffffff (4294967295) Cout=0  

Behavioral→ F=0xffffffff (4294967295) Cout=0  

[PASS] Arithmetic Match  

-----  

-----  

      Decrement A (underflow)  

sel=0x3 A=0x00000000 (0) B=0x00000004 (4) Cin=0 DinL=0 DinR=0  

Modular   → F=0xffffffff (4294967295) Cout=0  

Behavioral→ F=0xffffffff (4294967295) Cout=0  

[PASS] Arithmetic Match  

-----  

-----  

      Decrement A  

sel=0x3 A=0x00000001 (1) B=0x00000004 (4) Cin=0 DinL=0 DinR=0  

Modular   → F=0x00000000 (0) Cout=1  

Behavioral→ F=0x00000000 (0) Cout=1  

[PASS] Arithmetic Match  

-----  

-----  

      Transfer A (sel=3, Cin=1)  

sel=0x3 A=0xffffffff (4294967295) B=0x00000004 (4) Cin=1 DinL=0 DinR=0  

Modular   → F=0xffffffff (4294967295) Cout=1  

Behavioral→ F=0xffffffff (4294967295) Cout=1  

[PASS] Arithmetic Match  

-----  

-----  

      Addition Overflow Case  

sel=0x1 A=0x80000000 (2147483648) B=0x7fffffff (2147483647) Cin=0 DinL=0 DinR=0  

Modular   → F=0xffffffff (4294967295) Cout=0  

Behavioral→ F=0xffffffff (4294967295) Cout=0  

[PASS] Arithmetic Match  

-----  

--- Logic Operation Tests ---  

-----  

      AND Operation  

sel=0x4 A=0xf0f0f0f0 (252645135) B=0xf0f0f0f0 (4042322160) Cin=0 DinL=0 DinR=0  

Modular   → F=0x00000000 (0)  

Behavioral→ F=0x00000000 (0)  

[PASS] Logic/Shift Match (Cout ignored)  

-----  

-----  

      OR Operation  

sel=0x5 A=0xf0f0f0f0 (252645135) B=0xf0f0f0f0 (4042322160) Cin=0 DinL=0 DinR=0  

Modular   → F=0xffffffff (4294967295)  

Behavioral→ F=0xffffffff (4294967295)  

[PASS] Logic/Shift Match (Cout ignored)  

-----  

-----  

      XOR Operation  

sel=0x6 A=0aaaaaaaa (2863311530) B=0x55555555 (1431655765) Cin=0 DinL=0 DinR=0  

Modular   → F=0xffffffff (4294967295)  

Behavioral→ F=0xffffffff (4294967295)  

[PASS] Logic/Shift Match (Cout ignored)
-----
```

```
-----  
NOT A Operation  
sel=0x7 A=0x00000000 (0) B=0x00000000 (0) Cin=0 DinL=0 DinR=0  
Modular → F=0xffffffff (4294967295)  
Behavioral→ F=0xffffffff (4294967295)  
[PASS] Logic/Shift Match (Cout ignored)  
-----  
  
--- Shift Operation Tests ---  
-----  
Shift Right  
sel=0x8 A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=0  
Modular → F=0x091a2b3c (152709948)  
Behavioral→ F=0x091a2b3c (152709948)  
[PASS] Logic/Shift Match (Cout ignored)  
-----  
  
Shift Right (sel=10xx)  
sel=0xa A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=0  
Modular → F=0x091a2b3c (152709948)  
Behavioral→ F=0x091a2b3c (152709948)  
[PASS] Logic/Shift Match (Cout ignored)  
-----  
  
Shift Left  
sel=0xc A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=0  
Modular → F=0x2468acf0 (610839792)  
Behavioral→ F=0x2468acf0 (610839792)  
[PASS] Logic/Shift Match (Cout ignored)  
-----
```

```
-----  
      Shift Left (sel=11xx)  
sel=0xd A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=0  
Modular  → F=0x2468acf0 (610839792)  
Behavioral→ F=0x2468acf0 (610839792)  
[PASS] Logic/Shift Match (Cout ignored)  
-----  
  
-----  
      Shift Right  
sel=0x8 A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=1  
Modular  → F=0x891a2b3c (2300193596)  
Behavioral→ F=0x891a2b3c (2300193596)  
[PASS] Logic/Shift Match (Cout ignored)  
-----  
  
-----  
      Shift Right (sel=10xx)  
sel=0xa A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=1  
Modular  → F=0x891a2b3c (2300193596)  
Behavioral→ F=0x891a2b3c (2300193596)  
[PASS] Logic/Shift Match (Cout ignored)  
-----  
  
-----  
      Shift Left  
sel=0xc A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=0 DinR=1  
Modular  → F=0x2468acf0 (610839792)  
Behavioral→ F=0x2468acf0 (610839792)  
[PASS] Logic/Shift Match (Cout ignored)  
-----  
  
-----  
      Shift Left (sel=11xx)  
sel=0xd A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=0  
Modular  → F=0x2468acf1 (610839793)  
Behavioral→ F=0x2468acf1 (610839793)  
[PASS] Logic/Shift Match (Cout ignored)  
-----  
  
-----  
      Shift Right  
sel=0x8 A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=1  
Modular  → F=0x891a2b3c (2300193596)  
Behavioral→ F=0x891a2b3c (2300193596)  
[PASS] Logic/Shift Match (Cout ignored)  
-----  
  
-----  
      Shift Right (sel=10xx)  
sel=0xa A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=1  
Modular  → F=0x891a2b3c (2300193596)  
Behavioral→ F=0x891a2b3c (2300193596)  
[PASS] Logic/Shift Match (Cout ignored)  
-----  
  
-----  
      Shift Left  
sel=0xc A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=1  
Modular  → F=0x2468acf1 (610839793)  
Behavioral→ F=0x2468acf1 (610839793)  
[PASS] Logic/Shift Match (Cout ignored)
```

```
-----  
Shift Left (sel=11xx)  
sel=0xd A=0x12345678 (305419896) B=0x00000000 (0) Cin=0 DinL=1 DinR=1  
Modular → F=0x2468acf1 (610839793)  
Behavioral→ F=0x2468acf1 (610839793)  
[PASS] Logic/Shift Match (Cout ignored)  
-----  
  
All functional verification tests completed.  
  
Simulation complete via $finish(1) at time 160 NS + 0  
../RTL/tb/tb_modular_VS_behavioral.v:95      $finish;  
xcelium>
```