Digital VLSI - EECS4612
Project 2: Post-Layout simulation of a Complex Logic Gate

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Project Description

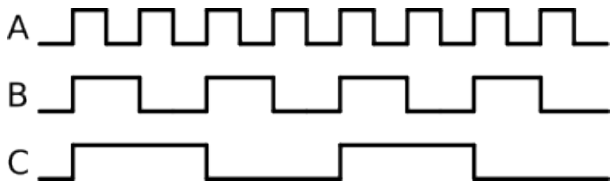
1. ***Schematic Design:***
   - Design the schematic for $F = \overline{C + A \cdot B}$ using Cadence Virtuoso.
   - Use the following transistor sizing:
     - $L = L_{\text{min}}$, $W_p = 200\,\text{nm}$, $W_n = 150\,\text{nm}$.
   - Create a ***symbol*** for the designed schematic.
   - **Note:** For the schematic of this logic function, you can refer to your course slides.

2. ***Layout Design:***
   - Create a compact layout for the circuit in Cadence Virtuoso Layout Editor.
   - You are allowed to use ***P-Cells***, but employ abutment techniques (merging shared diffusion regions between transistors) to optimize the area.
   - Only ***Poly*** and ***Metal 1*** interconnects are allowed. No other metal layers can be used.
   - You must draw a layout similar to what you learned in class, with PMOS transistors placed at the top and NMOS transistors placed at the bottom, following standard CMOS layout conventions.
   - Ensure the layout passes both Design Rule Check (***DRC***) and Layout vs. Schematic (***LVS***) validations.

3. ***Parasitic Extraction:***
   - Extract the layout in two configurations to analyze the effect of parasitics on circuit performance:
     - ***Without Parasitic Elements***: Perform a layout extraction that includes only the geometric and connectivity information of the layout, excluding parasitic resistances and capacitances.
     - ***With Parasitic Elements***: Perform a full layout extraction that includes parasitic resistances and capacitances, which model the physical effects of interconnects and diffusion regions.

4. Testbench Design:

- Create a separate schematic for the testbench and name it `yourDesignName_tb`. Instantiate the logic circuit three times (We want to simulate designed gate in 3 different configuration). Place a `vdc` instance from the `analogLib` library and connect the **VDD** pins of all instances to a 1.1V DC supply and the **GND** pins to Ground, respectively. Ensure proper connections to all instances.
- Use the `vsource` instance from the `analogLib` library to apply the input signals A, B, and C. The input signals should be follow:



- Assign appropriate input signals and connect a **50 fF load capacitance** to the output of each instance. Use the **Label** feature (`L` shortcut in Virtuoso Schematic Editor) to assign clear and meaningful net names to each output, such as:
  - `F_Schematic` for the schematic view instance.
  - `F_Extract` for the extracted view without parasitic elements.
  - `F_RcExtract` for the extracted view with parasitic elements.
- Create a **Config View** (as described in the Layout Extraction Tutorial) for the testbench and set the view of the instances as follows:
  1. **Schematic View**.
  2. **Extracted View Without Parasitic Elements**.
  3. **Extracted View With Parasitic Elements**.

5. *Post-Layout Simulation:*

- Simulate the transient response for the testbench config view and compare the results for the three instances.
- Measure and report:
  - Rise time (t_{LH}) and fall time (t_{HL}).
  - Maximum propagation delay (t_{max}).
  - Power dissipation (P_{diss}).
  - Peak current (I_{peak}).
- Calculate the ***maximum operating frequency*** of the circuit.
- **Note:** For the definitions of rise time, fall time, and propagation delay, refer to your course slides.
- Explain how parasitic elements (resistance and capacitance) impact the circuit's performance, particularly the rise time, fall time, propagation delay, and maximum operating frequency.

Deliverables:

- A short report in PDF format that includes:
  - A picture of your schematic.
  - A picture of your layout.
  - DRC and LVS results.
  - Simulation waveforms (input and output signals) for all three configuration views (Schematic, Extracted without parasitics, and Extracted with parasitics).
- Cadence design files.

Submission Guidelines

1. Create a single ZIP archive containing all the required deliverables.

2. Name the ZIP file using the following convention:
`P2_FirstName_StudentID.zip` (e.g., `P2_Donald_1234567.zip`).

3. Submit the ZIP file through the eClass portal by the deadline: ***February 09, 2025, 23:59 (EST)***.

Important Note: No submissions will be accepted through email.

Grading Criteria (out of 10)

Your project will be evaluated based on the following criteria:

- ***Schematic Design:*** Correct implementation of the schematic, proper transistor sizing, and creation of the symbol *(2 out of 10)*.
- ***Layout Design:*** Compact layout with proper abutment techniques, adherence to design rules, and successful DRC/LVS compliance *(3 out of 10)*.
- ***Simulation Accuracy:*** Accurate transient simulation results for all three configuration views (Schematic, Extracted without parasitics, Extracted with parasitics) and correct comparison of results *(3 out of 10)*.
- ***Report Quality:*** Thoroughness, clarity, and inclusion of all required items (schematic, layout, DRC/LVS results, simulation waveforms, and parasitic impact analysis) *(2 out of 10)*.

Resources

- Lecture notes and slides.
- Lab sessions.
- EDA tool tutorials (there are plenty of videos available on YouTube).
- Design rule manuals for the selected technology.

Important Notes

- ***Late Submissions:*** The submission deadline is final, and no submissions will be accepted after the deadline.
- ***Academic Integrity:*** Collaboration in understanding concepts is encouraged; however, each student must independently design and create their own schematics and layouts. Plagiarism will result in a failing grade for the project.
- ***Seek Help:*** If you need clarification or assistance, feel free to contact the TA or instructor during office hours or via email.