Digital VLSI - EECS4612/5612
Project 3: RTL-to-GDSII Flow for a 16×24-Bit Multiplier

Instructor: Dr. Amir M. Sodagar
TA: Mohsen Namavar

Winter 2025

Objective

The goal of this project is to introduce students to the **ASIC design flow** by implementing a **16×24-Bit Multiplier** from **RTL to GDSII**. The primary focus is on the **back-end design process**, including **logic synthesis, place and route (PnR), and verification**.

Students will:

- Simulate a 16×24-Bit Multiplier using Cadence Xcelium.
- Synthesize the design using Cadence Genus.
- Perform Place and Route (PnR) using Cadence Innovus.
- Generate and analyze reports from the synthesis and PnR processes, including timing, power, and area.

Project Description

1. **HDL Design and Functional Simulation:**
   - As the primary focus of this project is the RTL-to-GDSII flow rather than HDL design, the HDL code and its testbench will be provided (you can download it through e-Class). However, it is strongly recommended that you attempt to write your own Verilog code based on the specifications below to enhance your understanding.
   - The design consists of an unsigned 16×24-Bit multiplier with a 1-stage pipeline for the inputs and a 3-stage pipeline for the output to improve timing performance.
2. **Logic Synthesis:**
   - Synthesize the HDL code using Cadence Genus.
   - Generate and report:
     - Gate-Level Netlist
     - Timing Report
     - Power Report
     - Area Utilization Report
3. **Place and Route (PnR):**
   - Import the synthesized netlist into Cadence Innovus.
   - Perform:
     - Floorplanning.
     - Placement
     - Clock Tree Synthesis (CTS)
     - Routing
     - Add fillers
   - Generate the final GDSII layout.
   - Import the generated layout into Cadence Virtuoso for post-layout analysis.

Deliverables

Each student must submit the following files in a single ZIP archive:

- Report (PDF format) including:
  - Simulation results (waveforms of inputs, outputs, and pipeline stages)
  - Synthesis reports: gate-level netlist, timing, power, and area analysis
  - PnR reports: placement, routing, and final layout
  - Screenshots of the layout in virtuoso
- Cadence Design Files, including:
  - Synthesized netlist and constraints
  - Layout files from Cadence Innovus

Submission Instructions

- Name your ZIP file as: `P3_FirstName_StudentID.zip` (e.g., `P3_John_1234567.zip`).
- Upload the ZIP file to the eClass portal before the deadline.
- Late submissions will not be accepted.

Grading Criteria (out of 10)

- Functional Simulation: Correct behavior of the multiplier and verification through waveforms (2 points)
- Synthesis and Reports: Proper constraints, timing optimization, and synthesis report submission (2 points)
- PnR and GDSII Layout: Floorplanning, placement, CTS, routing, and report generation (4 points)
- Report Quality: Clarity, completeness, and detailed documentation of steps taken (2 point)