Project 1
NAND Gate Project

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Course: EECS4612
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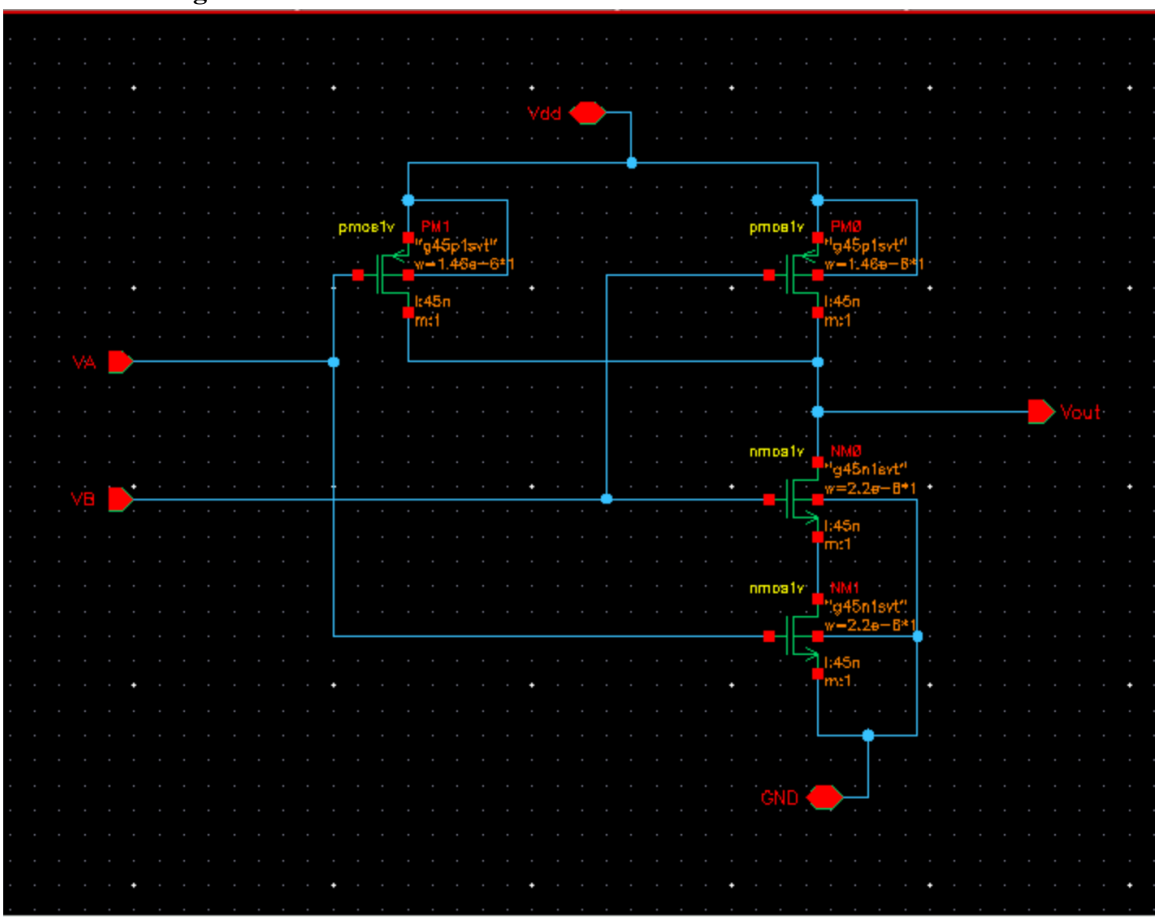
Objective

The goal of this project was to design a 2-input NAND gate in **Cadence Virtuoso**, ensuring equal rise and fall times (both under **0.5 ns**) at the output, create the corresponding layout, and verify functionality through DRC and LVS checks.

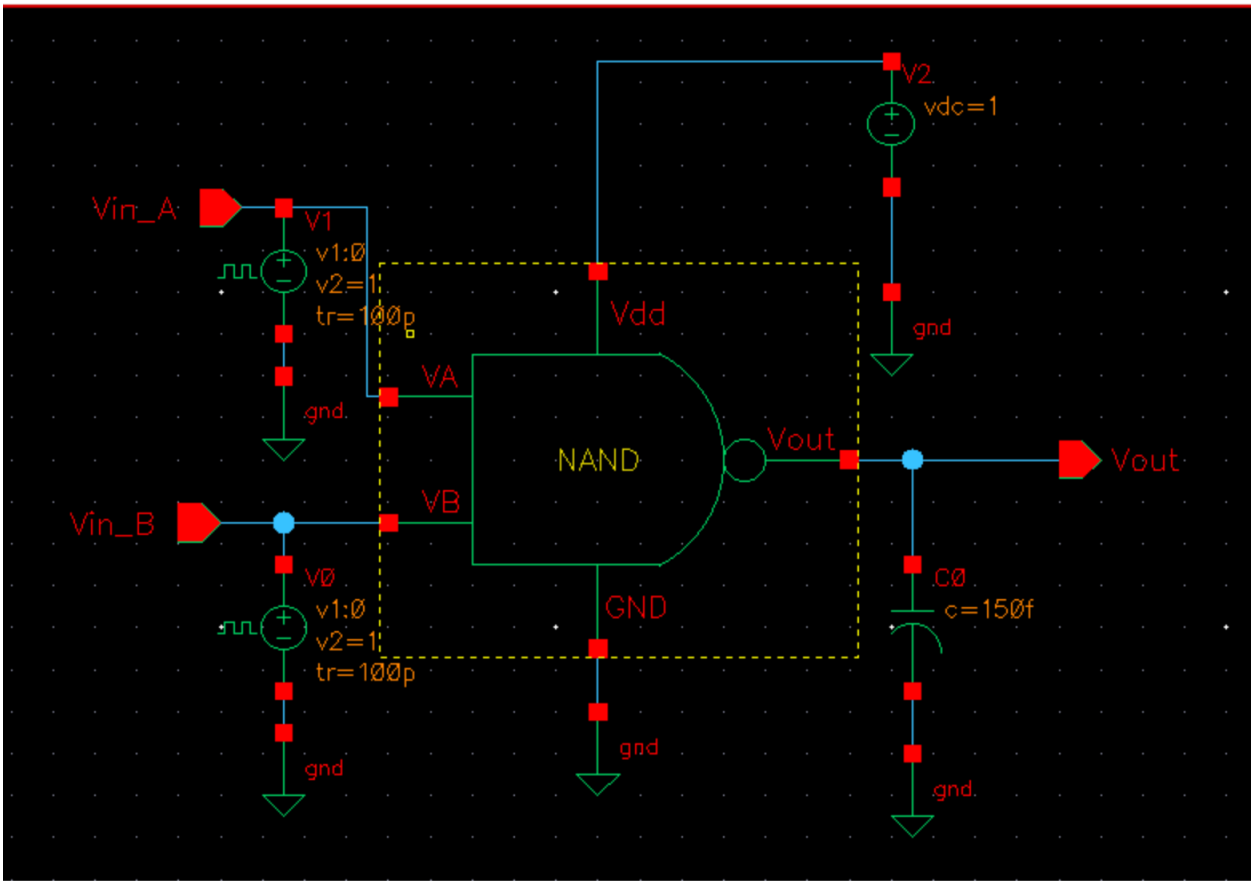
Work Summary:

1. **Schematic Design**:
   - A schematic of the 2-input NAND gate was created using the Virtuoso Schematic Editor.
   - A 150 fF load capacitor was connected at the output to simulate realistic load conditions.
   - Transistor sizes (W/L) were optimized to achieve rise and fall times of 458.592 ps and 454.85 ps, respectively, ensuring compliance with the design specifications.
   - The following is pictures of the schematic and symbol designs:

Schematic Design:



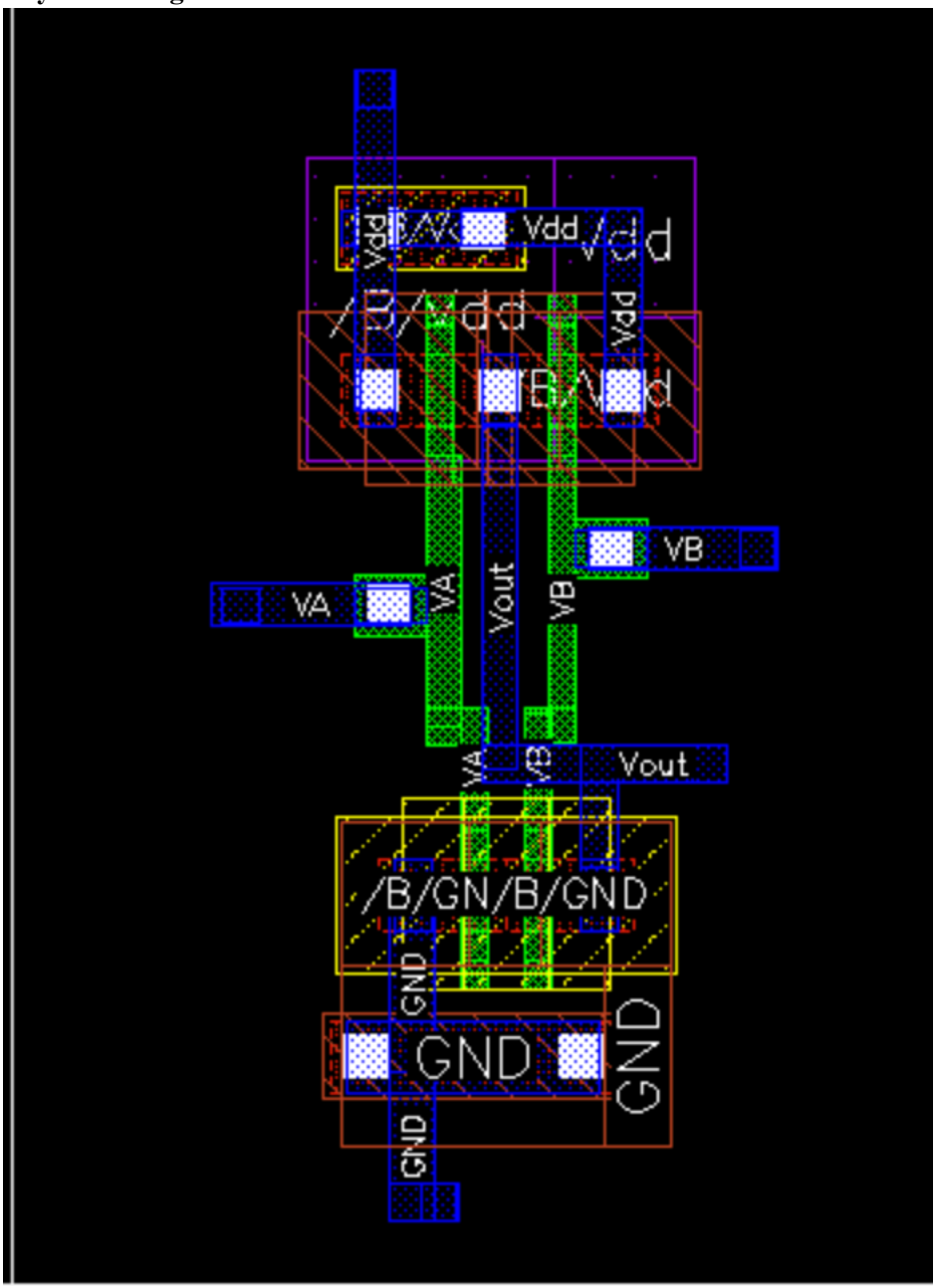
Symbol Design:



2. **Layout Design**:

- The layout of the NAND gate was created in Virtuoso Layout Editor, adhering to the provided design rules.
- Efficient use of layout area and clean routing practices were followed.
- Below is a picture of the layout design:

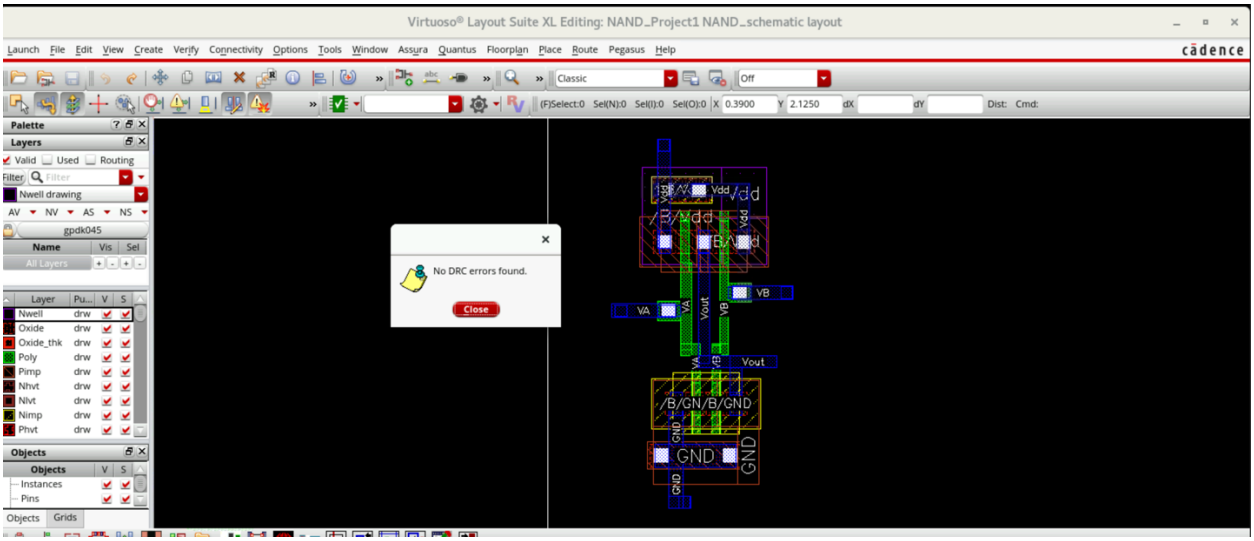
Layout Desing:



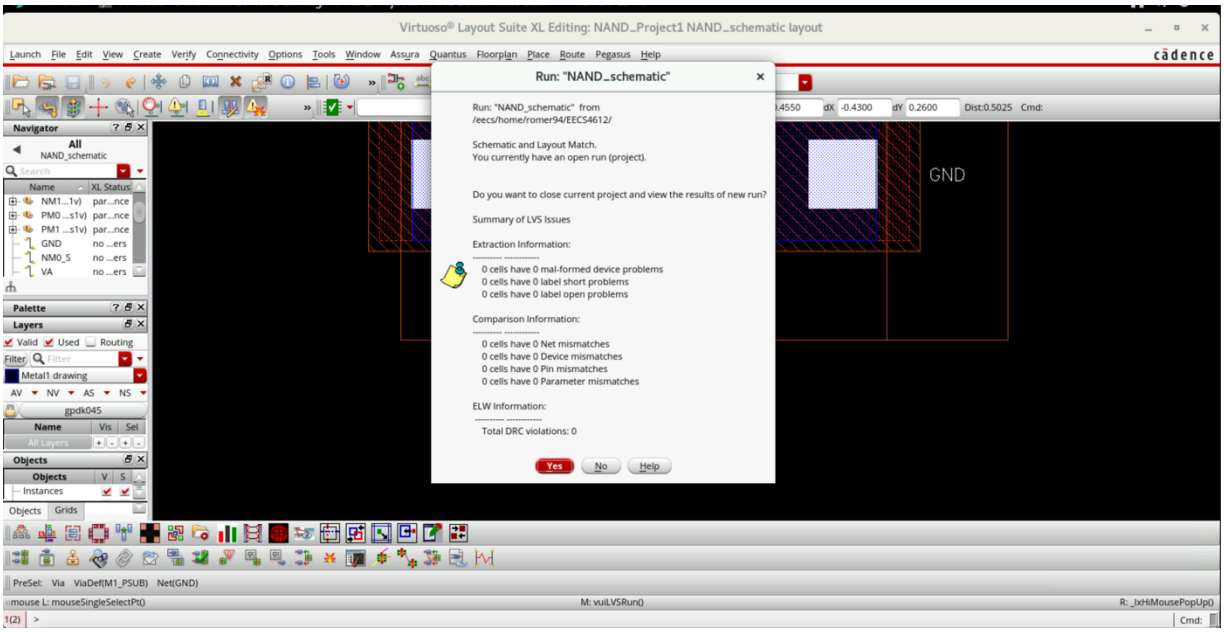
3. **Verification**:

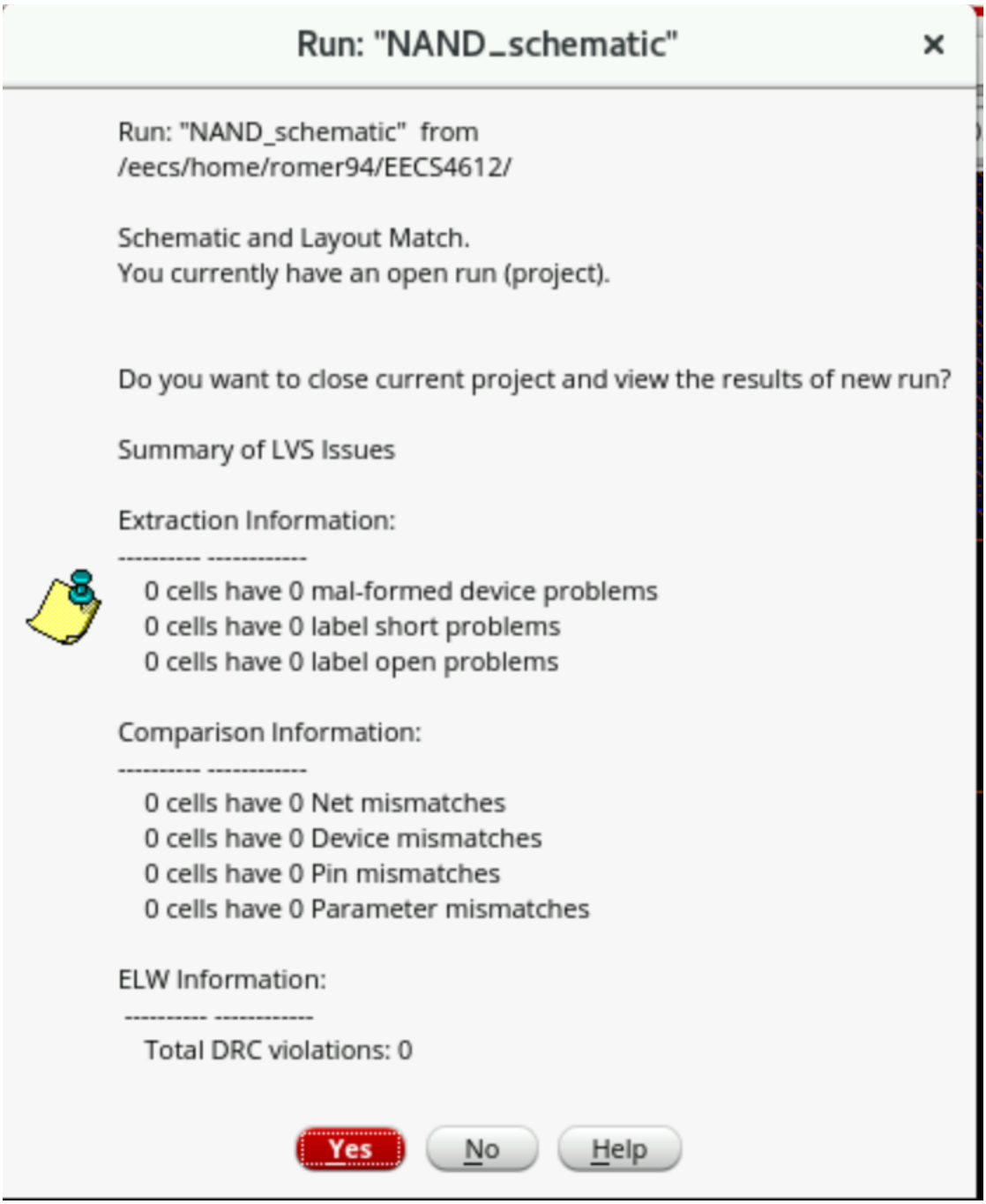
- The design successfully passed the Design Rule Check (DRC), confirming adherence to layout constraints.
- The design also passed the Layout vs. Schematic (LVS) verification, ensuring that the layout matched the schematic.
- The following is a list of pictures showing the results of the DRC and LVS tests:

DRC Result:



LVS Result:




Run: "NAND_schematic"
Run: "NAND_schematic" from
/eecs/home/romer94/EECS4612/
Schematic and Layout Match.
You currently have an open run (project).
Do you want to close current project and view the results of new run?
Summary of LVS Issues
Extraction Information:
---------- ----------
0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems
Comparison Information:
---------- ----------
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches
ELW Information:
---------- ----------
Total DRC violations: 0
Yes
No
Help

Results

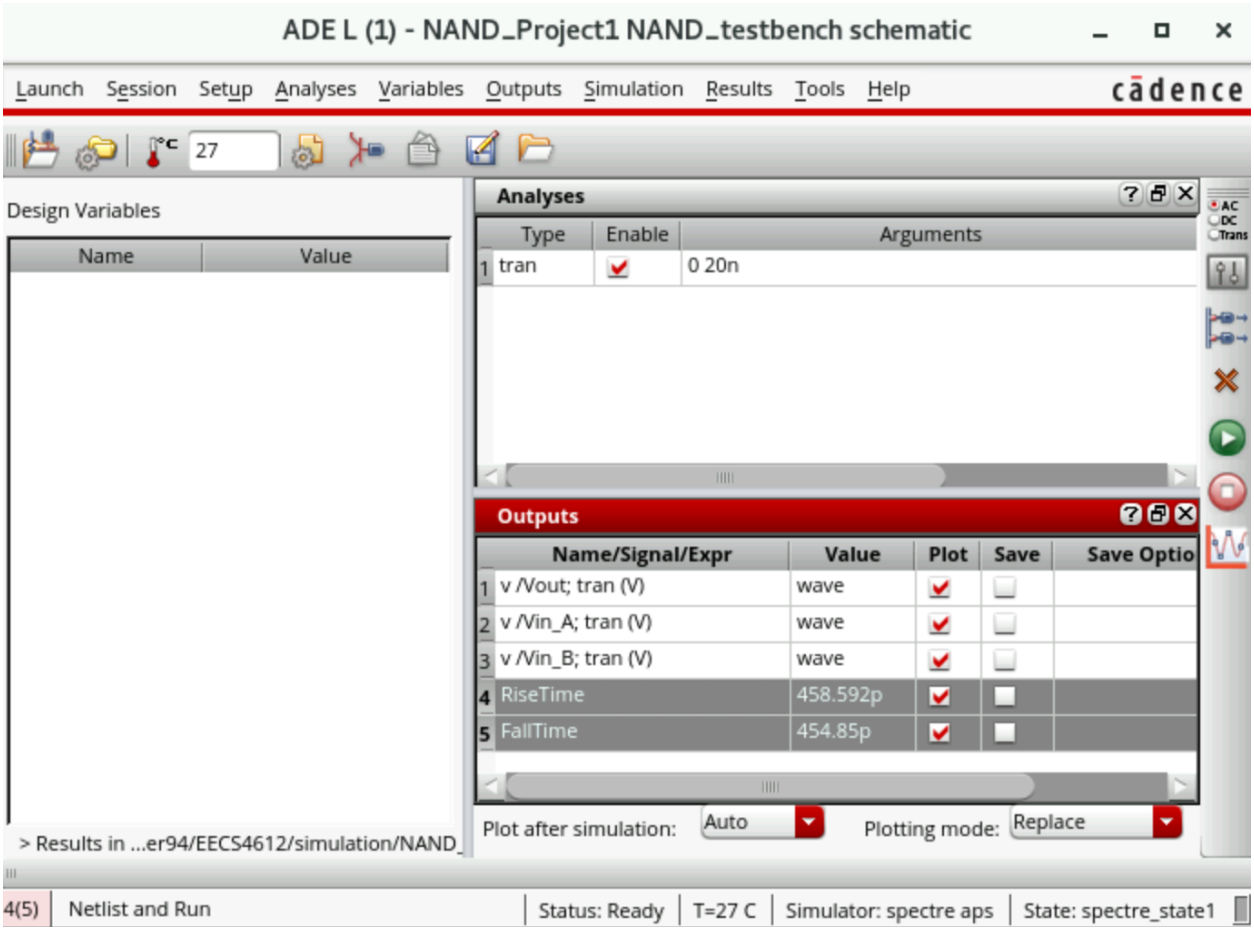
- The NAND gate meets the requirements of the project, with equal rise and fall times less than 0.5 ns.
- Both DRC and LVS checks were successful, as shown in the screenshots attached earlier.
- Below are screenshots of the plot showing the output of the NAND gate vs the input Vin_A and Vin_B and another screenshot showing the rise time and fall time calculated in the ADE window:

Vout vs Vin_A and Vin_B Plot:

The output waveform confirms the truth table of a NAND gate.

A	B	NAND
0	**0**	**1**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

Rise Time and Fall Time Claculated:



The rise time and the fall time are equal (0.45 ns) and they are both below 0.5ns.