Digital VLSI - EECS4612
Project 1: Schematic and Layout Design of a 2-input NAND Gate

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Objective

The purpose of the first project is to become familiar with IC design toolsets (e.g., Cadence Virtuoso Suite). During the first lab session, students will learn how to use these tools to create the schematic and layout of a simple primitive cell. Additionally, students will simulate the cell to analyze its DC and transient response.

Project Description

1. **Schematic Design:**
   Design a 2-input NAND gate schematic using the Cadence Virtuoso Schematic Editor. Connect a 150 fF load capacitor to the output of the gate. Adjust the (W/L) ratios of NMOS and PMOS transistors to ensure equal rise and fall times, both of which should be less than 0.5 ns.
   Recommended starting point: Begin with a W/L ratio of 5 for both PMOS and NMOS transistors. Adjust these values as needed based on simulation results and the specific technology process.
   No manual calculations for rise and fall times are required.

2. **Layout Design:**
   - Remove the load capacitor and create the layout of the NAND2 gate. you can use P-cells in your layout, but it will be a good practice to try draw layout from scratch.
   - Adhere to all design rules specified for the chosen technology.

3. **Verification:**
   - Ensure the layout passes both DRC and LVS.

4. **Deliverables:**
   - A short report include a picture of your schematic, simulation waveforms (input signal, output signal), layout and DRC/LVS results (report format should be PDF)
   - Cadence design files

Submission Guidelines

1. Create a single ZIP archive containing all the required deliverables.

2. Name the ZIP file using the following convention:
`P1_FirstName_StudentID.zip` (e.g., `P1_Donald_1234567.zip`).

3. Submit the ZIP file through the eClass portal by the deadline: **January 26, 2025, 23:59 (EST)**.

Important Note: No submissions will be accepted through email.

Grading Criteria (out of 5)

Your project will be evaluated based on the following criteria:

- **Functionality:** Correct operation of the schematic and compliance with the requirements (equal rise and fall times, both less than 0.5 ns) *(2 out of 5)*.
- **DRC/LVS Compliance:** Successful completion of Design Rule Check (DRC) and Layout vs. Schematic (LVS) checks *(1 out of 5)*.
- **Layout Quality:** Efficient use of area, clean routing, and adherence to best layout practices *(1.5 out of 5)*.
- **Report Quality:** Thoroughness, clarity, and organization of the report *(0.5 out of 5)*.

Resources

- Lecture notes and slides.
- Lab sessions.
- EDA tool tutorials (there are plenty of videos available on YouTube).
- Design rule manuals for the selected technology.

Important Notes

- **Late Submissions:** The submission deadline is final, and no submissions will be accepted after the deadline.
- **Academic Integrity:** Collaboration in understanding concepts is encouraged; however, each student must independently design and create their own schematics and layouts. Plagiarism will result in a failing grade for the project.
- **Seek Help:** If you need clarification or assistance, feel free to contact the TA or instructor during office hours or via email.