Title: CMOS Implementation of $F = \overline{C + A \cdot B}$

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Course: EECS4612

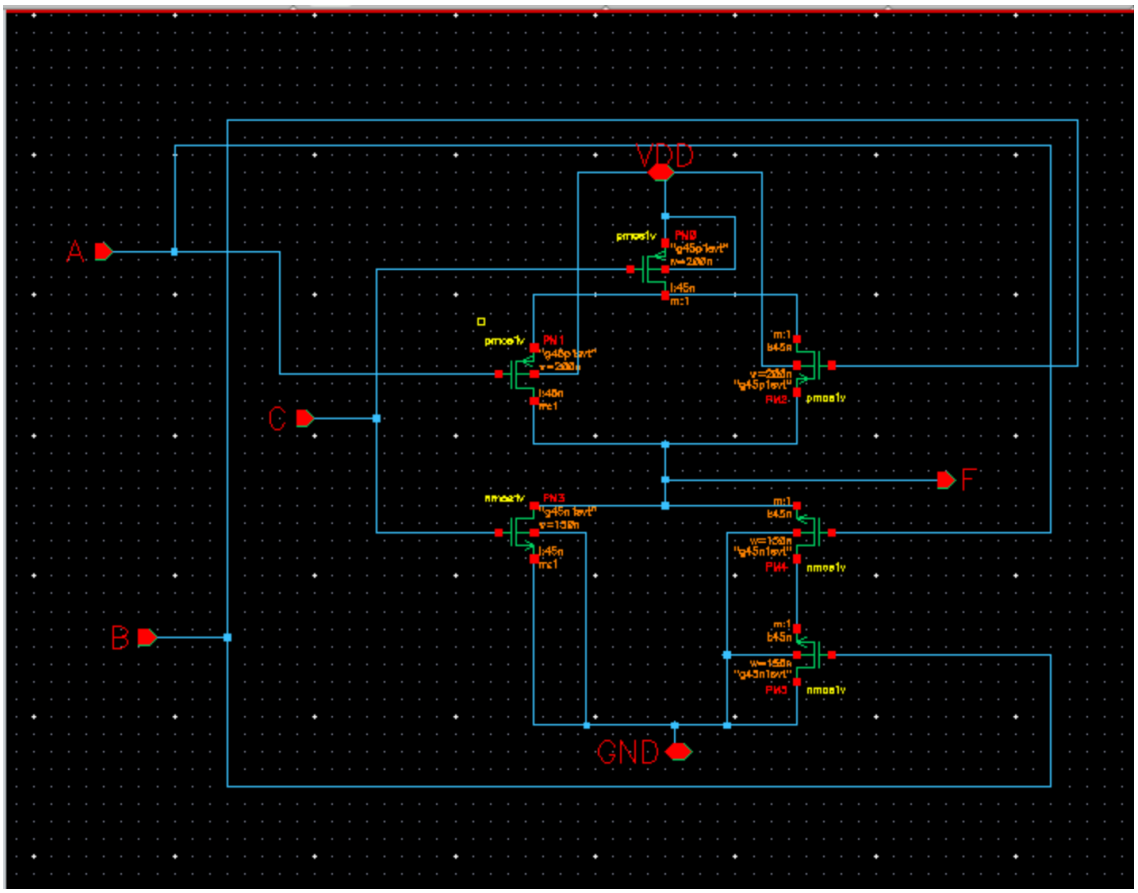
PROJECT 2

Objective:
This report presents the design, simulation, and verification of a CMOS circuit implementing the function:

$$F = \overline{C + A \cdot B}$$

The design is tested across three configurations:
1. Schematic view (ideal behavior, no parasitics)
2. Extracted view without parasitics (post-layout with ideal interconnects)
3. Extracted view with parasitics (real-world behavior including resistance and capacitance effects)

Schematic Design

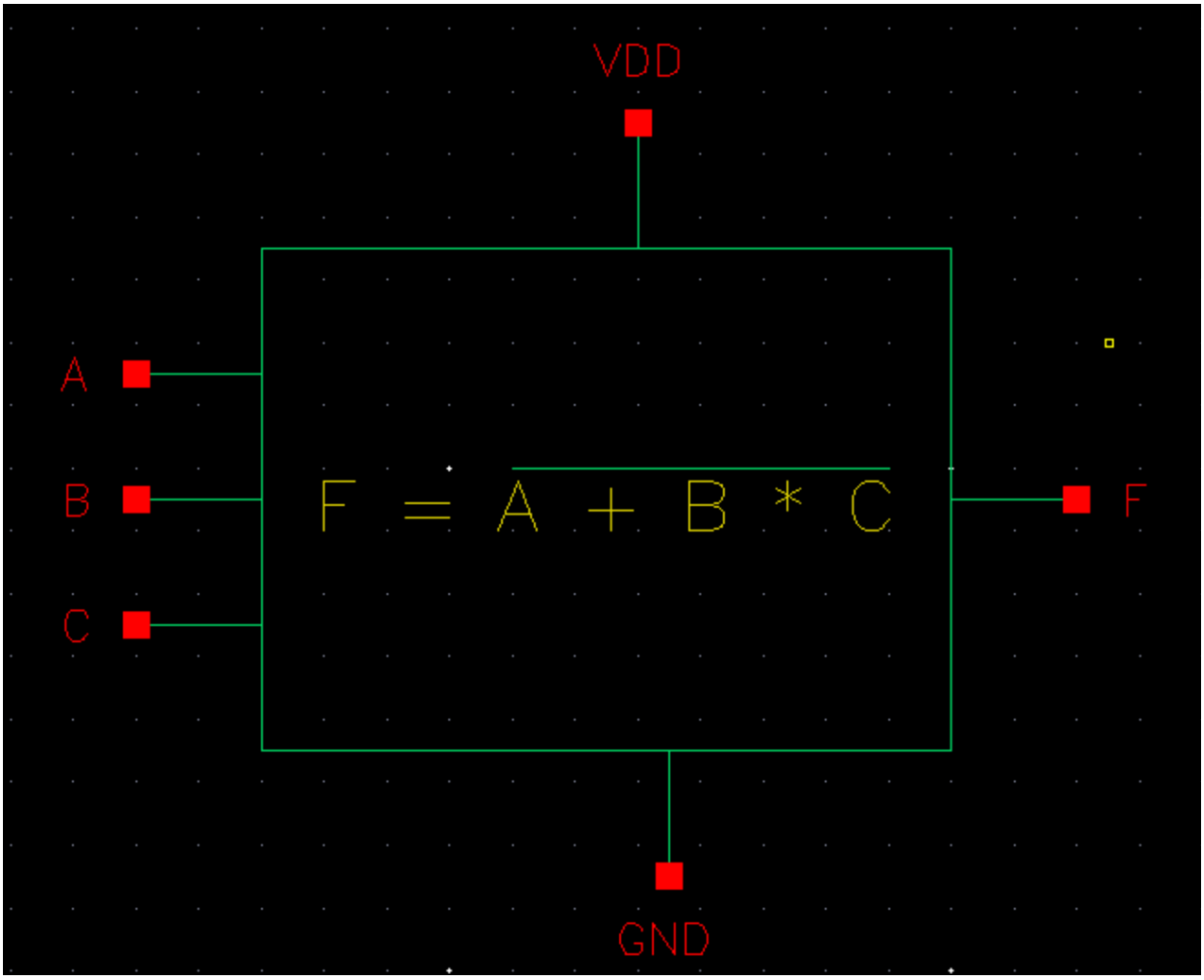


Key Components:

One PMOS transistor in series with two parallel PMOS transistors sit at the top half of the circuit, and two in-series NMOS transistors connected in parallel with a third NMOS transistor sit at the bottom half of the circuit. The two groups are connected at the output point F, and they successfully implement the logic of the function $F = \overline{C + A \cdot B}$.

Power and ground connections are VDD and GND respectively. Input signals are A, B, C and the output signal is F. This is more clearly illustrated in the symbol representation of the above schematic. The

following picture is the symbol view of the schematic:

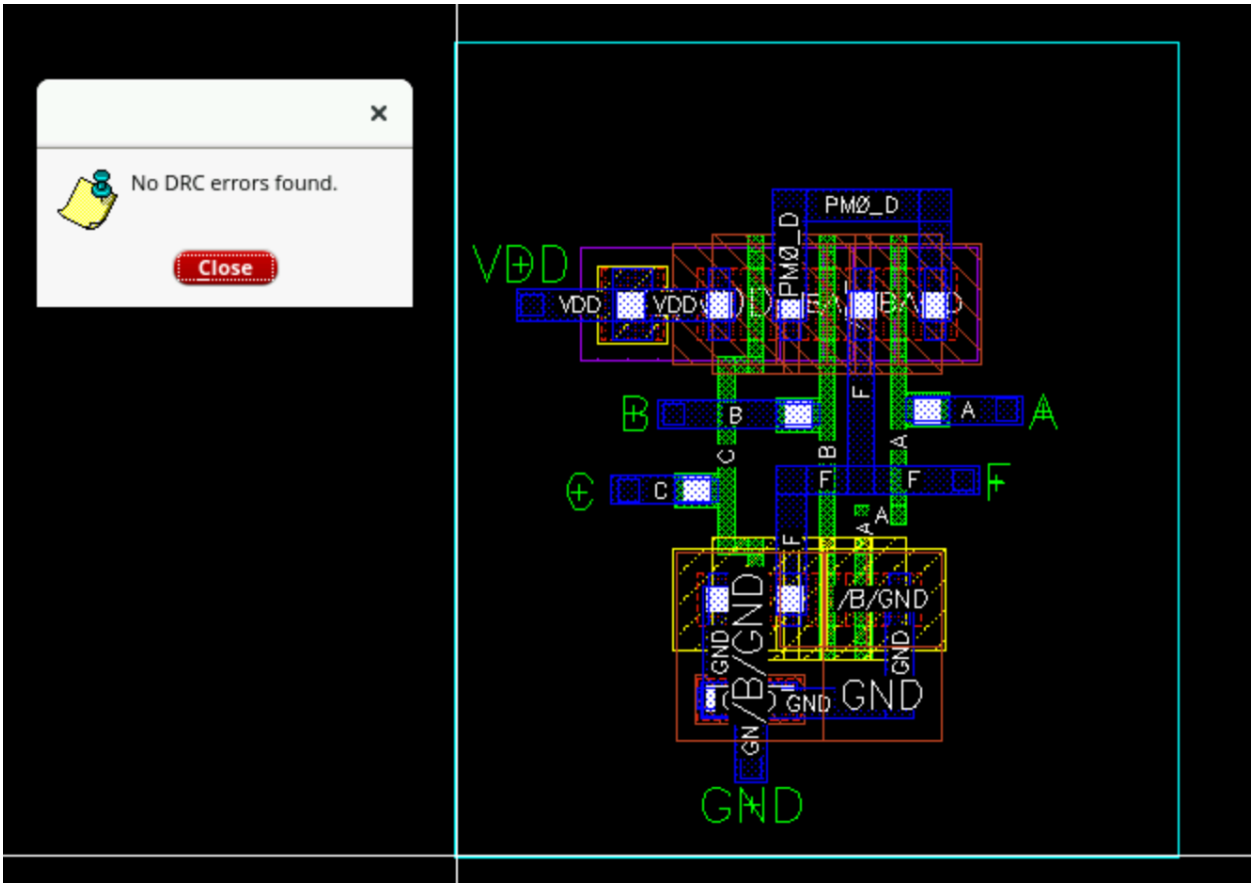


Layout Design, DRC and LVS Verification

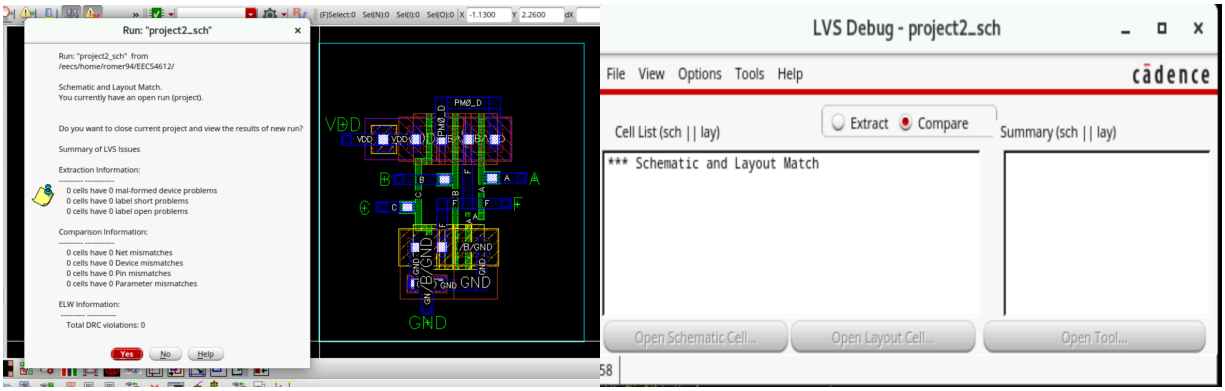
Below is a screenshot of the layout design of the schematic circuit. Note that, I took the following considerations when designing the layout of the circuit:

- PMOS transistors grouped at the top (P-well), NMOS at the bottom (N-well).
- Minimum-length routing used to reduce interconnect resistance.
- Metal, Contacts, Poly and Via layers optimized for signal propagation.

Notice also that the picture of the layout also shows the result of the DRC test, which is a pass.

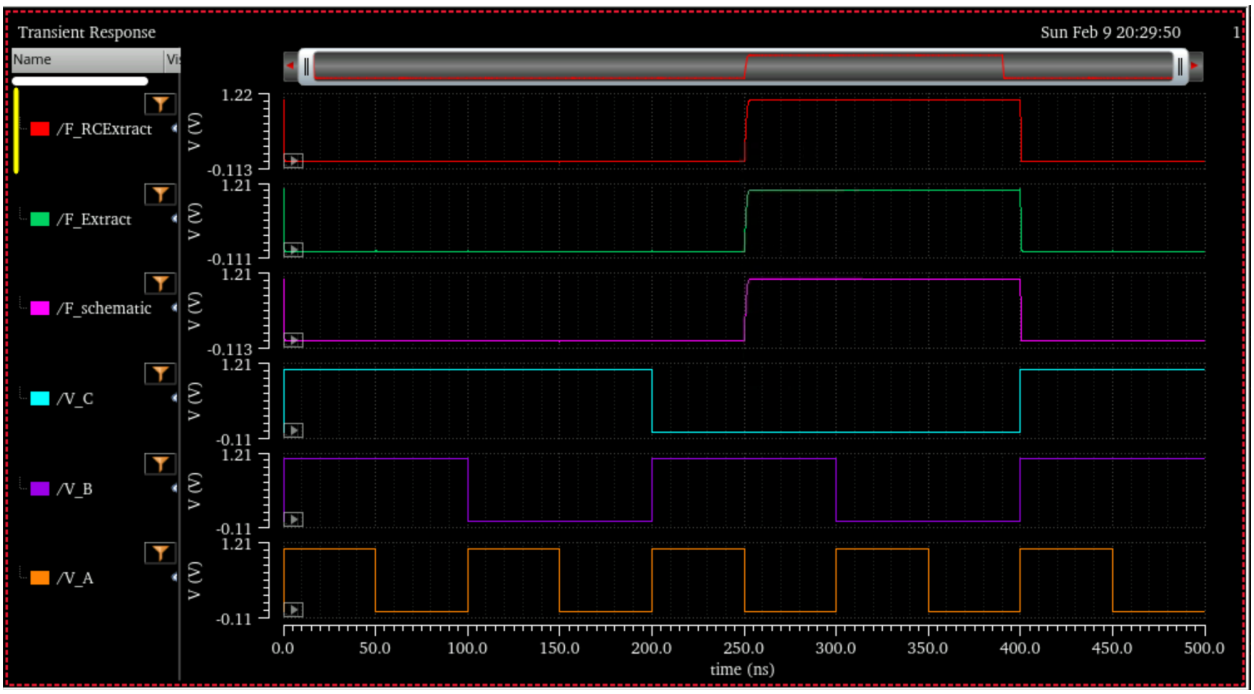


The layout also passed the LVS test as shown in the pictures below:



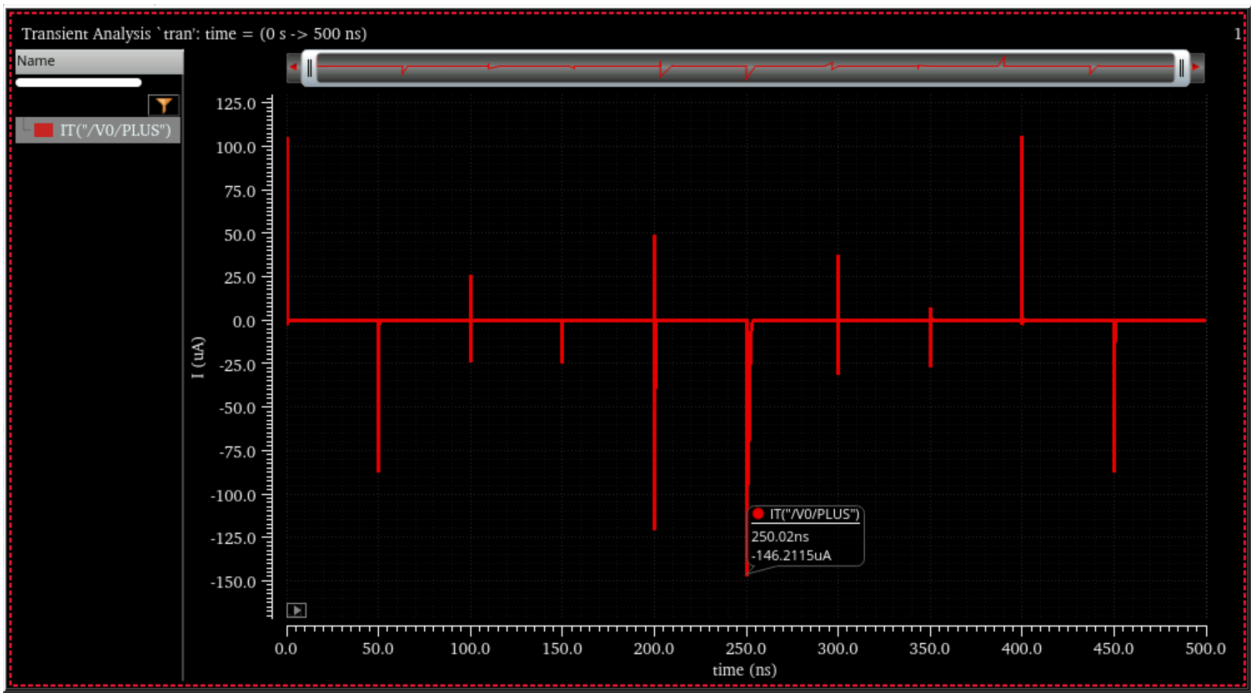
Simulation Results

The following screenshot shows the waveforms for the input signals A, B, and C and the output signal F for three cases: Schematic, Extracted Without parasitics (F_Extracted), and Extracted With Parasitics (F_RCExtracted).



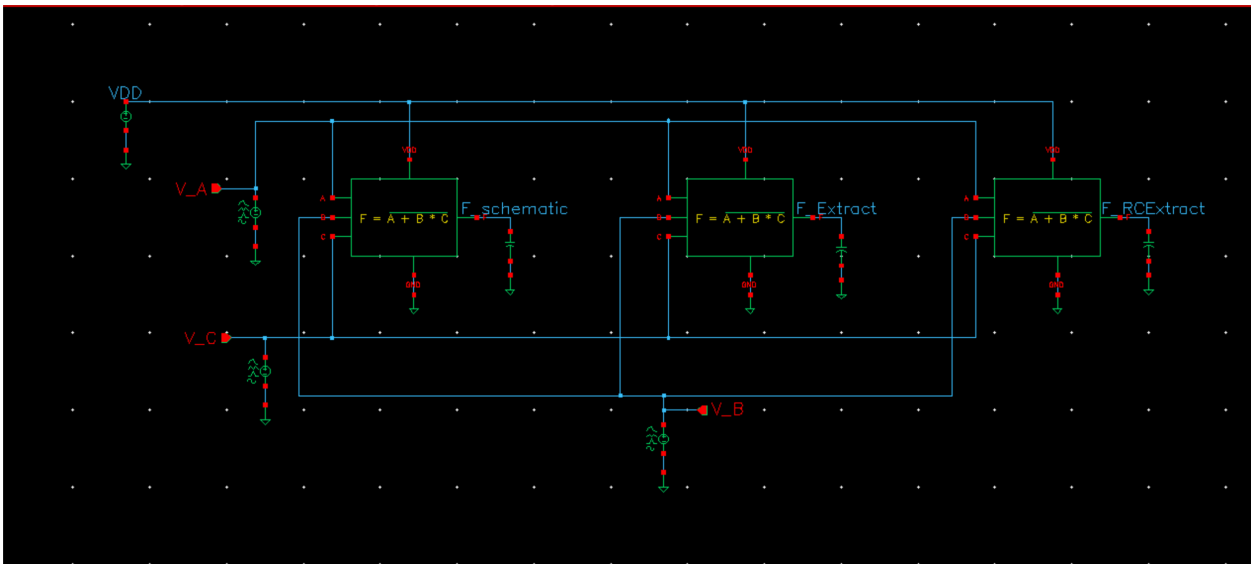
The following is a screenshot that shows the results of my calculations/simulation in ADE L to obtain the values that shows the fall time, rise time, maximum propagation delay, power dissipation and maximum switching frequency for all three cases. I will also include a plot of the current (I_{VDD}) that I used to find the peak current (I_{peak}).

7	Power Dissipation	wave
8	Average Power Dissipated	564.713n
9	FallTime_F_Schematic	374.617p
10	RiseTime_F_Schematic	1.22281n
11	FallTime_F_Extract	355.717p
12	RiseTime_F_Extract	1.28912n
13	FallTime_F_RCExtract	364.564p
14	RiseTime_F_RCExtract	1.31917n
15	F_Schematic propagation delay	-258.119p
16	F_Extract propogation delay	-245.044p
17	F_RCExtract propogation delay	-251.873p
18	Max freq F_schematic	626.007M
19	Max freq F_Extract	607.964M
20	Max freq F_RCExtract	593.919M



I_{peak} = -146.211 micro-Ampere

The following is the a screenshot of the design used to test all three cases:



We can clearly notice from the data that the presence of parasitic capacitance and resistance increases the fall time, rise time and propagation delay when compared with the layout extract without RC effect. These observations can be explained by the fact that the cycle of charging and discharging the parasitic capacitances introduces a delay in the rise time, fall time and propagation delay. This, in turns, slows down the circuit as demonstrated by a slower switching frequency for the cases with RC as compared to the other two cases. Therefore, the presence of parasitic capacitance and resistance is harmful and our goal should be always to try and eliminate or reduce their effect in our circuit design as much as possible.