BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

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Analog Integrated Circuits Laboratory

Final Project Report

Section: G1 Group: 07

Design of an Analog 8:1 Multiplexer

Course Instructors:

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Signature of Instructor: _____

Academic Honesty Statement:

IMPORTANT! Please carefully read and sign the Academic Honesty Statement, below. Type the student ID and name, and put your signature. *You will not receive credit for this project experiment unless this statement is signed in the presence of your lab instructor.*

"In signing this statement, We hereby certify that the work on this project is our own and that we have not copied the work of any other students (past or present), and cited all relevant sources while completing this project. We understand that if we fail to honor this agreement, We will each receive a score of ZERO for this project and be subject to failure of this course."

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1 Abstract

An 8:1 analog multiplexer is an electronic device or integrated circuit (IC) that allows you to select one of eight analog input signals and route it to a single output. Analog multiplexers are indispensable in data acquisition systems, facilitating the seamless switching between various sensors and sources. They also play a pivotal role in medical diagnostics, where analog signals are crucial for selecting different sensor inputs, such as in ECG (Electrocardiogram) machines and blood glucose monitors. Nevertheless, the design of an 8:1 multiplexer presents challenges, notably the complexity associated with a substantial number of wires and the consequential power loss. Recognizing these challenges, our project is dedicated to crafting an efficient 8:1 analog multiplexer that mitigates these issues. Leveraging CMOS transmission gate logic, we've optimized the design by minimizing the transistor count, resulting in enhanced efficiency for applications in communication systems and biomedical fields. The circuit design has been executed and optimized using Cadence Virtuoso IDE.

2 Introduction

In today's era of advanced electronics, the demand for precise, versatile, and efficient signal routing has never been more crucial. Communication systems require seamless frequency switching between channels, necessitating the use of analog multiplexers—often likened to the traffic controllers of electronic circuits. Among these multiplexers, the 8:1 analog variant emerges as a standout, capable of smoothly switching between eight distinct analog input channels to route a chosen signal to a single output.

Nonetheless, the design of an 8:1 analog multiplexer presents unique and multifaceted challenges. These encompass not only the intricacies of signal integrity but also concerns about power consumption, circuit complexity, and overall efficiency. In response to these challenges, our project embarks on a journey to conceive and implement an 8:1 analog multiplexer that excels in minimizing power loss, maximizing efficiency, and optimizing signal fidelity.

Our design approach leverages CMOS transmission gate logic, a bilateral switch that offers versatility in handling input and output. This logic utilizes a control signal to determine the state of the transmission gate. In our implementation, we employ a total of 24 transmission gates, arranged in groups of 3 gates per input line, resulting in 8 lines comprising 24 transmission gates as inputs to the multiplexer. Select pins determine which of these 8 lines is active at any given time. This thoughtfully crafted design minimizes signal loss and ensures exceptional efficiency.

3.1 Problem Formulation (PO(b))

3.1.1 Identification of Scope

In our project, we have pursued a design philosophy focused on simplifying circuit complexity while prioritizing low power consumption, rendering our multiplexer ideal for bio-medical applications and data acquisition systems. A standout feature of our design is its exceptionally low ON resistance, measuring just 10 ohms. This characteristic is of paramount importance,

especially in contexts where signal fidelity and minimal attenuation are non-negotiable, such as in medical instruments and communication systems.

Our choice of CMOS transmission gate logic has been a strategic one. This logic not only affords bidirectional signal flow but also boasts wide voltage compatibility and minimal crosstalk, all of which are invaluable traits in the context of an 8:1 analog multiplexer. Furthermore, we have operated our design with a 3V DC supply voltage, ensuring efficient power management within the transistors.

For our transistor selection, we opted for tsmc18 model transistors. These transistors, characterized by their high threshold voltage and broad voltage swing, have facilitated the creation of a multiplexer design boasting moderate bandwidth and minimal switching time. These attributes are particularly advantageous in communication channels where swift signal switching is a requisite.

3.1.2. Formulation of Problem

Our project centers around the design of an 8:1 analog multiplexer with specific objectives aimed at addressing crucial needs in industrial and biomedical applications. The primary goals we've set are as follows:

Low Power Consumption: We are committed to designing a multiplexer with exceptionally low power consumption, aligning with the stringent energy requirements of both industrial and biomedical devices.

Bidirectional Signal Routing: To enable versatile signal flow in both directions, we've chosen to implement bidirectional signal routing using transmission gate logic. This choice enhances the multiplexer's adaptability in various scenarios.

Operating Signal Range: The multiplexer is designed to accommodate a signal range of 4V peak to peak. This specification ensures compatibility with different analog signal levels commonly encountered in these applications.

Efficient Control Signals: Achieving a robust and efficient method of control signals is paramount to the multiplexer's functionality. To this end, we have employed Pulse signals as our control mechanism.

Minimal ON Resistance: One of our core design objectives is to minimize ON resistance to facilitate efficient signal passage, resulting in minimal voltage drop when the multiplexer is active.

In pursuit of these objectives, our project seeks to provide solutions that not only meet but exceed the demands of industrial and biomedical applications, where precise signal routing, energy efficiency, and robust performance are of utmost importance.

3.1.4. Analysis: A comprehensive analysis of the project includes the advantages and difficulties encountered in designing it. The advantages of this project will be:

Signal Routing: An 8:1 analog multiplexer allows you to select from eight different analog input channels and route a chosen signal to a single output. This capability simplifies complex signal routing tasks.

Space Efficiency: By consolidating multiple input channels into one output, an 8:1 multiplexer reduces the number of required connections and components, saving space on a circuit board.

Cost Savings: Fewer components and simplified routing can lead to cost savings in terms of component procurement, assembly, and circuit board real estate.

Versatility: Multiplexers are versatile components that can be used in various applications, including data acquisition, instrumentation, audio processing, and more.

Increased Signal Integrity: Well-designed multiplexers minimize signal distortion, crosstalk, and noise, preserving the integrity of the selected analog signal.

Improved System Efficiency: In systems where multiple sensors or inputs are periodically sampled, multiplexers reduce power consumption by allowing only one input to be active at a time.

Enhanced System Performance: An 8:1 multiplexer can be used to select the best signal source among multiple sensors, improving system accuracy and performance.

Reduced Complexity: It simplifies circuit design by reducing the number of switches and connections required to manage multiple analog inputs.

Data Acquisition: In data acquisition systems, multiplexers help scan and measure different analog signals, making them invaluable for monitoring and control applications.

Instrumentation and Testing: Multiplexers are commonly used in test and measurement equipment, such as oscilloscopes and spectrum analyzers, to select different input sources for analysis.

Communication Systems: In communication systems, multiplexers are used to switch between various channels, enabling the transmission of different signals over a shared communication link.

Medical Devices: Multiplexers play a crucial role in medical devices like ECG (Electrocardiogram) machines and blood analyzers, where they select different sensor inputs to monitor patient health.

Energy Efficiency: By enabling efficient signal routing and reducing power consumption, multiplexers contribute to overall energy efficiency in electronic systems.

Integration: Multiplexers can be integrated into larger systems, ensuring efficient signal management and control within the system architecture.

Consistency: Multiplexers provide consistent and repeatable signal routing, reducing the likelihood of errors in signal selection.

The challenges that we faced on implementing this project are:

Signal Fidelity: Maintaining high signal fidelity is critical, as any distortion, noise, or crosstalk between channels can significantly impact the quality of the output signal.

Bandwidth: Ensuring that the multiplexer can handle a wide range of frequencies without significant loss in signal quality can be challenging, especially for high-frequency applications.

Component Matching: Achieving consistent performance across all input channels can be challenging due to variations in component characteristics, such as transistor parameters.

Environmental Factors: Environmental factors such as temperature variations and electromagnetic interference (EMI) can impact the performance of the multiplexer and need to be considered in the design.

Reliability: Ensuring the long-term reliability of the multiplexer, especially in critical applications like medical devices, requires careful design and testing.

Design Method (PO(a))

An 8:1 analog multiplexer is an electronic device or integrated circuit (IC) that allows one to select one of eight analog input signals and route it to a single output. It's commonly used in electronic circuits to switch between multiple analog signals, and it operates like a digital switch for analog signals.
Here's the workflow of the process:

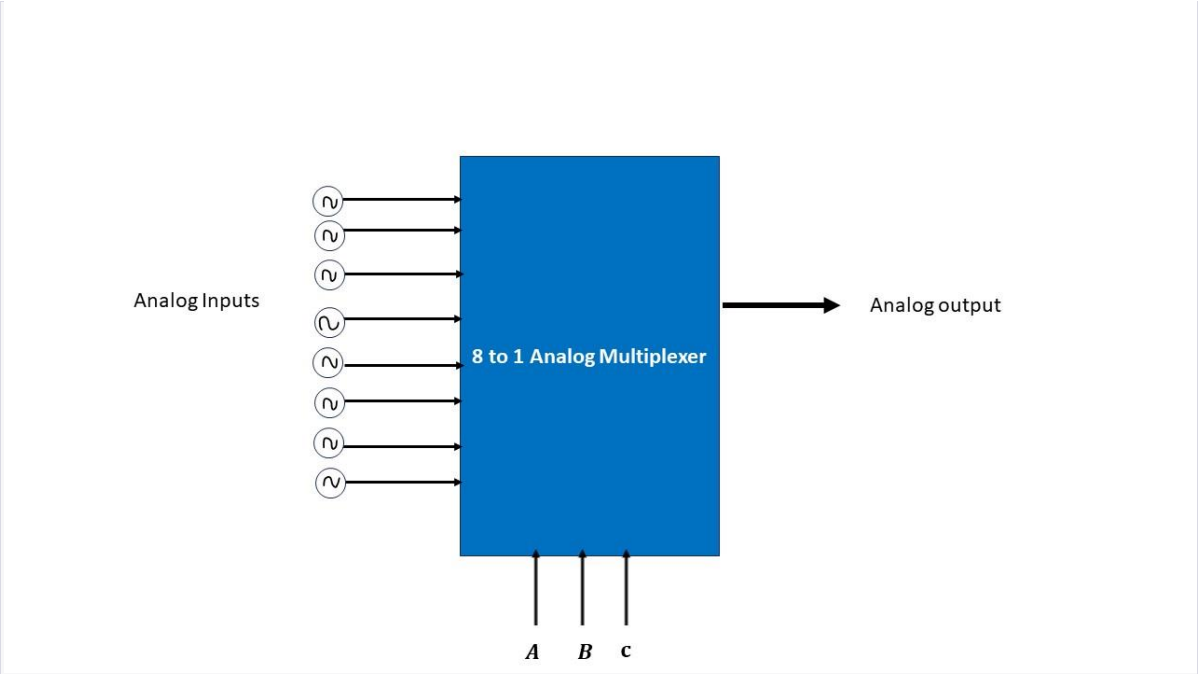
Input Channels: An 8:1 analog multiplexer has eight input channels, labeled from 0 to 7. Each channel is designed to accept an analog voltage or signal.

Control Inputs: It typically has control inputs that allow one to select which input channel gets connected to the output. These control inputs are binary in nature, which means they require a binary code to specify which input channel should be active.

Output: The selected input signal is then routed to the output of the multiplexer. The output can be connected to other components or processing stages in the circuit.

Multiplexing: Depending on the binary code applied to the control inputs, the multiplexer will connect one of the eight input channels to the output. For example, if we apply a binary code of "001" to the control inputs, it will connect the input channel labeled "1" to the output.

The block diagram is as follows:



We have designed the multiplexer using CMOS transmission gate logic. As it has 8 input channels, 3 select pins are needed to access any of the input to the output channel. That's why we have used 24 CMOS transmission gates to implement this design. There will be 3 transmission gates in each input channel and based on the state of the select pins, appropriate output will be selected. The logic equation describing the operation of the multiplexer is given by –

$$Vout = \bar{A}\bar{B}\bar{C}S_0 + \bar{A}\bar{B}CS_1 + \bar{A}B\bar{C}S_2 + \bar{A}BCS_3 + A\bar{B}\bar{C}S_4 + A\bar{B}CS_5 + AB\bar{C}S_6 + ABCS_7$$

This multiplexer uses 6 transistors for three selection lines. These 6 transistors are 3 CMOS whose gate voltages and outputs both work as control signals for the 24 transmission gates. Two logics are used in this design, CMOS logic and transmission gate logic. The CMOS logic can be described as follows:

CMOS Logic:

Complementary Metal-Oxide-Semiconductor (CMOS) logic is a widely used digital logic design technique that utilizes Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) to implement digital logic gates and circuits. CMOS logic relies on the operation of two types of MOSFETs: N-channel MOSFETs (NMOS) and P-channel MOSFETs (PMOS). NMOS transistors are ON when a voltage is applied to their gate terminal, allowing current to flow from the drain to the source. PMOS transistors are ON when a low voltage (complementary to NMOS) is applied to their gate terminal, allowing current to flow from the source to the drain. In our design of selection lines, we have used the most basic CMOS gate is the inverter, which consists of one NMOS transistor and one PMOS transistor. When the input is high, the NMOS transistor is ON, and the PMOS transistor is OFF, causing the output to be low. When the input is low, the NMOS transistor is OFF, and the PMOS transistor is ON, causing the output to be high. The inverter performs logical inversion and serves as the building block for more complex CMOS gates. CMOS logic offers several advantages, including low power consumption, high noise immunity, and compatibility with modern semiconductor fabrication processes.

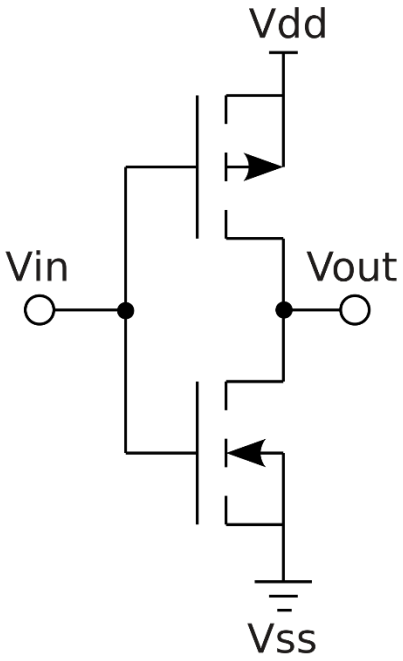


Figure 1: CMOS inverter circuit

We have used Vdd as 3 V and Vss as -3 V to implement the CMOS inverter.

Transmission Gate logic:

Transmission gate logic, also known as pass-transistor logic, is a digital logic design technique that uses MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) to perform logic functions. Unlike traditional static CMOS logic, which uses inverters and complex gate structures, transmission gate logic utilizes simple transmission gates to pass or block signals. A basic transmission gate consists of two MOSFETs arranged in parallel: one NMOS (N-channel MOSFET) and one PMOS (P-channel MOSFET). The behavior of a transmission gate depends on the control signal applied to the gate terminals of the NMOS and PMOS transistors. When the control signal is HIGH, the NMOS transistor is ON, and the PMOS transistor is OFF, allowing data to pass through unchanged. When the control signal is LOW, the NMOS transistor is OFF, and the PMOS transistor is ON, allowing inverted data to pass through. The circuit for a transmission gate will be:

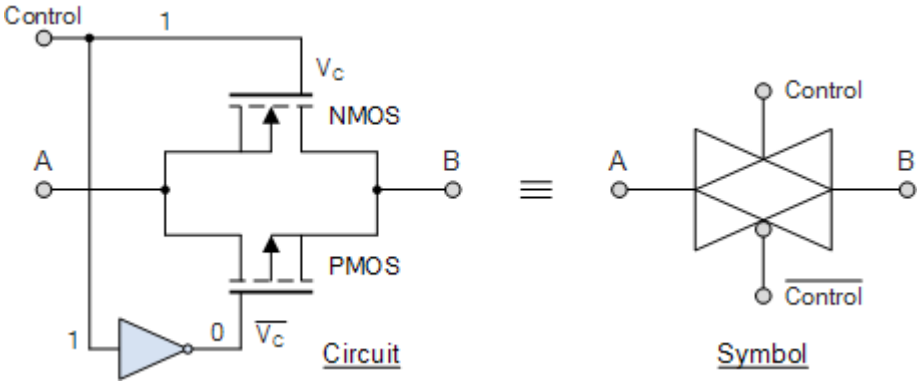


Figure 2: Transmission gate circuit

Transmission gate logic can be more power-efficient than static CMOS logic for some applications because it doesn't have the static power dissipation and offers low propagation delay. The control signals of transmission gates come from the selection lines.

Circuit Diagram and Results:

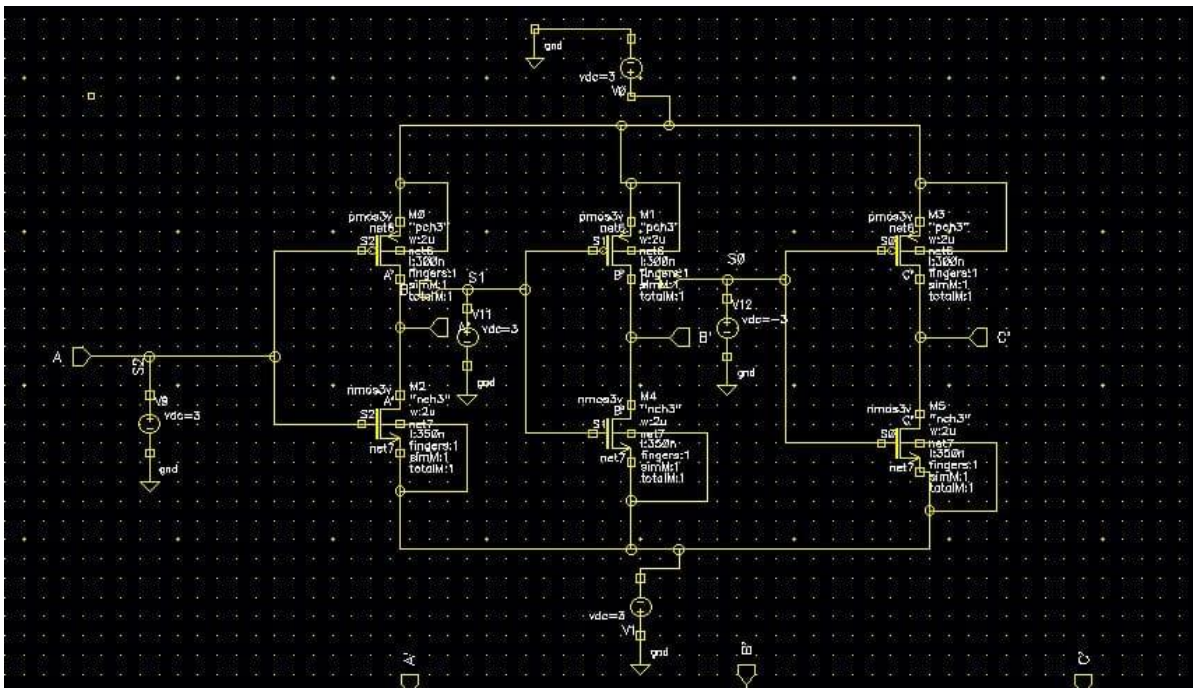


Figure 3: Selection Line circuit

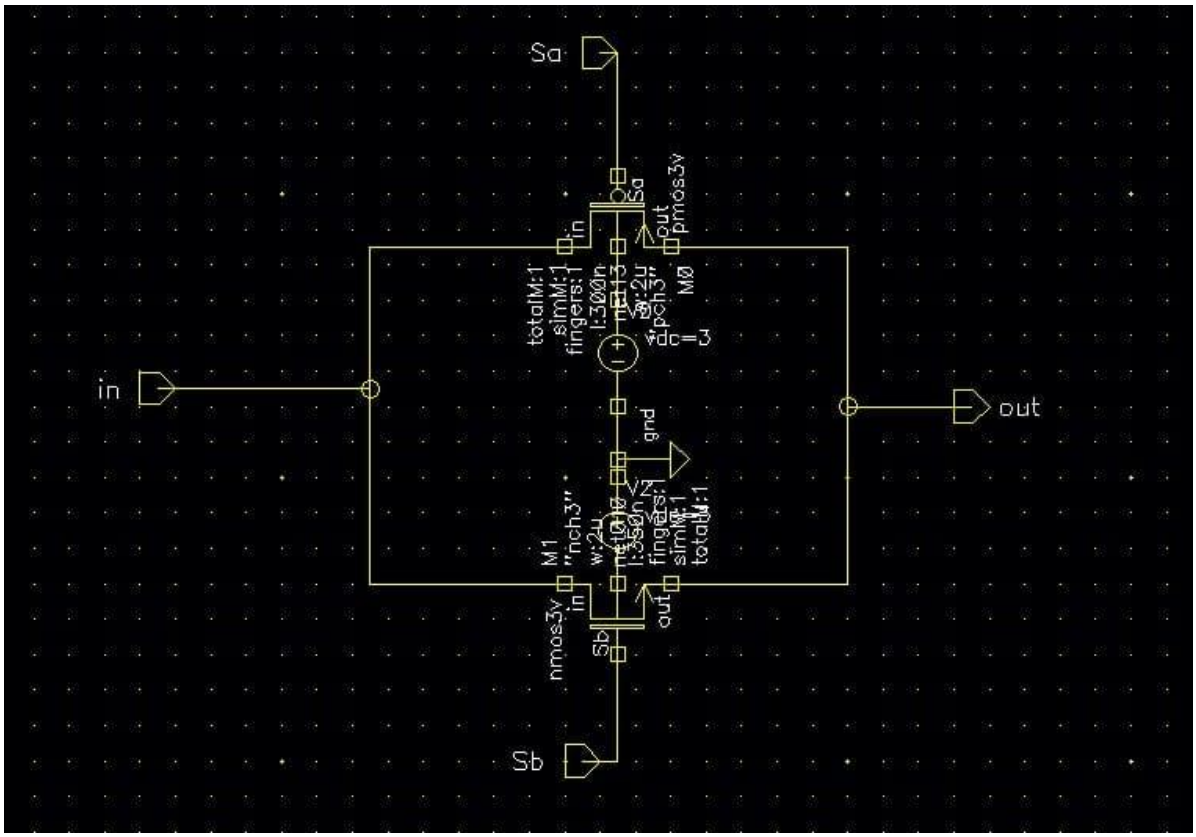


Figure 4: Transmission Gate Circuit

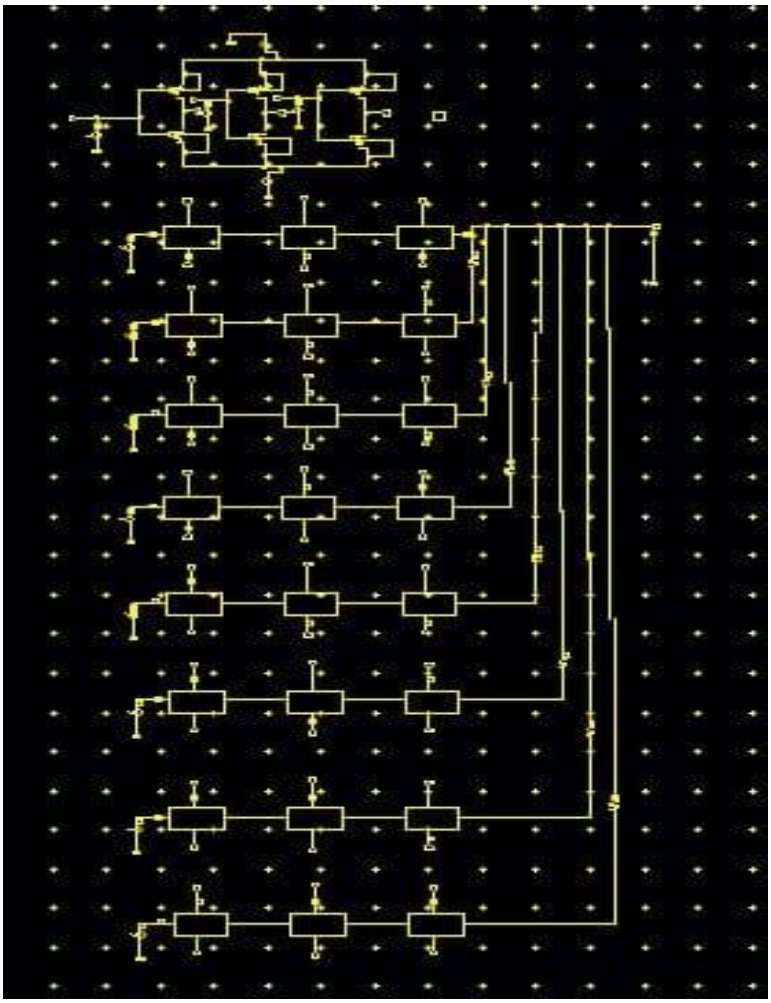


Figure 5: Full Circuit for 8:1 Analog Multiplexer

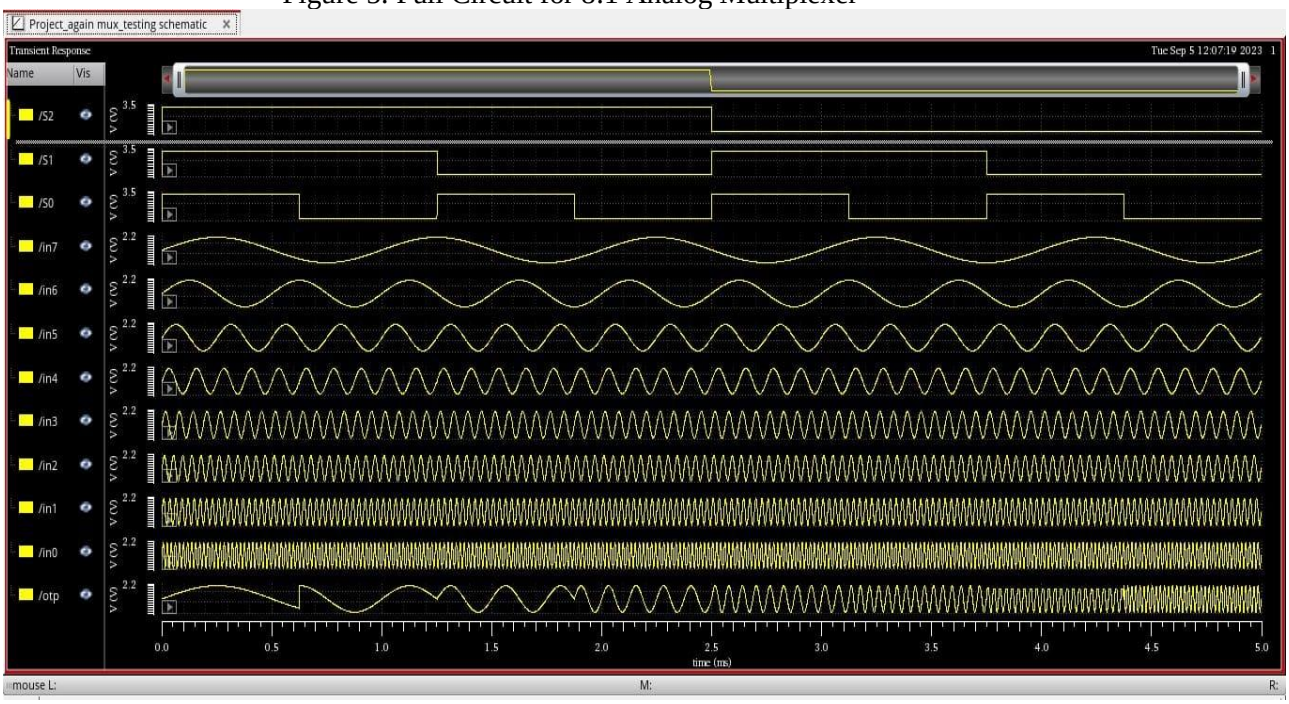


Figure 6: Results in the output terminal

Design Analysis & Evaluation:

Power Dissipation:

The required specification for power dissipation is 10mW (max). We have calculated the power dissipation using the equation:

$$P.D = VDD * IDD$$

Where VDD is the input supply voltage and IDD is the current drawn by the multiplexer. The result for the calculation of power dissipation is as follows:

```
I(V0:p) = -1.25242 nA
```

Here, the supply voltage VDD is 3V, so our power dissipation will be –

$$P.D = (3 \times 1.2542)nW$$
$$or\ , P.D = 3.7626\ nW$$

Which met our specific requirements.

Bandwidth:

The required bandwidth for our design is 1Mhz. We have got the exact bandwidth of 1Mhz by doing AC analysis of our design. The result is as follows:

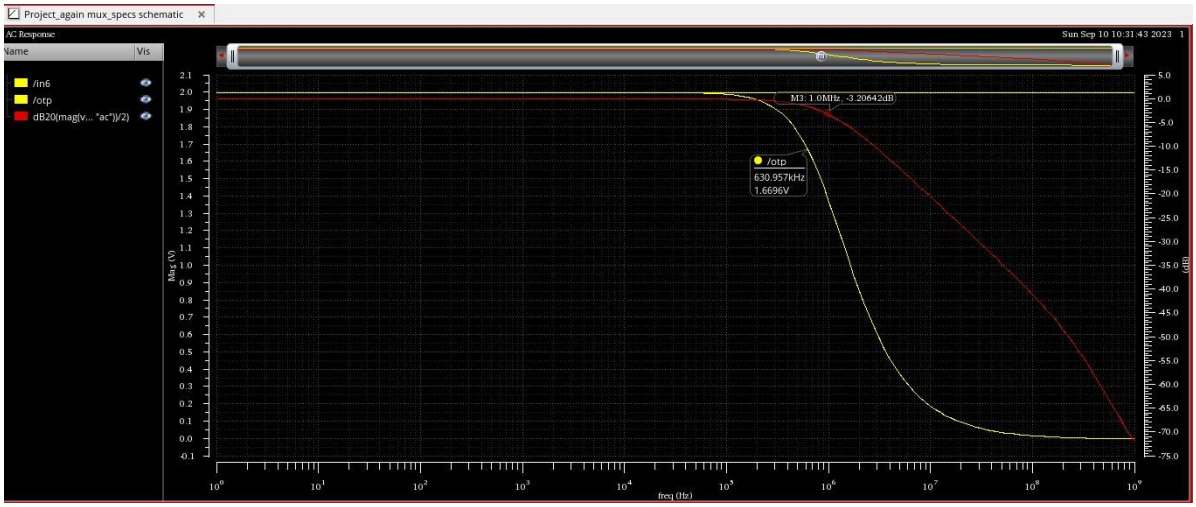


Figure 7: Bandwidth of our designed multiplexer

ON Resistance:

The formula for ON resistance is as follows:

$$Ron = \frac{1}{kn \times ID}$$

Where ID is the drain current of the switch. We have measured the voltage difference across the input and output of transmission gate terminal. We have also measured the current difference and current to measure the ON resistance. The result is as follows:

```
DC Operating Point:
    V(in) = 2 V
    V(net09) = 3 V
    V(net010) = -3 V
    V(net013) = -3 V
    V(net13) = 3 V
    V(out) = 1.99326 V
    I(V0:p) = -3.12864 pA
    I(V2:p) = -16.2574 pA
    I(V3:p) = 0 A
    I(V4:p) = 0 A
    I(V5:p) = -1.99326 mA
```

From these data, the calculated-ON resistance will be-

$$Ron = \frac{2 - 1.99326}{1.99326 \times 10^{-3}}$$
$$Ron = 3.38\ \Omega$$

For one input line, there are 3 transmission gates so the total ON resistance will be $3 \times 3.38 = 10.14\Omega$. However, in these circumstances, the bandwidth becomes very large and gets up to 70 MHz. If we want to keep our bandwidth at 1 MHz, the results are-

```
DC Operating Point:
    V(in) = 2 V
    V(net09) = 3 V
    V(net010) = -3 V
    V(net013) = -3 V
    V(net13) = 3 V
    V(out) = 760.659 mV
    I(V0:p) = -3.24013 pA
    I(V2:p) = -11.0827 pA
    I(V3:p) = 0 A
    I(V4:p) = 0 A
    I(V5:p) = -760.659 uA
```

Then ON resistance will be-

$$Ron = \frac{2 - 760.659 \times 10^{-3}}{760.659 \times 10^{-6}}$$
$$Ron = 1629.3\Omega$$

Considering 3 transmission gates, the total ON resistance will be $3 \times 1629.3 = 4887.9\Omega$. This can be considered as a tradeoff between bandwidth and ON resistance. If we want to have low ON resistance, the bandwidth will become larger and if we want moderate bandwidth ON resistance will become larger.

Charge Injection Time:

The required charge injection time is 5pC (max) where our designed project has 1.94 pC. The result from the Virtuoso IDE is-

	Expression	Value
1	integ(i("/V9/PLU...	1.940E-12

Logbook of Project Implementation:

Date	Milestone achieved
14/08/2023	Research started for the design.
21/08/2023	CMOS inverter designed.
28/08/2023	Transmission gates and full circuit were designed.
04/09/2023	Design was optimized to meet the required specifications.

References:

Udary, G., Chary, B., Sateesh, K., & Kumar, A. (2014). Design of Low Voltage Low Power CMOS Analog Multiplexer for Bio-Medical Applications. *International Journal of Engineering and Advanced Technology (IJEAT)*, *3*, 2249–8958. https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=1a802c57a55cf58157c19ae90d8556642f8c118f

Chen, C.-L., Hu, Y., Luo, W., Wang, C.-C., & Juan, C.-Y. (2012, May 1). *A high voltage analog multiplexer with digital calibration for battery management systems*. IEEE Xplore. https://doi.org/10.1109/ICICDT.2012.6232881