16 February
Tuesday

47-318 / Week 8

February 2021
S	M	T	W	T	F	S
	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28						

→ (CMOS)

Atmega - 2560 → 100 pin

Specs

*) High performance, low power Atmel® AVR® 8-bit controller

*) Advanced RISC Architecture

*) 135 instructions — most single clock cycle Execution

*) 32 × 8 general purpose working registers

*) Fully static operation.

*) up to 16 MIPS throughput at 16MHz. → million instruction per second

*) on-chip 2-cycle multiplier
  ↳ within 2 clock cycle the multiplication will done.

*) 256 KBytes Flash memory.
*) 4 KB EEPROM
*) 8 KB SRAM
*) write /Erase cycle — 10,000 Flash / 100,000 EEPROM

March 2021
S M T W T F S
1 2 3 4 5 6
7 8 9 10 11 12 13
14 15 16 17 18 19 20
21 22 23 24 25 26 27
28 29 30 31

February **17**
Wednesday

48-317 / Week 8

*) Two 8-bit Timer/Counter with Separate Prescaler and Compare mode.

*) Four 16-bit T/C with Separate prescaler, Compare and capture mode.

*) Real time Counter with separate Oscillator.

*) ☞ Four 8-bit PWM channels

*) 12 PWM channels with programmable Resolution from 2 to 16 bits

*) Output Compare Modulator.

*) 16 - channel, 10-bit ADC

*) programmable Serial USART

*) Master/Slave SPI serial interface

*) Byte oriented 2-wire Serial Interface

*) On-chip analog Comparator

*) Programmable watchdog Timer with Separate on-chip oscillator.

18 February
Thursday

49-316 / Week 8

February 2021
S	M	T	W	T	F	S
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28						

Special Feature

\#) Power-on Reset and Programmable Brown-out Detection

\#) Internal Calibrated Oscillator.

\#) External and Internal interrupt source

\#) Six sleep modes : Idle , ADC noise reduction , Power-save, Power-down, Standby and Extended Standby.

I/o and Package

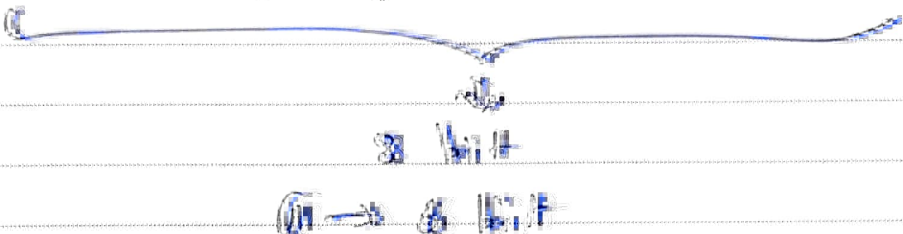\#) 86 programmable I/o lines

Power Consumption

Active mode : 1 MHz , 1.8V : 500 μA

Power down mode : 0.1 μA at 1.8V

Speed Grade

0-2 MHz → 1.8V - 5.5V

0-16 MHz → 4.5V - 5.5V

March 2021

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28	29	30	31			

February **19**
Friday

50-315 / Week 8

I/O - port → A, B, C, D, E, F, H, G, I, K, L

↓

8 bit

6 → 6 bit

For configuration of ports we need to configure three registers for it

1. Data Direction register (DDR)
2. Output Register (PORT)   x — PORT Name
3. Input Register (PINx)

If I write 1 in DDR means the port bit is configured to input. If I write 0 in DDR means the port bit is configured to output.

In PORT register if I write 1 means the bit is configured to Pull-up and input. If I write 0 the pull-up resistor off and to output.

Whenever the reset comes the port pins are set to tri-stated, even if the there is no clock.