CA Project

K. Ram Mohan

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Flow of Algorithm:

1. Creating Main Memory, Registers and Reservation banks and initializing them as global variables.
2. Putting some dummy values in to memory to doing operations.
3. Reading the instruction.txt file and storing them in a list to do one by one.
4. Taking instruction by instruction
    a. Checking whether the functional unit required for it is available or not. If not available pushing it once again to list
    b. If available filling the details of sources, destinations and others in to reservation banks. So that we can check later if any dependency is there or not.
5. Then executing the instruction using the Verilog hardware.
6. After execution updating the reservation bank details, register details. So that the instructions waiting for these values will be using them.
7. Then updating the completion time of instruction