CA_Lab5

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Verilog Code:

```
module REGISTERFILE (write, writeReg, writeData, readReg1, readData1, readReg2,
readData2, clk);
   input[4:0]  writeReg;
   input[63:0]  writeData;
   input write;
   input[4:0]  readReg1, readReg2;

   output[63:0]  readData1, readData2;

   input clk;
   reg[63:0] regFile[0:31];

   assign readData1 = regFile[readReg1];
   assign readData2 = regFile[readReg2];

   always @(posedge clk) begin
      if (write) begin
         regFile[writeReg] <= writeData;
      end
   end
endmodule
```

Test Bench:

```
module REGISTERFILE_TB;
   reg[4:0] writeReg;
   reg[63:0] writeData;
   reg write;

   reg[4:0] readReg1, readReg2;

   wire[63:0] readData1, readData2;

   reg clk;

   reg[4:0] index;

   REGISTERFILE regfile1(write, writeReg, writeData, readReg1, readData1, readReg2, readData2,
clk);

   initial begin
      clk = 0;
      forever begin
         #5 clk = ~clk;
      end
   end

   initial begin
      clk = 0;
      write = 1;
      $display("Writing Data");
```

```
        for (index = 0; index < 31; index = index + 1) begin
            #10 writeReg = index; writeData = index;
            $display("Write Address: %d, WriteData: %d", writeReg, writeData);
        end

        $display("\nReading");

        for (index = 0; index < 30; index = index + 2) begin
            #10 readReg1 = index; readReg2 = index+  1;
            #2 $display("Read Address1: %d, Read Data1: %d \tRead Address2: %d, Read Data2: %d",
readReg1, readData1, readReg2, readData2);
        end

        $finish(500);
    end
endmodule
```

Output:

```
C:\Users\rammo\OneDrive\Documents\CA\Lab\Lab5>vvp register
Writing Data
Write Address:  0, WriteData:                    0
Write Address:  1, WriteData:                    1
Write Address:  2, WriteData:                    2
Write Address:  3, WriteData:                    3
Write Address:  4, WriteData:                    4
Write Address:  5, WriteData:                    5
Write Address:  6, WriteData:                    6
Write Address:  7, WriteData:                    7
Write Address:  8, WriteData:                    8
Write Address:  9, WriteData:                    9
Write Address: 10, WriteData:                   10
Write Address: 11, WriteData:                   11
Write Address: 12, WriteData:                   12
Write Address: 13, WriteData:                   13
Write Address: 14, WriteData:                   14
Write Address: 15, WriteData:                   15
Write Address: 16, WriteData:                   16
Write Address: 17, WriteData:                   17
Write Address: 18, WriteData:                   18
Write Address: 19, WriteData:                   19
Write Address: 20, WriteData:                   20
Write Address: 21, WriteData:                   21
Write Address: 22, WriteData:                   22
Write Address: 23, WriteData:                   23
Write Address: 24, WriteData:                   24
Write Address: 25, WriteData:                   25
Write Address: 26, WriteData:                   26
Write Address: 27, WriteData:                   27
Write Address: 28, WriteData:                   28
Write Address: 29, WriteData:                   29
Write Address: 30, WriteData:                   30

Reading
Read Address1:  0, Read Data1:                    0     Read Address2:  1, Read Data2:                    1
Read Address1:  2, Read Data1:                    2     Read Address2:  3, Read Data2:                    3
Read Address1:  4, Read Data1:                    4     Read Address2:  5, Read Data2:                    5
Read Address1:  6, Read Data1:                    6     Read Address2:  7, Read Data2:                    7
Read Address1:  8, Read Data1:                    8     Read Address2:  9, Read Data2:                    9
Read Address1: 10, Read Data1:                   10     Read Address2: 11, Read Data2:                   11
Read Address1: 12, Read Data1:                   12     Read Address2: 13, Read Data2:                   13
Read Address1: 14, Read Data1:                   14     Read Address2: 15, Read Data2:                   15
Read Address1: 16, Read Data1:                   16     Read Address2: 17, Read Data2:                   17
Read Address1: 18, Read Data1:                   18     Read Address2: 19, Read Data2:                   19
Read Address1: 20, Read Data1:                   20     Read Address2: 21, Read Data2:                   21
Read Address1: 22, Read Data1:                   22     Read Address2: 23, Read Data2:                   23
Read Address1: 24, Read Data1:                   24     Read Address2: 25, Read Data2:                   25
Read Address1: 26, Read Data1:                   26     Read Address2: 27, Read Data2:                   27
Read Address1: 28, Read Data1:                   28     Read Address2: 29, Read Data2:                   29
```