

Flow of Algorithm:

1. Creating Main Memory, Registers and Reservation banks and initializing them as global variables.
2. Putting some dummy values in to memory to doing operations.
3. Reading the instruction.txt file and storing them in a list to do one by one.
4. Taking instruction by instruction
 - a. Checking whether the functional unit required for it is available or not. If not available pushing it once again to list
 - b. If available filling the details of sources, destinations and others in to reservation banks. So that we can check later if any dependency is there or not.
5. Then executing the instruction using the Verilog hardware.
6. After execution updating the reservation bank details, register details. So that the instructions waiting for these values will be using them.
7. Then updating the completion time of instruction

Tomasulo's Algorithm

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□ Three Steps:

□ Issue

- Get next instruction from FIFO queue
- If available RS, issue the instruction to the RS with operand values if available
- If operand values not available, stall the instruction

□ Execute

- When operand becomes available, store it in any reservation stations waiting for it
- When all operands are ready, issue the instruction
- Loads and store maintained in program order through effective address
- No instruction allowed to initiate execution until all branches that proceed it in program order have completed

□ Write result

- Write result on CDB into reservation stations and store buffers
 - (Stores must wait until address and value are received)