Design patterns reuse for real time embedded software development

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Abstract

This article describes software reuse components using C language on IBM-Rational Rose Real Time (RRRT) environment. In it a software development process becomes refined by means of a design pattern reuse. Its main contribution meets definition of a process for construction of a Data Logger Platform. Use of design pattern in an Integrated Computer Aided Software Engineering Environment allows definition of an industrial process aimed for future systematic reuse. Direction lines from Rational Unified Process (RUP) had recently helped undergraduate and graduate students from the Brazilian Aeronautics Institute of Technology (ITA) to create a fertile scene for practical applications of design pattern concepts. A Computer Software Component was constructed with attributes and generic methods in order to make possible its reuse. As a result of this process, members of ITA Software Engineering Research Group had generated a quality report previously improved to carry out classroom work, and proposed a specific data management design pattern for input and output.

Key words: CMMi, UML-RT, RUP, I-CASE-E, and Design Patterns.

1. INTRODUCTION

In second semester of 2007, members of Brazilian Aeronautics Institute of Technology Software Engineering Research Group (Grupo de Pesquisa de Engenharia de Software - GPES) had used Technological Development Laboratory of Casimiro Montenegro Filho Foundation (FCMF) to develop a Real Time Embedded Software (RTES).

Developed software used Problem Based Learning (PBL) methodology [1], IBM Rational Unified Process (IBM-RUP), an Integrated Computer Aided Software Engineering Environment (I-CASE-E), Rational Rose Real Time (RRRT) [2], and a design pattern [3] [4] [5] [6].

This work focuses on definition of a reuse process for design pattern in development of a RTES. RUP was modified in some key points to elaborate one design pattern. A case study, involving a Data Logger Platform – DLP was also developed, prototyped, and experimented as an IO Manager, using Microsoft Visual C ++ compiler. Use of I-CASE-E represents significant initial investments, involving licenses acquisition, equipment, training, and qualifications.

Conceptualization of a new software development process named W-model represents main contribution of this article. It involves identification, documentation, and reuse of a design pattern, and a quantification of productivity profits and quality, obtained from software reuse, during development process.

2. SCENARIO

This research applies PBL methodology aiming to restrict scope of design patterns reuse for software development, during System Development Life Cycle (SDLC) analysis, shown in Figure 3.

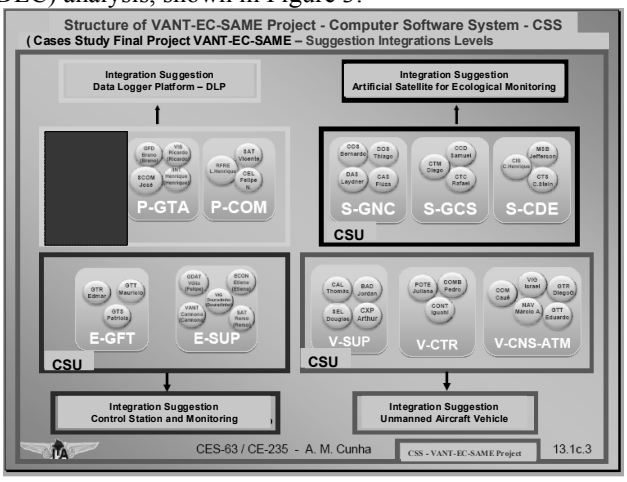

Figure 1 - CSS Structure of VANT-EC-SAME Project Cunha (2007).

In an academic environment, SDLC study for RTES has adopted following nomenclature. On highest level of project it is placed Computer Software System - CSS. It was divided into some Computer Software Configuration - Items CSCI. Each one of them was divided into different Computer Software Components CSC. Finally, each CSC

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was also divided into different Computer Software Units - CSU. All of them shown in Figure 1 as part of a project named VANT-TEC-SAME used as a case study.

CSC DLP is composed of following three different CSU: a Data Management Platform - DMP; a Storage Data Platform – SDP; and a Data Recovery Platform – DRP. They comprise CSS named VANT-EC-SAME (Veículo Aéreo Não-Tripulado – Estação de Controle – Satélite Artificial de Monitoramento Ecológico), an Unmanned Aircraft Vehicle together with a Control Station, and an Artificial Satellite for Ecological Monitoring [1].

3. I-CASE-E, OO, UML, AND DESIGN PATTERNS REUSE

IBM-RRRT integrated environment tools using Unified Modeling Language (UML) [7] was used to implement Object Orientation (OO) paradigms allowing components generation in C++ language in a design patterns project. UML has provided a visual language for modeling, building, and documenting OO complex software systems [5].

To evaluate use of design patterns it was necessary to analyze existing RUP, because reuse of patterns is not a natural phenomenon.

3.1 RRRT using OO and UML-RT

In order to reflect technical characteristics of codification, some traditional OO concepts [8] [9] such as classes and packages for real time design patterns software had been improved from traditional UML to Real Time UML (UML-RT).

In this scope, RTES can be explained by Systems that need signals and data in specific time intervals to have its use accepted. UML-RT was developed in accordance with IEC Std. 61499 and introduced to adjust classic UML for Real Time Systems [6].

Main aspects of UML adaptation to UML-RT [7] in this work have focused on concepts of increasing traditional OO, so that it can be implemented in a real time system by using RRRT. This UML-RT research line has focused in definition of constructors that had included capsules, connectors, and ports in order to build components with less aggregation among other systems elements [6].

In order to provide a disciplinary approach to distribute tasks and responsibilities within organized vision of software construction developed by IBM-Rational [10], RUP represents a product whose functions are to describe a complete and standardized process of Software Engineering.

Relationship between UP disciplines and UML Models are shown in Figure 2. UP has the same disciplines but UML-RT has more models [6].

RUP defines a set of software artifacts that are organized according to UP. They are necessary for implementation of software projects using best practices of Software Engineering [11]. RRRT is a visual modeling tool for Real-time that has mechanisms to support processes, methodologies, standards, and frameworks following RUP.

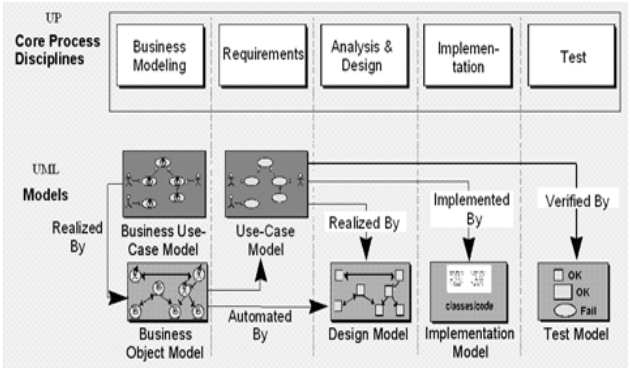

Figure 2 - UP and UML diagrams relationships [2].

According to a visual modeling of UML-RT in UP, the code generation by RRRT consists of a real-time framework. This abstraction originated from a universal modeling with UML-RT, made possible the generation of compatible source-codes for different languages, operating systems, and compilers [12].

The RRRT generates code to implement the projected system model [5]. Components generated by RRRT include packages, passive classes (with OO class's standards), capsules (active classes with ports and connectors), and protocol classes [2].

The activities' organization focused centrally in meta-models of classes and packages' diagrams. These meta-models were useful to define the conceptual tests of components using the following diagrams: Use Case, Class, Sequence, Structure, and State. The effectiveness of OO was translated by modeling UML-RT during the creation of source code in the C language.

3.2 The I-CASE-E RRRT Framework Tool

The software components' construction for real time systems has used a framework and the reutilization approach was top-down, allowing to select generic characteristics, hypothetically adaptable to other semantically similar components.

A framework is a collection of collaborative classes that provides specific functionalities. According to James Booch, frameworks are used to help the object orientation reuse [8] so that developers can customize them for new applications.

A design pattern project reuse application effect was gotten using I-CASE-E RRRT tool aiming to get a component architecture standard. This component had to be shaped according to UML-RT for an adaptive RUP [2] process.

A suggested and adaptive process model took place by the most convenient point of a construction process for design patterns' reuse. An existing concept like "V model" was derived from Manufacture Cells Production Line [13] for adaptive SDLC aiming components' reuse. Figure 3 shows a process represented by W-model.

The process was gotten through UP customization [14]. From this Figure 3, phases "one" trough "five" identify Business Requirements, Financial Requirements, Functional Requirements, Non Functional Requirements, and Detailed Requirements. Theses phases are represented by diagrams and more specifically by use cases.

SDLC's framework study is composed of twelve conceptual phases for reuse. The main contribution of this article is the phase six, placed between phases five and seven, as shown in Figure 3.

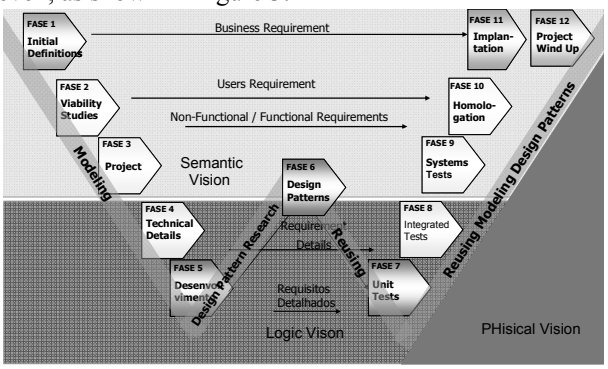

Figure 3 – The "W" metamodel of Component Reuse. Source: Authors.

The W-model was organized in three views: semantical, logical, and physical, all of them based upon different concepts. It reuses a set of procedures to define specific points to analyze and customize components.

The semantical view of W-model defines how a design pattern process will be researched and constructed. The logical view focus on groups of requirements distributed on the first five phases of the W-model. It addresses reusability aspects and its potential of reutilization. The potential of reutilization is given by the needs of a specific interest area, by means of functions' generalization. The physical view implements the construction, the adaptation, and components' test of a computational language.

3.3. Components Reuse

The utilization of specific OO concepts, UML-RT, RUP, RRRT tools, and Microsoft C++ characterizes a backbone for a software component reuse project [8] [9] [6]. The use of design patterns for code generation and the description of its reuse were first proposed by Budd [9], who stated that software products should be organized into activities for reuse.

Its main proposed directions for reuse have been defined by a set of fundamental characteristics for W-model functioning. The reuse process was constructed from definition of the following aspects described in Table 1.

Table 1 - Lines of direction for design patterns reuse.

- Generic systems requirements are defined by minimum environment characteristics, ceteris paribus, in Objective, Context, and basic Structure.
- Generic functionalities.
- Classes and Communication Protocol.
- Definition of a Customization Procedure.
- Definition of Test and Homologation.

For design patterns' reuse it is necessary to remodel it and to make it generic for researches' use with class diagrams. Production of reusable code demanded a customization treatment, in order to create a more elaborated and generalized design pattern.

The adaptation of a component is not an innovative activity. The hypothesis tested was: "component's reutilization will be faster and of better quality if a predefined systematic process does exist for generic services organized by application areas".

From a semantically view how similar are Use Cases and Classes of the involved components under analysis.

The reuse process is faster than the normal programming process if the identification and redefinition of a design pattern is more specialized. And the reuse process is slower than the normal programming process if the identification and redefinition of a design pattern is less specialized. It means that if the component is generic the reprogramming effort will be greater than the normal programming's process.

This reutilization hypothesis was verified with a test on semantic relationships in the UP framework using the RRRT. This standard was customized for a development process of components with adaptable and projected characteristics to allow these benefits to developers.

4. DESIGN PATTERN PROJECT

The GPES has considered the design pattern identified by the Research Group Gang of Four (GoF) that created a standard family among some available. The GoF has focused on object oriented programming languages and design pattern families in this research to accumulate generic class characteristics through attributes and methods [5].

GoF authors have considered initially the following standards' families: Creation, Structural, Behavior, and General Responsibility Assignment Software Patterns (GRASP) [4]. The starting point for a standard choice was the identification of one type to be used for a new entity selection.

The selected concept for developing project was the "Creation" standard with "Prototypation" subtype. For the reuse study and design patterns customization it was necessary to convert it from a standard to a standard family creating another family adjusted for its reuse and

customization.

The choice criterion was the association between classes and objects represented by the Creation of standards' families [2]. The design pattern was created by the GPES and classified under the name of IO Manager. This component fits in Behavior standards category. Therefore, it describes interactions' modeling and responsibilities' divisions between classes or objects.

4.1. The Design Pattern Identification Process

The identification process started with an existing research design pattern and its category. The standards' catalogued by GoF [4] had been distinguished in order to shape the design pattern IO Manager, as a good practical project standard [15].

The "cloning" operation consists in removing one component from a library to be reused in other project. In order to do it, this research provided a transformation from the design pattern Creation Prototype class to the design pattern Composite class, following the previous formulated hypothesis. This design pattern has followed QoS requirements from the structure of the library of components reuse catalogue form.

The catalog form is an artifact witch contains data and UML-RT modeling to register the functionalities of the CSC P-DLP presented in Figure 4.

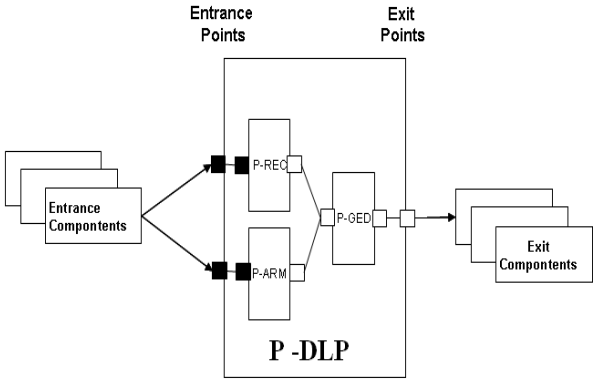

Figure 4 – CSC P-DLP design pattern class.

This catalog form aims to organize information to facilitate location and recovery of registries and implementation of standards in the library of design patterns.

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The Data Loggers allows to the control of the transactions carried between its dependent objects of drive and the storage control and recovery of data, programmed or by external accesses. A Data Logger project is illustrated in Figure 4.

5. THE DESIGN PATTERNS REUSE

The applicability of the standard of IO Manager project in Components of Input and Output Data Management came of VANT-EC-SAME Project, and it was possible through the technician detailing of the described and registered standard in a Catalog Form. The frameworks standard meets established in the requirement of the QoS to structuralize a server for the catalogued components reuse.

The Catalog Form contains the data and the UML-RT modeling, to attend to the three CSC P-DTL, Data Logger functionalities, represented for Figure 05. This Catalog Form aims to organize the information, so that this can facilitate its localization and recovery of the registered and implemented standards by the framework.

5.1. The design pattern description for reuse

The RUP process is generic and meets improvement chances in its procedures to accomplish design pattern processes identification, elaboration, and reutilization. During its definition, the RUP cannot be established without a previous definition of duties and responsibilities for each specialized activity.

The reusing process and the improvement change of RUP were identified and added in phase 6 of Figure 3 to modify the original "V model". Figure 4 presents this modification from the "V model", step by step, mapped to the "W-model". Following, all details are described as a complementary set of activities carried out for the design pattern reuse, characterizing the main contribution of this article.

The RUP tailoring for the design pattern process is shown in Table 2. It represents an original and adaptive way to solve implementation, verification, and validation for component reuse. A technique of implementation review is known as Final Inspection (FI) was carried out at the end of each SDLC project phase. It followed the concept of model Entry, Task, Verify, and eXit (ETVX) [16].

Table 2 – The pattern process to design pattern reuse activities.

Reuse procedure		
Activities	**Actions**	**Objectives**

1. Business Identification.	1. Analyze Semantic Similarities of Business, Financial, Functional, Non-Functional, and Detailed Requirements. 2. Create Requirements Attributes Matrices.	1. For each requirement type, there is a matrix that lists components that contain at least one requirement in one axis and all attributes in the other.
2. Candidate Components Selection in the Library.	1. Search components in library to identify requirements. 2. Analyze Requirements Traceability Matrices.	1. The choice criteria definition of traced components. For each requirement type, there is a matrix that lists components containing at least one requirement in one axis and all traced items in the other.
3. Components Test.	1. Analyze and test the infra-structure documentation.	1. Verification and Validation of the component test project.
4. Iteration and Customization for Planning.	1. Customize details for planning. 2. Create the requirements traceability tree.	1. Tree mapping traceability through a graphic visualization in order to see affected points and its relationships.
5. Components Distribution for Customization.	1. Make available documentation and customization to team-members.	1. Use of a requirement management tool to keep information repository.
6. Customization Process.	1. Measure, select and execute component customization from the library.	1. To update project planning from software estimation which consists of attributes identification to document products and requirements management. 2. To customize component submition for project review to determine if team members got necessary items to built components. 3. To identify existing components in the library. 4. To identify and review other similar activities in the design pattern process.
7. Identification of a Candidate Design Pattern.	1. Propose a new pattern to the library.	1. To select specification for project team members including the main justifications for architecture changes updates. 2. To select components from the library to be reviewed by team members, informing the project reviewer in advance when components are ready to be reviewed.
8. Cataloguing of Design Pattern.	1. Execute design pattern to the catalog process.	1. To catalog new design patterns elaborations, describing theirs motivations, applications, structures, reuse profits, and implementation examples. 2. To inform the catalog storage in the library about requirements, attributes, and project dependencies.
9. Finalization of Reuse Project.	1. Review the documentation.	1. To review and validate back steps and documentations.

6. ANALYSIS OF PRODUCTIVITY REUSE

A productivity analysis was performed by Use Case Points Effort Estimation using the same criteria shown in Figure 5.

An estimate was performed right in the beginning of the project for forecasting what would be the necessary effort for the development of the CSC P-DLP. A group of three developers with low monthly availability was considered for this academic project. In this case, the efforts estimation for the software development was equal to 5,5 months, as shown in Figure 5.

The effective time for the development of the CSC P-DLP Prototype in the CE-235 RTES discipline was very close to the previously estimated time. Three developers had dedicated about

600 working hours to elaborate the: Requirements Survey, Use Case Modeling, Sequence Diagrams, Classes Modeling, Capsules States Machines, and C Language Codification from the tools environment. environment

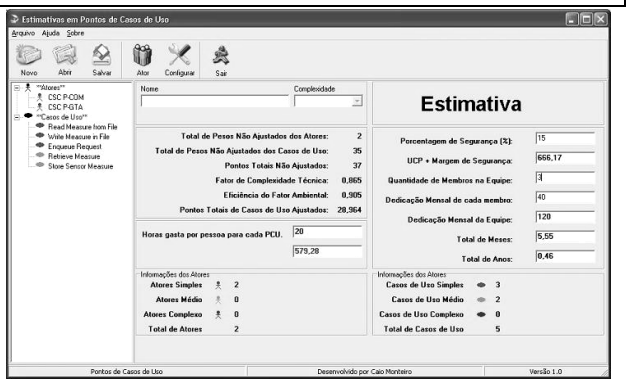

Figure 5. The P-DLP development effort using UCP.

Out off these 600 hours and considering only the RUP construction phase, about 300 hours had been dedicated for effective modeling, implementation and prototype tests. About 50 hours had been used for component generalization in a verification process using the results for functional validation characteristics of two inputs and outputs data components. In both CSC P-DLP and CSC P-COM, the same constructive process has been applied,

reusing the IO Manager design pattern. At the end of the implementation process in the same construction phase development times have been compared.

For this calculation, the time for developing CSC P-DLP and CSC P-COM was taking into account, according to the ceteris paribus condition [19] [20] [21]. Data tabulation is presented next, demonstrating self productivity profits in the construction phase reusing the IO Manager design pattern.

Table 3 - CSC P-DLP and CSC P-COM time construction using IO Manager.

Component	P-DLP	P-COM
Original construction time	300 h	230 h
Construction time using IO Manager design pattern	50 h	40 h
Productivity profit	85%	82%

Table 4 - CSC P-DLP project case study analysis.

SDLC	Other Phases	Construction Phase	Project Totals
P-DLP Project executed during CE-235	250h (42%)	350 h (58%)	600 h
P-DLP Project executed in FCMF, using IO Manager design pattern	250 h (83%)	50 h (17%)	300 h

The collected data analysis from Tables 3 and 4 allows concluding the significant earned value accomplished by reusing design pattern in case study as listed below:

1 - The effort in Project Total hours for the CSC P-DLP was 50% lower with the reuse of the IO Manager design pattern;

2 - In the Construction Phase of the CSC P-DLP, the gain with its reuse was 83% higher as compared with the previous estimation; and

3 - The Construction Phase duration was reduced from 58% to 17% as related to the Project Total hours.

7. CONCLUSION

This article presented a framework implementation, named "W-model", based upon a specialized process for identification, registration, and design pattern reuse for real time systems, based on Unified Modeling Language Real Time (UML-RT). Design patterns reuse for RTES development used Problem Based Learning (PBL) [1] within the software quality line of research. The main contribution from this paper was the "W-process" elaboration derived from the defined process of design pattern construction.

According to the last VANT-EC-SAME project survey, 15.096 Lines Of Code (LOCs) in C language have been generated by the Rational Rose Real Time (RRRT) tool CASE. These LOCs have been distributed in 56 archives, using visual modeling components and reusing patterns with a minimum of manual codification. An RRRT framework was used to plan activities and requirements for the components construction. The proper reutilization of components and design patterns allows may represent gains in effort, time, and costs throughout projects.

In this case study, the use of design patterns has required specific knowledge about Modeling, UML-RT, and RRRT. Technical knowledge in programming, as well as familiarity with test planning, abstraction capability, catalog, and design pattern was also required.

The catalog form creation and the UML-RT for RUP organization were fundamental for fulfilling design pattern test.

The construction and reutilization of the IO Manager design pattern have proved the hypothesis previously stated, allowing faster and better quality systematic for the construction of the W-process.

A significant earned value was accomplished on the case study application by using design pattern in a production line during the development of an RTES [13].

8. RECOMMENDATIONS

In order to continue this research, it is recommended:

1 – The reuse of the systematic Catalog Form concept on larger software scale components;

2 – The reuse of the "W-process" to support design pattern and Catalog Form in production lines of manufacture cells [13] [17];

3 – The refinement and review of the "W-process" to allow the customization for each new production line; and

4 - This model to be applied on software houses and factories [18] [19] [20] [21] [22] to scale profits in RTES production cells.

Finally, it is suggested that the results of this research be used as an alternative to improve technological implementation aspects using I-CASE-E for design pattern maximization.

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10. REFERENCES

[1] Cunha, A., "CE-235 Real-time Embedded Systems Lecture Notes", Brazilian Aeronautics Institute of Technology –

ITA. Available in : http://www.ita.br/~cunha, Available in: December de 2007.

[2] Rational Software Corporation, "DEV470 - Mastering Rational Rose Real Time - Student Material", Volume 1, 2003. Available in: http://www-128.ibm.com /com/ developerworks/rational/library/content/03July/1000/1155/ _umlmodeling.pdf. Available in: December 2007.

[3] Christopher, Alexander. A Pattern Language. USA: Oxford University Press, 1977.

[4] Erich Gamma, Richard Helm, Ralph Johnson, John Vlissides. Design Patterns: Elements of Reusable Object-Oriented Software. 1.ed. USA: Addison-Wesley, 1995.

[5] Gamma, E., Helm, R., Johnson, R., Vlissides J, "Design Patterns", Addison-Wesley, 2005.

[6] Selic, B., and J. Rumbaugh, "Using UML for Modeling Complex Real-Time Systems". Available in: http://www-128.ibm. Available in: October de 2006.

[7] OMG, "UML". Available in: http://www.omg.org/ gettingstarted /what_is_uml.htm. Available in: December 2007.

[8] Booch, G., "Object-oriented analysis and design with applications", Benjamin/Cummings, 1999.

[9] Budd, T., "An Introduction to Object Oriented Programming", Addison Wesley 3rd Ed, 2002.

[10] Jacobson, I., and Rumbaugh, J., "The Unified Software Development Process", Addison Wesley Logman, 1999.

[11] Rational Software Corporation, "Rational Unified Process". Available in: http://www-128.ibm.com/developerworks/ rational/library/may05/brown/index.html. Available in: December 2007.

[12] Seliec, B., Gullekson, G., and Ward, P., "Real-Time Object-Oriented Modeling", John Wiley & Sons, 1994.

[13] Montini, Denis Ávila, Modelo de indicadores de risco para o orçamento de componentes de software para célula de manufatura. / Denis Ávila Montini.360p. Dissertação (Mestrado) em Engenharia de Produção – Universidade Paulista - (2005).

[14] TCS, Tata Consultancy Services, "Operational Process for Iterative Development (Unified Process) Version 1.0", Integrated Quality Management System IQMS, Air India Building Mumbai, India October, 2006.

[15] Meszaros, Gerard and Jim Doble. Metapatterns: A pattern language for pattern writing. 3rd Pattern Languages of Programming conference, Monticello, Illinois, September 1996. Available in: http://hillside.net/patterns/writing/ patternwritingpaper.htm, Available in: December 2007.

[16] Radice E Philips, 1988, Special Report CMU/SEI-94-SR-3 - Exemplo de representação de processo em ETVX – Disponível no sítio WEB em 17/06/2007: www.seicmu.edu/pub/ docments /94.reports/pdf/sr03. 94. pdf.

[17] Montini, Denis Ávila; Spinola, Mauro de Mesquita; Sacomano, José Benedito; Nascimento, Marcos Ribeiro Do; BATTAGLIA, Danilo. Aplicação do Modelo PSP Manual e amparado por ferramenta CASE em um estudo de caso de Fábrica de Software Brazileira. Simpósio, Hotel Serra Azul - Gramado, RS, 2005.

[18] Montini, Denis Ávila; Spinola, Mauro de Mesquita; Sacomano, José Benedito; Nascimento, Marcos Ribeiro do; Battaglia, Danilo. Application of model PSP manual and supported by tool in a study of case of brazilian plant of software. Revista produção on line, Florianópolis - SC - Brazil, 2006.

[19] Montini, Denis Ávila; Albuquerque, Antonio Roberto Pereira Leite de; Nascimento, Marcos Ribeiro Do. Strategy for the use of the model of personal software process for the establishment of measurement and analysis for obtain CMMI level 2 in a study of case of a brazilian software factory. In: ASEE - 5th ASEE Global Colloquium on Engineering Education, Rio de Janeiro, 2006.

[20] Montini, Denis Ávila; Sekhar, Chandra; Negry, Tatiana Tavares; Nascimento, Marcos; Battaglia, Danilo. Strategy for the use of the model of personal software process for the establishment of measurement and analysis for obtain CMMI level 2 in a study of case of a brazilian software factory. In: Montivideu: TACTICS Iberoamerica 2006.

[21] Montini, Denis Ávila; Moreira, Gabriel de Souza; Vieira, Luiz Alberto; Battaglia, Danilo; Gnatiuc, Carlos Eduardo; Cunha, Adilson Marques da; In: TACTICS Iberoamerica 2007. Estudo de caso de uma estratégia de integração de middleware para um serviço SOA de gerenciamento e controle de fábrica de software: TCS – Tata Consultancy Services – Intranet website de Base de Conhecimento Corportativa KnowMax: TACTICS Iberoamerica 2007, Brazil, São Paulo, SP 25-26/October/2007.

[22] Montini, Denis Ávila; Moreira, Gabriel de Souza; Vieira, Luiz Alberto; Battaglia, Danilo; Gnatiuc, Carlos Eduardo; Cunha, Adilson Marques da; In: Global TACTiCS 4th Global Conference, Study of case of a strategy of middleware integration for SOA service of administration and control of factory of software: TCS – Tata Consultancy Services – Intranet website Corporative Knowledge Data Base KnowMax: Global TACTiCS 4th Global Conference, Índia, Kerala, Thiruvananthapuram. 16-19/January/2008.