



**Escola de Enxeñaría de Telecomunicación**

**Microwave and Millimetre Wave Circuit  
Design and CAD**

**COMMUNICATIONS TRANSCEIVER  
PA DESIGN**

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# 1 Introduction

The aim of this practice is the design and manufacture of a narrowband power amplifier in class A, for a center frequency of  $f_o = 2.3GHz$ , using ADS simulator. The circuit is made of a single amplification stage.

The performance specifications to be obtained with this circuit are:

- 12 [dB] Gain at  $f_o = 2.3GHz$ .
- 13 [dBm] At 1 dB compression point.

The active device used is "ATF35143". The transistor non-linear model is included in the corresponding ADS project design, and it has been downloaded from the manufacturer website.

Practice sections follow the logical evolution of the design of a power amplifier and they will include question to help you understand the specifics of the design of these circuits. The ADS design will be implemented in the ADS Project: *MMCAD\_PA\_Design\_wrk*.

# 2 Design using ideal ckt components

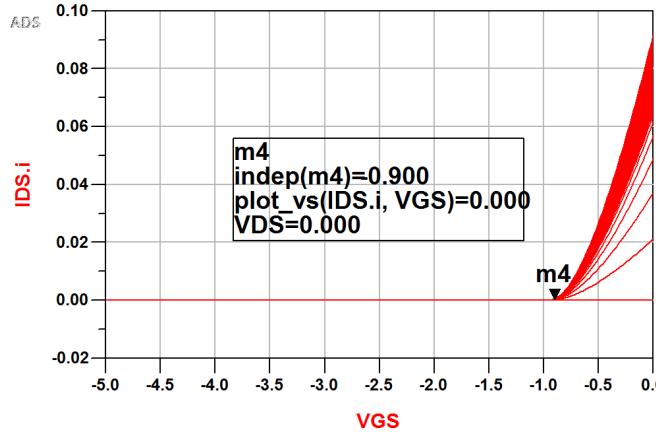
Initially, in the PA design it will be used ideal models of the components, thus a first estimation of the circuit performance is obtained

As you do know that there are different way to design amplifiers depending on the goal or performance to be obtained. It is not the same to design an amplifier for low noise, maximum gain or maximum RF power. In the present design, we seek to maximize the output RF power to that corresponding to the 1dB compression point, at a certain frequency, although the obtained gain is not maximum that can provide the transistor.

## 2.1 Bias point selection

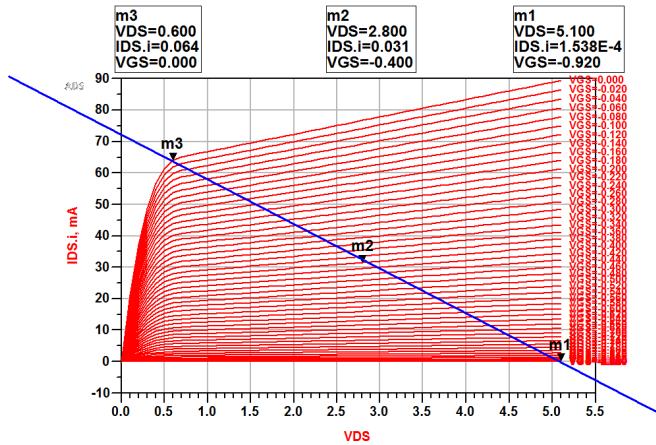
**Question #1:**

The figure (1) shows the value of  $V_{gs}$  above which the device starts to drive current,  $V_{th} = -0.9V$ .



**Figure 1:**  $I_{ds}$  versus  $V_{gs}$

The figure (2) shows the variation of  $I_{ds}$  versus  $V_{ds}$  for different values of  $V_{gs}$ .



**Figure 2:**  $I_{ds}$  versus  $V_{ds}$

Bias point could be calculated using the following formula:

$$V_{dsQ} = \frac{V_{dsmax} + V_{dsmin}}{2} \quad (1)$$

Where

- $V_{dsmax} = V_{gdB} - |V_{th}| + V_{OFFSET} = 5 - |-0.9| + 1 = 5.1V$
- $V_{dsmin} = V_{knee} = 0.6V$

Replacing  $V_{dsmax}$  and  $V_{dsmin}$  values in equation 1 gives

$$V_{dsQ} = \frac{5.1 + 0.6}{2} = 2.85V \quad (2)$$

$I_F$  is the maximum current in the  $V_{knee}$  of the figure (2), i.e., the maximum current that will be supported for the device.

$$I_{dsQ} = \frac{I_F}{2} = \frac{64}{2} = 32mA \quad (3)$$

Finally,  $V_{gs} = -0.4$  for the calculated bias point

**Question #2 :**

According to data-sheet, maximum drain current is  $I_{ds} \approx 80mA$ . For the transistor operates as class A amplifier, it is needed  $V_{gs} = -0.4$ .

**Question #3 :**

The slope of the load line is the optimal resistance.

$$R_{opt} = \frac{V_{dsMAX} - V_{dsMIN}}{I_{dsMAX} - I_{dsMIN}} = \frac{5.1 - 0.6}{0.064 - 0} = 70.31\Omega \quad (4)$$

The maximum RF power estimated, is.

$$P_{RFMAX} = \frac{1}{2} \frac{V_{dsMAX} - V_{dsMIN}}{2} \frac{I_{dsMAX}}{2} \quad (5)$$

$$P_{RFMAX} = \frac{1}{2} \frac{5.1 - 0.6}{2} \frac{0.064}{2} = 0.036W \quad (6)$$

$$P_{RFMAXdB} = 10\log_{10}(P_{RFMAX}) = 10\log_{10}(36) = 15.56dBm \quad (7)$$

The DC power estimated, is.

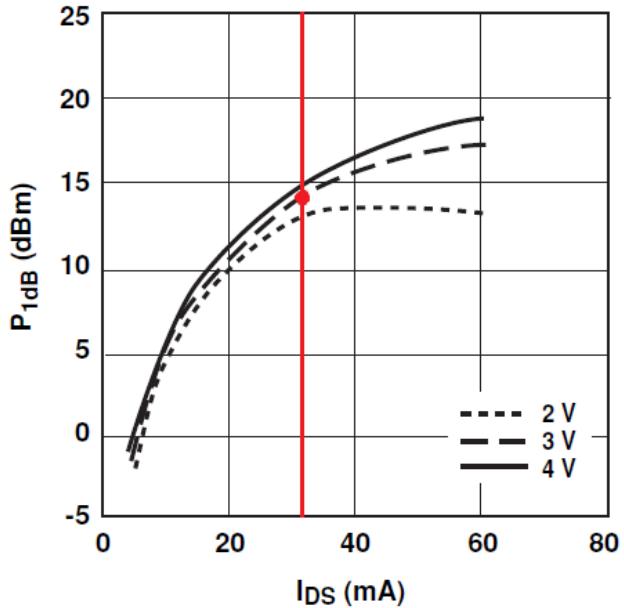
$$P_{DC} = V_{dsQ}I_{dsQ} = 2.85 * 0.032 = 0.091W \quad (8)$$

Efficiency

$$\eta = \frac{P_{RFMAX}}{P_{DC}} 100 = \frac{0.036}{0.091} 100 = 39.56\% \quad (9)$$

**Question #4 :**

According to data provided by the manufacturer (see figure (3)), for  $V_{ds} = 3V$  and  $I_{ds} = 32mA$ , the transistor provides 15 dBm RF power. These data are consistent with those obtained with the ADS, because with the bias point chosen, the RF power is 15.56 dBm.



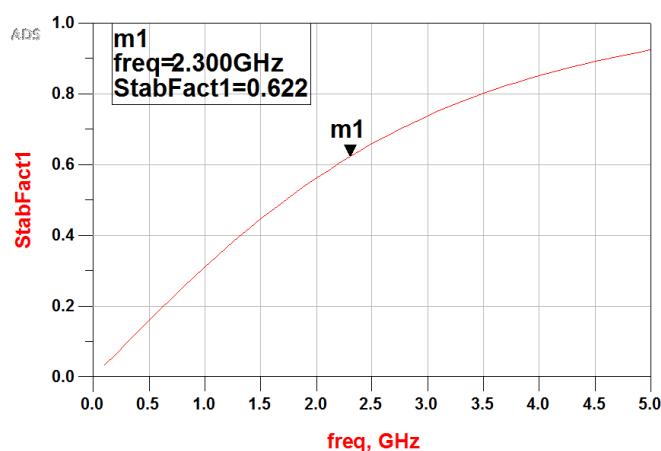
**Figure 3:**  $P_{1dB}$  versus Bias (Active Bias) Tuned for NF @ 2V, 15 mA at 2 GHz

## 2.2 S-Parameters SIMULATION

### 2.2.1 Assessing Stability

**Question #5 and #6 :**

Obtained stability figures are shown in the following section



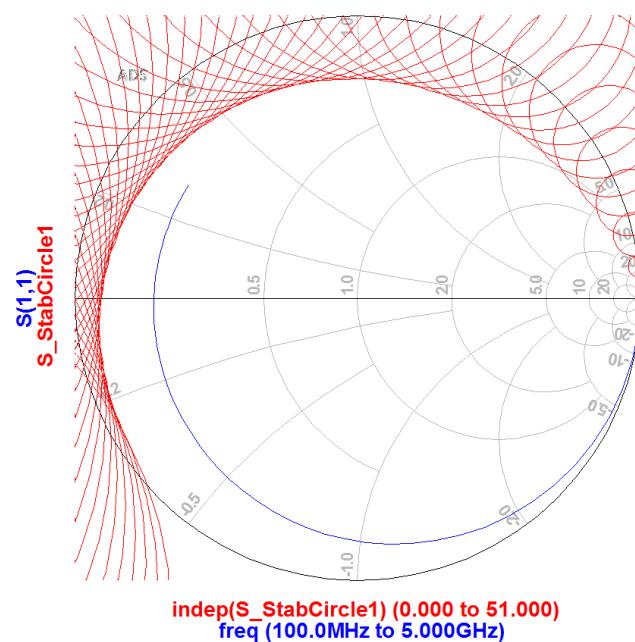
**Figure 4:** Rollet factor( $K$ ) variation with frequency



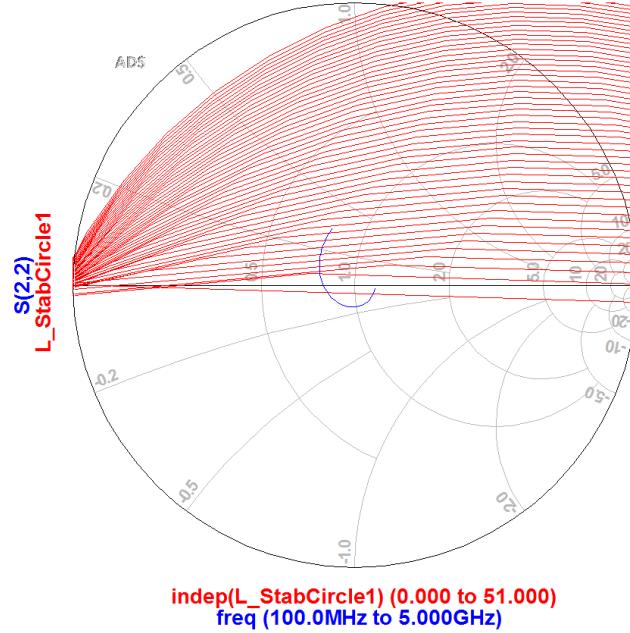
**Figure 5:** Delta factor( $\Delta$ ) variation with frequency

It can be seen that there are frequencies where  $0 < K < 1$  and  $|\Delta| < 1$  therefore, the amplifier is conditionally stable

Another method to analyse stability is using stability circles(see figures (6) and (7)).



**Figure 6:** Source stability circle



**Figure 7:** Load stability circle

### 2.2.2 Source and Load Impedances Computation

**Question #7 :**

- The optimum impedance output:

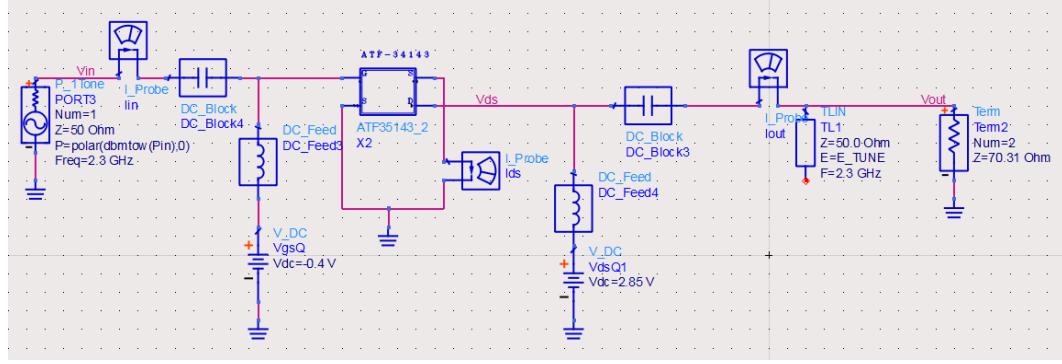
The optimum output impedance is that one allowing the load line (see figure (2)) and cancelling the susceptance output of the transistor. According to Cripps method, the optimum load impedance is that one cancelling the output capacity  $C_{ds}$ . That capacity value can be calculated as  $-i\{Y_{12} + Y_{21}\}$ . The optimum output impedance is the parallel of  $R_{opt}$ , as calculated as in figure (2), with  $C_{ds}$ .

In this case, as  $i\{Y_{12} < 0\}$  and  $i\{Y_{21} > 0\}$  has been obtained(see figure (8)), the Cripps method can not be used.

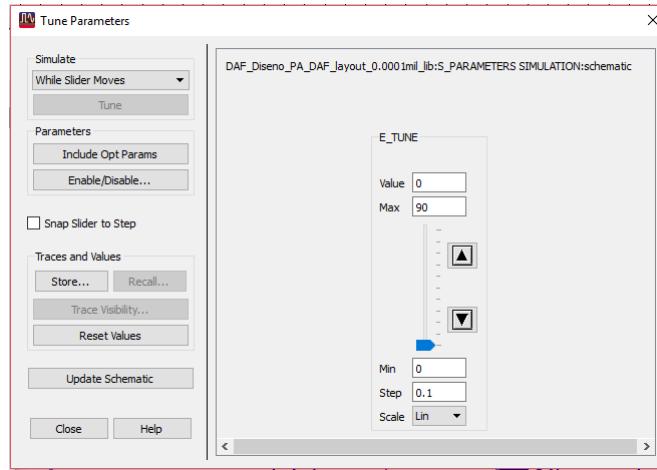
freq	$Y(1,2)$	$Y(2,1)$
2.300 GHz	-1.161E-4 - j0.003	0.103 - j0.048

**Figure 8:**  $Y_{12}$  and  $Y_{21}$  parameters

The effect of the capacity can also be achieved using an open-circuit stub in parallel with the load. By tuning the length of this stub, RF power can be maximized. Once the optimal length has been obtained, the imaginary part of  $Z_{opt}$  can be calculated.



**Figure 9:** Tuning the length of open-circuit stub in parallel with the load,  $\iota\{Z_{opt}\}$  calculation



**Figure 10:** Tune Parameters

Probes have been used to obtain the  $Z_{opt}$  value. Results can be seen in figure(11))

Pin	Zin	Zout
1.500	9.671 - j40.433	70.310 - j1.941E-15

**Figure 11:** Optimum impedance output and input impedance

Results:

$$Z_{opt} = 70.31 \Omega$$

- The input impedance when the transistor is loaded with  $Z_{opt}$  (see S parameters, figure (12)):

$$Z_{in} = Z_0 \frac{1 + \Gamma_S}{1 - \Gamma_S} \quad (10)$$

when  $\Gamma_S$  and  $\Gamma_L$  are:

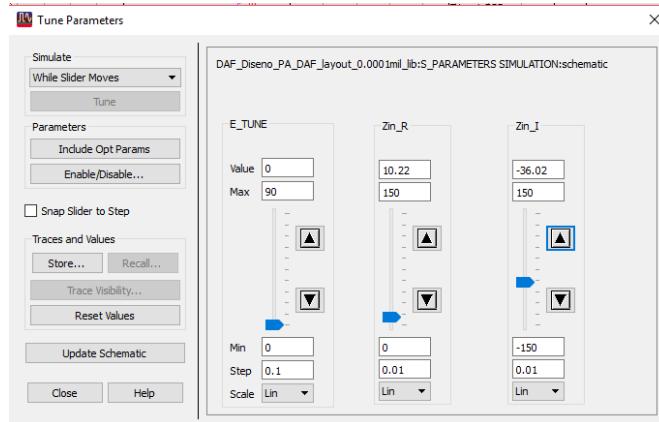
$$\Gamma_S = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (11)$$

$$\Gamma_L = \frac{Z_{opt} - Z_0}{Z_{opt} + Z_0} \quad (12)$$

freq	S(1,1)	S(1,2)	S(2,1)	S(2,2)
2.300 GHz	-0.232 - j0.749	0.093 + j0.065	-1.083 + j4.823	-0.166 - j0.213

**Figure 12:** S parameters

Input impedance is optimized by tuning real and imaginary parts of the input impedance. To tune  $Z_{in}$ , auxiliary variable should be created ( $Z_{in\_R}$  and  $Z_{in\_I}$ ) both for real and imaginary parts (see figure (13)). As a starting point for estimation of  $Z_{in}$ , obtained values using probes may be used ( $Z_{in} = 9.67 - 40.43i\Omega$ , see figure (11))



**Figure 13:** Tune Parameters

Results:

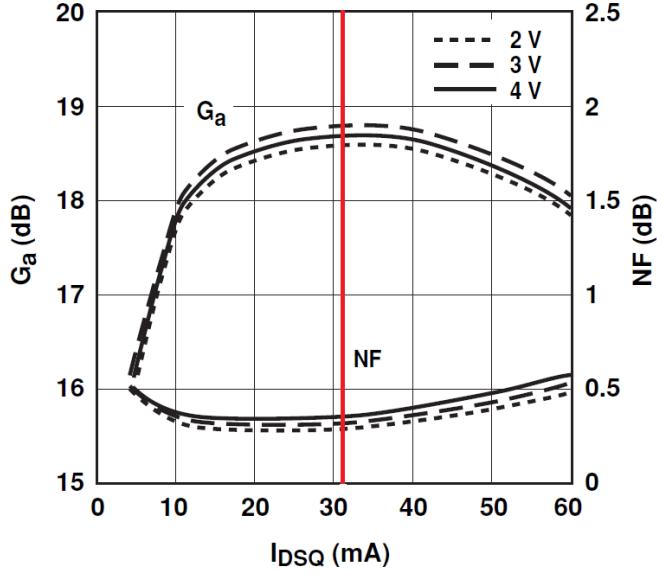
$$Z_{in} = 10.22 - 36.02i\Omega$$

### Question #8 :

At the center frequency (2.3 GHz), 11.809 dB of gain is obtained (see figure (14)). The manufacturer gives a value of close to 18.8 dB (see figure (15)).



**Figure 14:** Operating Power Gain at 2.3 GHz



**Figure 15:** NF and  $G_a$  vs. Bias at 2 GHz

[H]

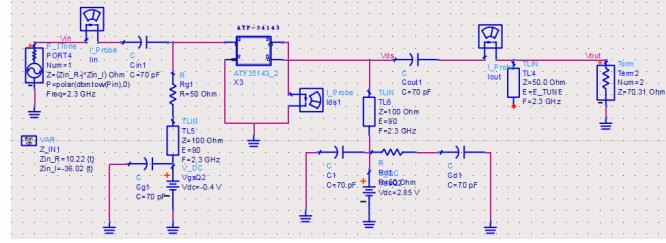
### 2.3 BIAS AND STABILITY NETWORK

With the bias circuit the schematic is as shown in figure (16). The capacitors values,  $C_g$ ,  $C_d$  and  $C$  have been chosen to achieve a impedance lower than  $1\Omega$  at 2.3 GHz frequency.

$$Z_c(f_o) = \frac{1}{j2\pi f C} < 1\Omega \quad (13)$$

Then:

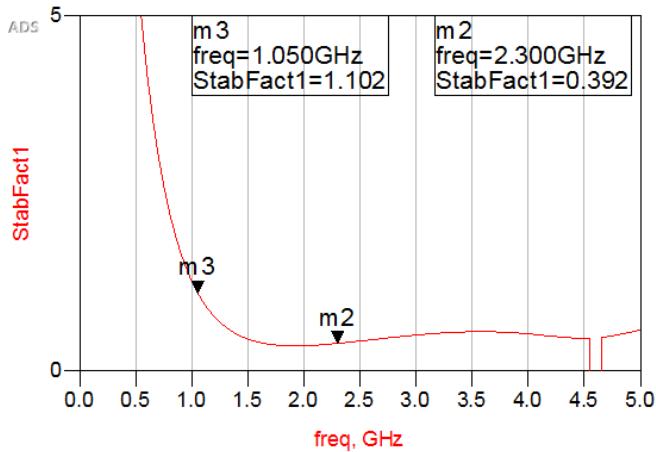
$$Z_c(f_o = 2.3GHz) > 69.198pF \approx 70pF \quad (14)$$



**Figure 16:** Schematic with the bias circuit

### Question #9 :

A new value of Rollet factor is shown in the figure 17. Modifications made to the circuit managed to stabilize the amplifier at frequencies below 1 GHz. The amplifier is conditionally stable at  $f_0$  frequency( $K < 1$ ).



**Figure 17:** Rollet factor in schematic with the bias circuit

To stabilize the circuit it was necessary to add a series resistor at the gate of the transistor. This solution would be discussed in the section "MICROSTRIP PA DESIGN". The questions #10 and #11 are solved with a Microstrip design hereinafter.

### Question #10 :

It is not necessary to answer this question because it was not needed a resistor in the drain to stabilize the transistor.

### Question #11 :

Now, with the resistor at the gate the transistor is unconditionally stable due to  $K > 1$  for all frequency bands. As a counterpart the gain is reduced in 3 dB.

### 3 MICROSTRIP PA DESIGN

After obtaining a preliminary ideal PA design, we will proceed now to use other passive component models that are closer to the actual components, so less idealized (since they include parasitic behaviour, hence, undesired). As a consequence, our circuit performance will be degraded, but simulation results will be closer to the fabricated prototype.

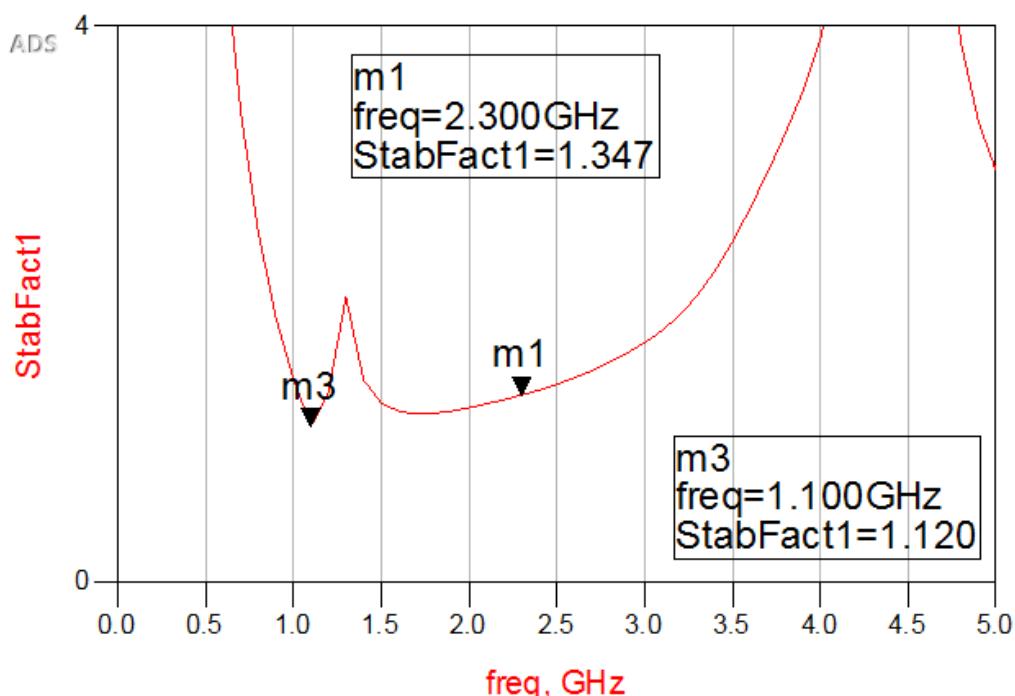
Besides using passive circuit components, we will replace ideal TLs by microstrip TLs and microstrip discontinuities (bends, T-junctions, Cross-junctions, steps...) to connect the different elements.

#### 3.1 S-parameters simulation

**Question #27 :**

It was necessary to introduce a  $R_{series} = 13\Omega$  in the gate of the transistor to achieve stability at the desired operating frequency  $F_o = 2.3GHz$ .

In the figure (18), stability factor is shown; it has been obtained using microstrip bias network. Microstrip design introduces losses, therefore,  $R_{series}$  value is less than the ideal design



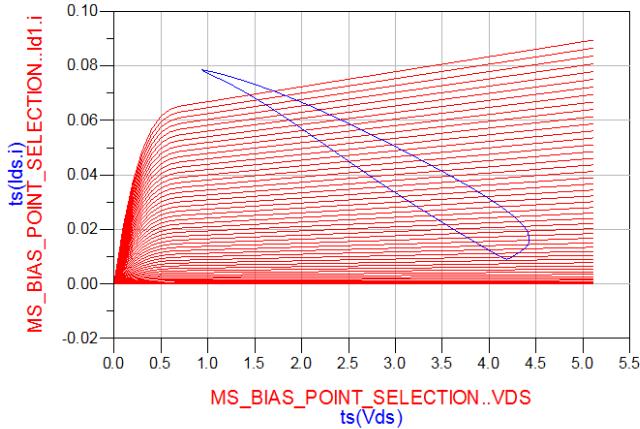
**Figure 18:** Rollet factor in schematic with the bias circuit( $R_{serie}$ ), microstrip design

### 3.2 Matching networks design

#### Question #28 :

Firstly, it is searched the optimal load impedance. Load resistance is obtained from the dynamic load-line(look at the figure (2)),which maximize the power RF of the amplifier ( $R_{opt} = 70.3\Omega$ ). Therefore it is necessary to make an adaptation of  $50\Omega$  to  $70.3\Omega$ . Once the load impedance is fixed, the input impedance is calculated ( $Z_{in} = 16.3 - 3.1i$ ). Consequently, it is necessary to make an adaptation of  $50\Omega$  to  $.16.3 - 3.1i$ .

The next figure(19) shows the dynamic load-line obtained after input and output impedance are fixed.



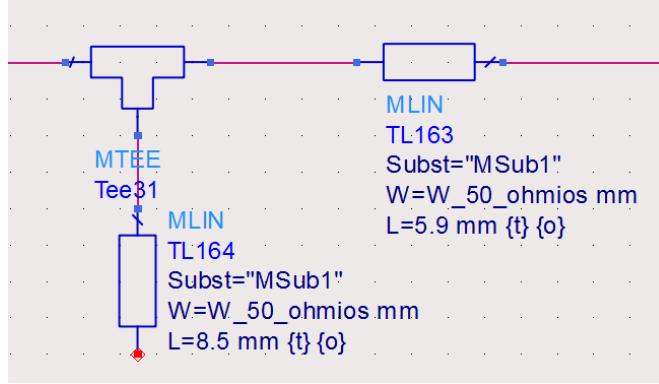
**Figure 19:** Dynamic load-line

### 3.3 Optimization

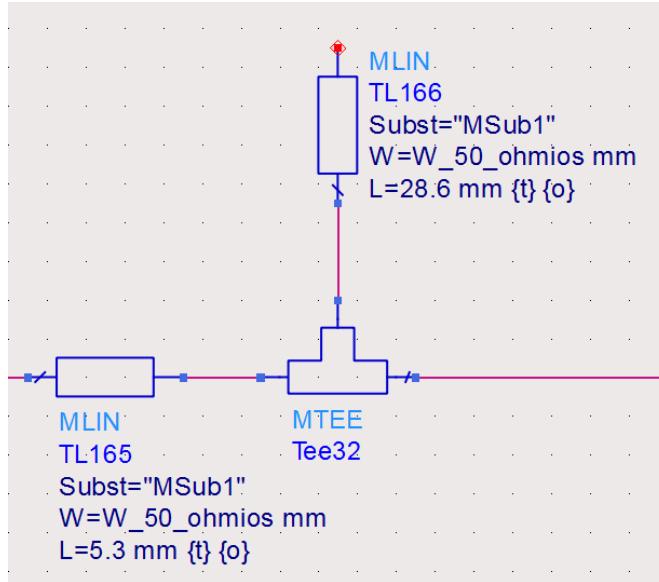
#### Question #29 :

Firstly, the matching input and output networks are obtained using Smith Chart tool. Subsequently, using LineCal tool, physical dimension of the stubs are calculated.

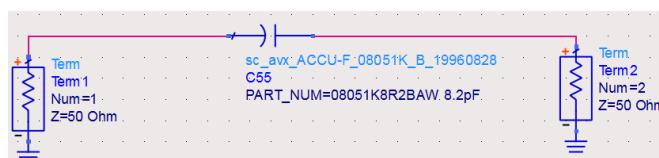
- The optimum impedance output: The matching output network is optimized by tuning length of the stubs. This optimization must maximize  $P_{1dB}$  without putting the dynamic load-line out of order. We can not forget that the slope dynamic load must be consistent with the A class operation.

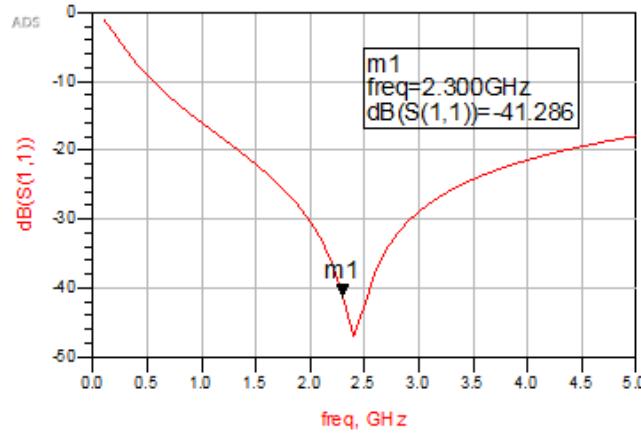
**Figure 20:** Input matching circuit

- The input impedance when the transistor is loaded with  $Z_{opt}$ : As in previous case, the matching input network is optimized by tuning length of the stubs. This optimization must maximize the gain.

**Figure 21:** Output matching circuit

- DCblocks: Instead DCBlock must be used real capacitors, and these must be chosen so that its resonant frequency matches the amplifier. After trying various capacitance values, it is found that capacitor  $8.2pF$  had a resonance frequency of about  $2.3GHz$ . The circuit to obtain the capacitor and reflection coefficient at the input, are shown in figure (22) and (23) respectively.

**Figure 22:** Circuit to search the capacitor that resonates at  $2.3GHz$



**Figure 23:** Reflection coefficient of the input capacitor  $8.2\text{pF}$

### 3.4 Results

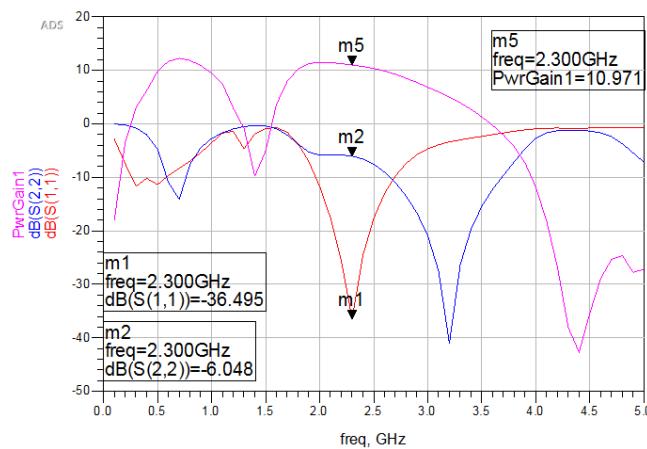
**Question #31(16) :**

There is not perfect matching in the input or in the output, although the reflection coefficient at the input is quite small. At the output is allowed worst matching, because load impedance is chosen to maximizing RF power, power gain is not maximized.

Power gain is  $\approx 11\text{dB}$ , close to the desired value  $12\text{dB}$ .

freq	$S_{(1,1)}$	$S_{(2,2)}$	PwrGain1
2.300 GHz	0.015 / 130.038	0.498 / 50.997	10.971

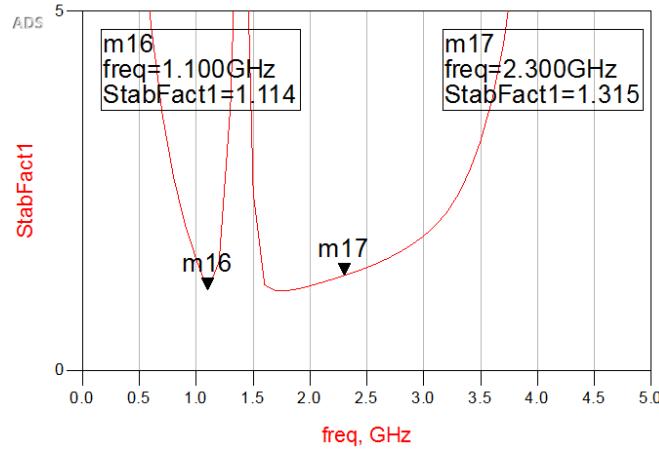
**Figure 24:** Gain power, reflection coefficient at the input( $S_{11}$ ) and reflection coefficient at the output( $S_{22}$ )



**Figure 25:** Gain power, reflection coefficient at the input( $S_{11}$ ) and reflection coefficient at the output( $S_{22}$ )

**Question #32(17) :**

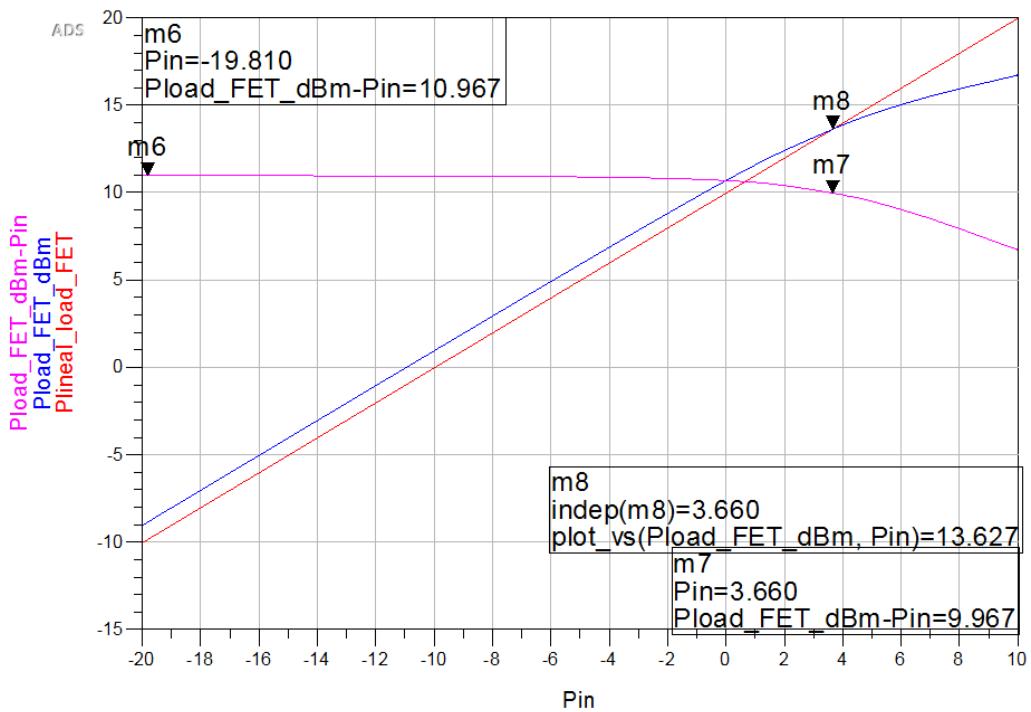
The circuit is unconditionally stable, because stability factor  $K > 1$ . See figure (26).



**Figure 26:** Stability factor

**Question #33(18) :**

The harmonic balance analysis allows us to calculate the power at the 1 dB compression point. In figure 27 is shown the power gain and the output power at the load. At the 1 dB compression point the input power is  $3.660\text{dBm}$  and the power at the load is  $13.627\text{dBm}$ . The result is similar to the linear power RF calculated in question #3 from the bias point ( $15.56\text{dBm}$ ).



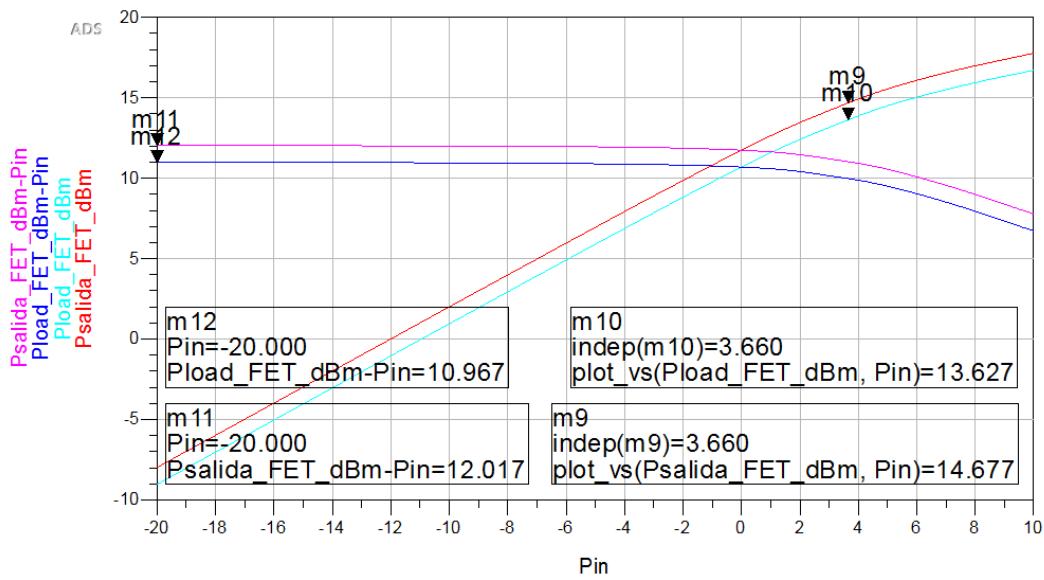
**Figure 27:** The gain and the power RF dependent on input power

### Question #34(19) :

The gain in the linear zone, as is shown in figure 27, is  $10.97dB$ . The obtained value is quite minor than the one appearing in the data-sheet ( $18.8dB$ ). However, the value is closer to the results from S-parameters simulation ( $10.971dB$ ).

### Question #35(20) :

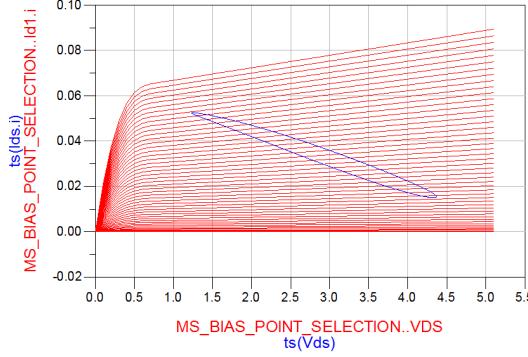
The power gain at the load ( $10.967dB$ ) is obviously lower than the power gain at the output of the transistor ( $12.017dB$ ). That is because the output of the amplifier is not matched. Furthermore, the RF power at the load ( $13.627dBm$ ) is lower than the RF power at the output of the transistor ( $14.677dBm$ ). In this case, it is produced because the input match is not perfect due to losses.



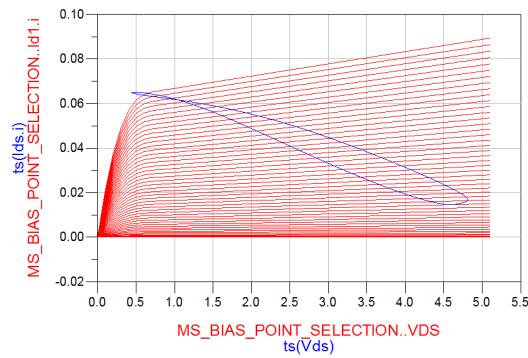
**Figure 28:** The gain and the power RF dependent on input power (load versus FET drain)

### Question #36(21) :

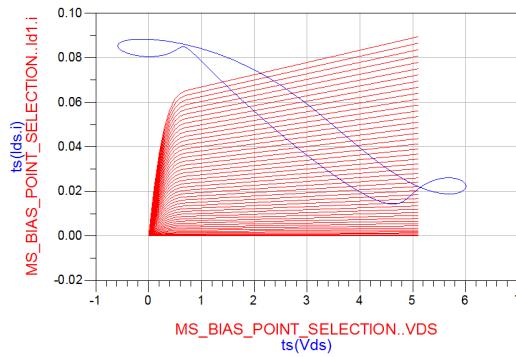
In the following figures (29),(30) and (31) are shown the dynamic load-line and the DC I-V curves of the transistor. Different input powers are applied to test the response of the amplifier in class A.



**Figure 29:** Dynamic load-line for 0 dB of input power



**Figure 30:** Dynamic load-line for P1dB of input power



**Figure 31:** Dynamic load-line for 10 dB of input power

When a 1 dB compression point is achieved, it is also achieved the full range of dynamic load-line, which has a A-class bias. When input power exceed  $P1dB$ , the transistor works out of range, with breaking risk.

#### Question #37(22) :

While the input power increase the output power get higher and gain keeps constant. Once it is achieved 1 dB compression point, the gain decrease an the output keeps getting higher in a slower

way. While input power raise, the dynamic load-line also increase voltages range.

#### Question #38(23) :

The power level of the harmonics increase as the amplifier come into a non-linear work zone, introducing signal distortion. The decoupling capacitor remark the harmonic components and DC at the input/output of the amplifier.

#### Question #39(24) :

The efficiency at 1 dB compression point is about 33.6% (the theoretical efficiency is 39.56%).

#### Question #40(25) :

The PAE applied to high-power values is lower than the efficiency because it does not consider the input power.

$$PAE = 100 * \frac{[POUT]RF - [PIN]RF}{[PDC]TOTAL} \quad (15)$$

$$\eta_{DRAIN} = 100 * \frac{[POUT]RF}{[PDC]TOTAL} \quad (16)$$

#### Question #41(26) :

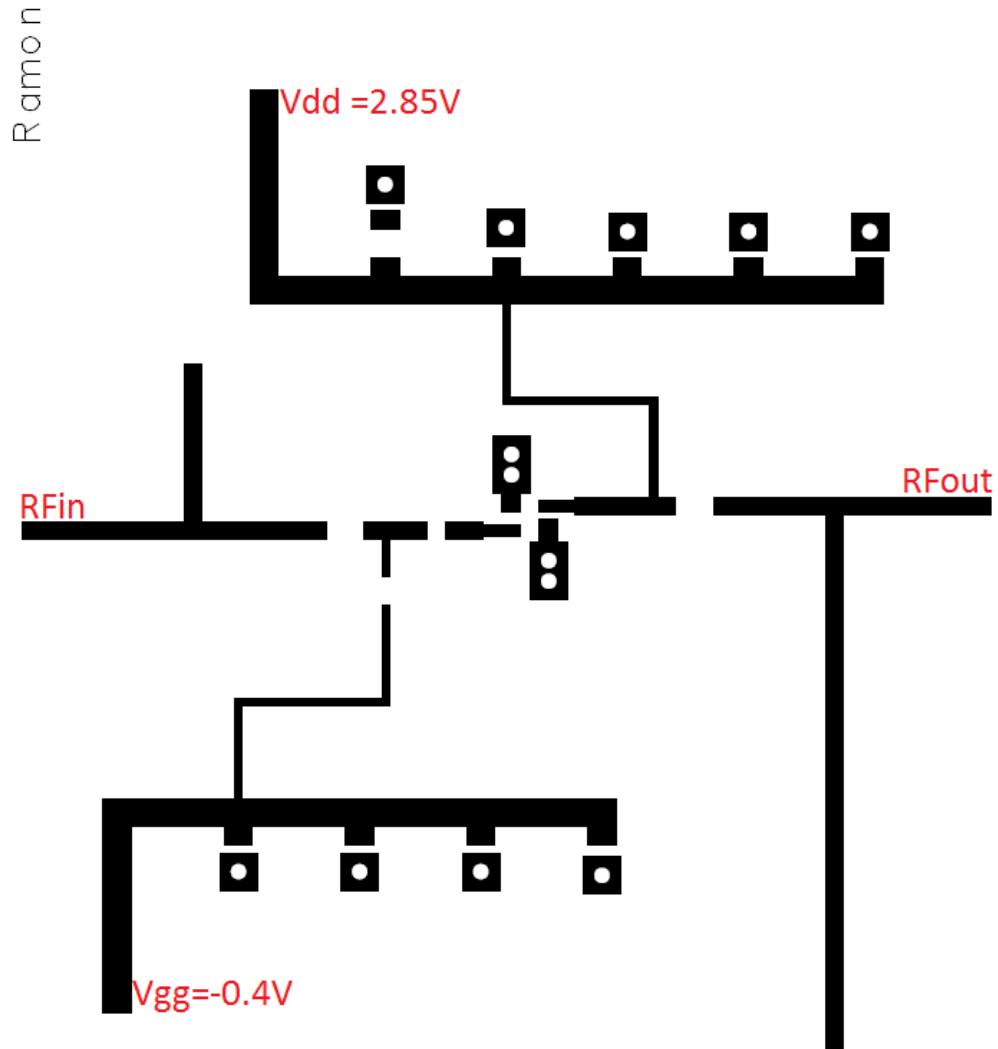
The 1 dB compression point has been calculated using the Gain-Compression simulation, obtaining the following results:

freq	inpwr	outpwr
0.0000 Hz	3.651 dBm	13.62 dBm
2.300 GHz	3.651 dBm	13.62 dBm

**Figure 32:** Gain-Compression simulation

#### Question #45 :

To generate the layout it is used the ADS option "Generate / Update Layout" and then, it had to create transistor PADs manually because there were none in the library. Below, in figure 33 is shown the layout created.



**Figure 33:** Circuit layout

## 4 EXPERIMENTAL VALIDATION

Firstly, it is checked that bias point is correct. The transistor gate is fed with  $-0.4V$  and, right away, the transistor drain is fed with  $2.85V$ .

### Question #46 :

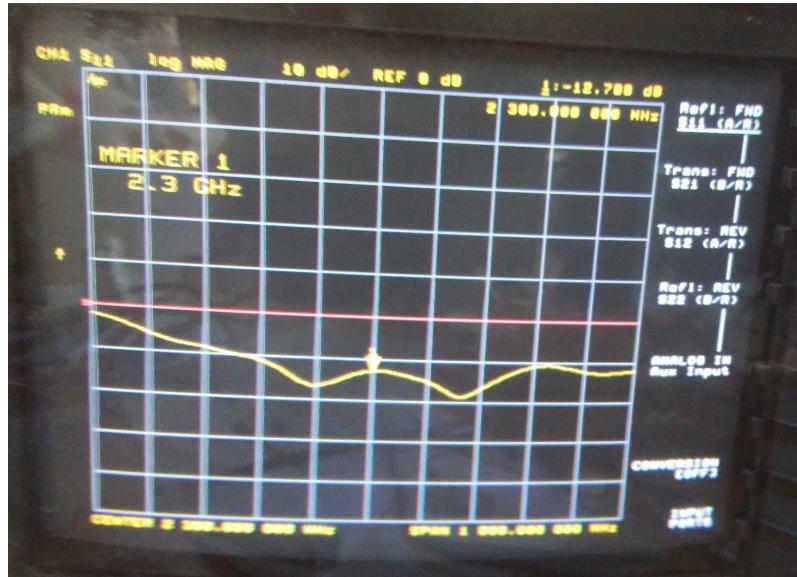
The drain current is  $60mA$ , very close to the simulated values. Apparently the transistor works fine. In the next step, the vector network analyser (VNA) is calibrated and it is put in NA mode, in order to calculate the S-parameters of the amplifier

**Question #47 :**

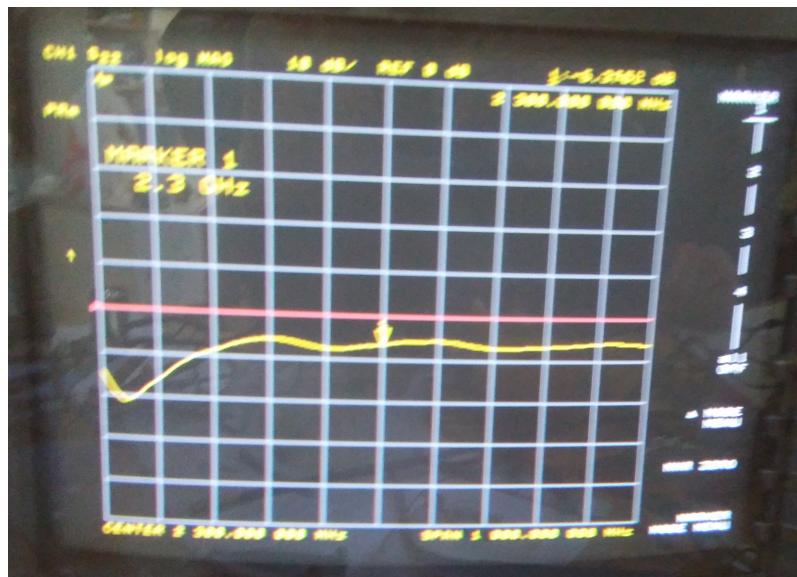
The wire has losses of  $1dB$  (approximately).

**Question #48 :**

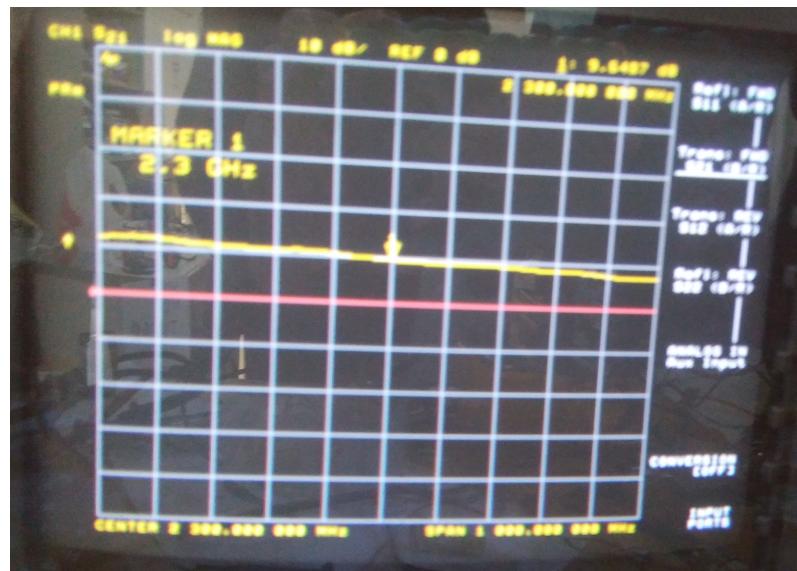
In this section power amplifier measures are included: Reflection coefficient at the input( $S_{11}$ ), reflection coefficient at the output( $S_{22}$ ), gain and power RF.



**Figure 34:** Reflection coefficient at the input( $S_{11}$ )



**Figure 35:** Reflection coefficient at the output( $S_{22}$ )



**Figure 36:** Amplifier gain( $S_{21}$ )

In the table below are summarized the most relevant results of the amplifier designed

Freq	S11	S22	Gain	P1dB	PowerRF(Pin1dB)
2.3GHz	-13 dB	-5 dB	10+1 dB	3 dBm	4+1 dBm

## 5 CONCLUSION

The implementation of this project allow me in one hand to strengthen all my knowledge about microwave circuits learnt during my master, and, in the other hand, learn, design, build and test a transceiver power amplifier.

The obtained results are not the most desired but I could achieve a practical point of view about circuits construction. That is explained because of my fault practice with the welder.