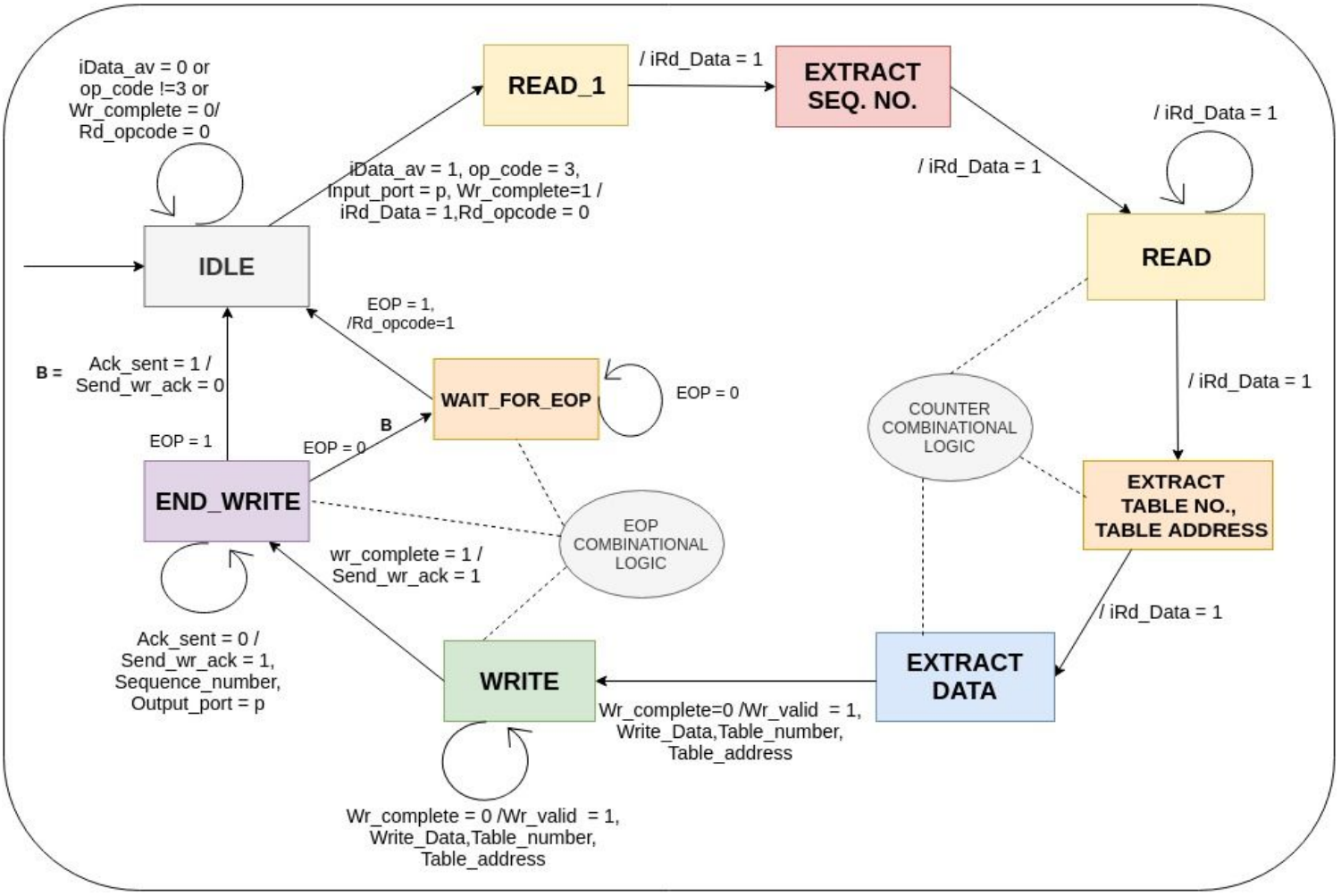
170050068 170050074 170050083 170050093 170050102

***The Designers* (U)**

Project State Diagram : Write Configuration Logic



STATES

IDLE :

Continue to be in IDLE state until iData_av becomes high and op_code becomes 3. Go to READ state once iData_av becomes high and op_code becomes 3.

READ_1 :

We start with asserting iRd_Data=1 and reading first chunk(16B) of data packet.

EXTRACT SEQ. NO. :

The second chunk of packet contains the sequence number. Extract it and store it in a signal and move to the next state.

READ :

Continue to be in this state until combinational logic returns a flag to move to the next state i.e Extract Table No. and Table Address.Table address is the first 2B (LSB) of information in the Data part of a packet.

EXTRACT TABLE NO. and ADDRESS :

Extract Table_adress, Table_number and Write_Data. Once the extraction is completed move to the EXTRACT DATA state, this transition is driven by counter combinational logic returning a specific flag.

EXTRACT DATA :

Extract the relevant data from the data part of the packet, based on the table number extracted in previous state.

Once the extraction is completed move to the WRITE state, this transition is driven by counter combinational logic returning a specific flag.

WRITE :

Continue to be in WRITE state giving out the extracted Write_Data, until the Wr_complete is driven high by the remote logic.

END_WRITE :

Once Write_complete becomes high, assert the Send_wr_ack signal and give out the Sequence_number and Output_port of the frame and wait for the Ack_sent signal to become high.

Once Ack_sent becomes '1' deassert the Send_wr_ack signal. If EOP signal is set high by the EOP combinational logic, go to the IDLE state waiting for the next packet's arrival, else go to WAIT_FOR_EOP state.

WAIT_FOR_EOP :

Wait in this state until EOP signal is driven logic high by the EOP combinational logic. Once it becomes high we make Rd_opcode logic high for one cycle and move to IDLE state.

Counter Combinational Logic :

This logic helps to move between the states as mentioned.

READ ---> EXTRACT TABLE ---> EXTRACT DATA

This logic uses N and determine the chunk containing the table number and table address and the chunks

EOP Combinational Logic:

End of packet is detected when the data validity bits out of 144 bits become zero. Once end of packet is reached it makes Rd_opcode logic high for one clock cycle. It also sets the signal EOP logic high, which means end of packet is reached.