170050068 - Assignment : **Sequence Detection**

X = “10101010111100100101001 1”

Input :

Seq : 1072 bit std_logic_vector (1000 + 24 +24 + 24)

Clk : 1 bit std_logic

Output :

Det : 1 bit std_logic (Updates for every clock cycle based on input bit).

States :

A,B,C,D,E,F,G,H,I,J,K,L,M,N,O,P,Q,R,S,T,U,V,W,X

5 bits are used to represent the states.

abcdef is a 5 bit vector

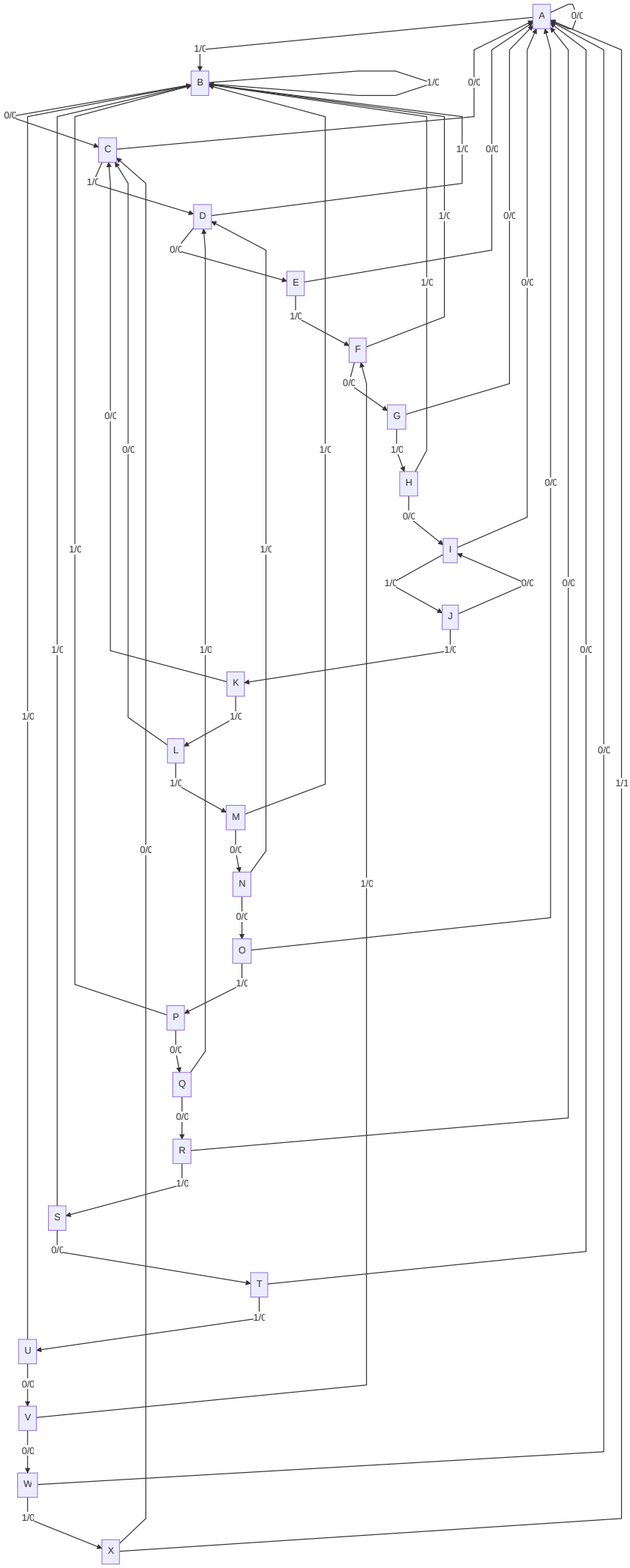
Present state	a	b	c	d	e	Input(f)	Output(Y)	Next state
A	0	0	0	0	0	0	0	A
A	0	0	0	0	0	1	0	B
B	0	0	0	0	1	0	0	C
B	0	0	0	0	1	1	0	B
C	0	0	0	1	0	0	0	A
C	0	0	0	1	0	1	0	D
D	0	0	0	1	1	0	0	E
D	0	0	0	1	1	1	0	B
E	0	0	1	0	0	0	0	A
E	0	0	1	0	0	1	0	F
F	0	0	1	0	1	0	0	G
F	0	0	1	0	1	1	0	B
G	0	0	1	1	0	0	0	A
G	0	0	1	1	0	1	0	H
H	0	0	1	1	1	0	0	I
H	0	0	1	1	1	1	0	B
I	0	1	0	0	0	0	0	A
I	0	1	0	0	0	1	0	J
J	0	1	0	0	1	0	0	I
J	0	1	0	0	1	1	0	K
K	0	1	0	1	0	0	0	C
K	0	1	0	1	0	1	0	L
L	0	1	0	1	1	0	0	C
L	0	1	0	1	1	1	0	M
M	0	1	1	0	0	0	0	N

M	0	1	1	0	0	1	0	B
N	0	1	1	0	1	0	0	O
N	0	1	1	0	1	1	0	D
O	0	1	1	1	0	0	0	A
O	0	1	1	1	0	1	0	P
P	0	1	1	1	1	0	0	Q
P	0	1	1	1	1	1	0	B
Q	1	0	0	0	0	0	0	R
Q	1	0	0	0	0	1	0	D
R	1	0	0	0	1	0	0	A
R	1	0	0	0	1	1	0	S
S	1	0	0	1	0	0	0	T
S	1	0	0	1	0	1	0	B
T	1	0	0	1	1	0	0	A
T	1	0	0	1	1	1	0	U
U	1	0	1	0	0	0	0	V
U	1	0	1	0	0	1	0	B
V	1	0	1	0	1	0	0	W
V	1	0	1	0	1	1	0	F
W	1	0	1	1	0	0	0	A
W	1	0	1	1	0	1	0	X
X	1	0	1	1	1	0	0	C
X	1	0	1	1	1	1	0	A

State Equations:

Y(t+1) = acdef
a(t+1) = ac'e'f' + ac'ef + ad'ef + acd'f' + bcdef' + acde'f
b(t+1) = bc'f + bc'd'e + bde'f + bcd'f' + a'b'cdef'
c(t+1) = cd'ef' + cde'f + bcd'f' + acd'f' + acd'e + a'b'ce'f + bc'def + ac'def + a'b'c'def'
d(t+1) = a'de'f + cd'ef' + cde'f + bd'ef + bc'df' + ac'd'f + ad'ef + acef' + a'b'd'ef' + ac'de'f'
e(t+1) = e'f + a'b'f + a'cf + ac'e' + ad'e' + bcd'e'

State Diagram:


A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
V
W
X
1/C
O/C
1/1