170050068 170050074 170050083 170050093 170050102

THE DESIGNERS(U)- Assignment - 4

DESCRIPTION:

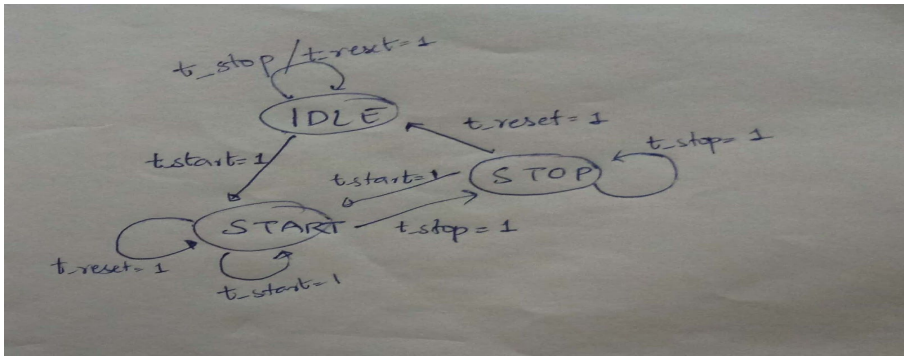
INPUT : Three inputs (t_start) ,(t_stop) and (t_reset) are 1 bit binary .
OUTPUT : (time_ms) := 8 bit bus.
And 100MHz clock as input.

- Built a state machine (state diagram shown below)with the states as IDLE,START and STOP (encoding shown below).
- Generated a 1ms clock from 10 ns clock by maintaining a counter.
- Used above1 ms clock to synchronize the output of the stopwatch.
- Used four seperate proccesses for FSM synchronizer logic, FSM combinational logic, 1ms clock logic and stopwatch logic.

STATE ENCODING(As generated by synthesis report ***):***

```
------------------
 State | Encoding
------------------
 idle  | 00
 start | 01
 stop  | 10
------------------
```

STATE DIAGRAM:



TIMING DIAGRAM: