

**The Designers**  
**Assignment 2 Report**

**COMPONENTS:**

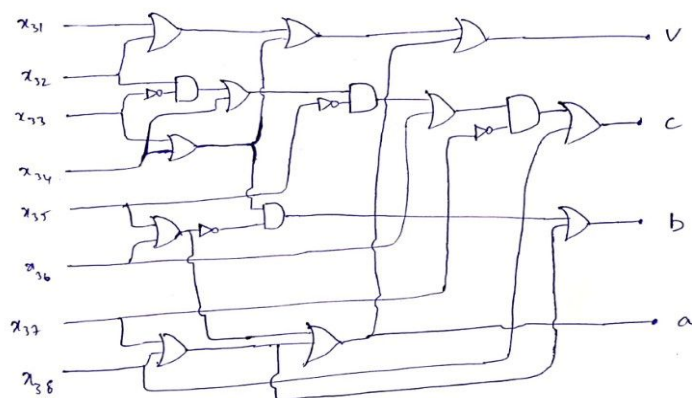
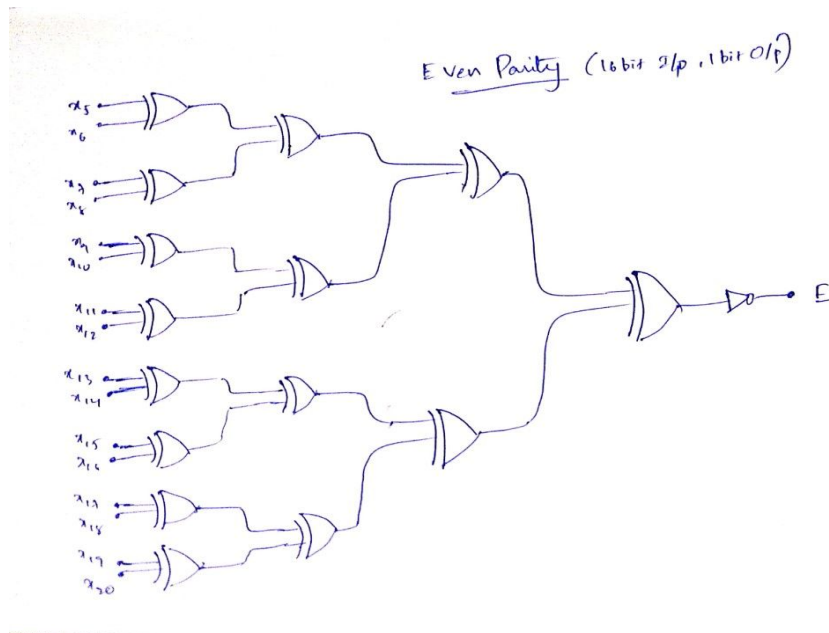
16 bit comparator, 16 bit even parity, (6 by 3) multiplexer, 1 bit full adder, 8 bit priority encoder

**DESCRIPTION:**

INPUT : (x) := 38 bit bus and (Sel) := 3 bit bus

OUTPUT : (O2) := 4 bit bus and (O1) := 1 bit binary.

- 16 bit Even Parity : 15 XOR gates and 1 NOT gate.
- 1 bit Full adder : 2 XOR gates, 2 AND gates and 1 OR gate
- 8 bit Priority Encoder : 11 OR gates, 4 AND gates and 4 NOT gates
- 16 bit comparator : 287 AND gates, 46 OR gates and 64 NOT gates
- 6 by 3 multiplexer : 15 AND gates, 5 OR gates and 3 NOT gates



*Priority Encoder (8 bit i/p, 4 bit o/p)*