170050068 170050074 170050083 170050093 170050102
The Designers

Assignment 3 Report

COMPONENTS:

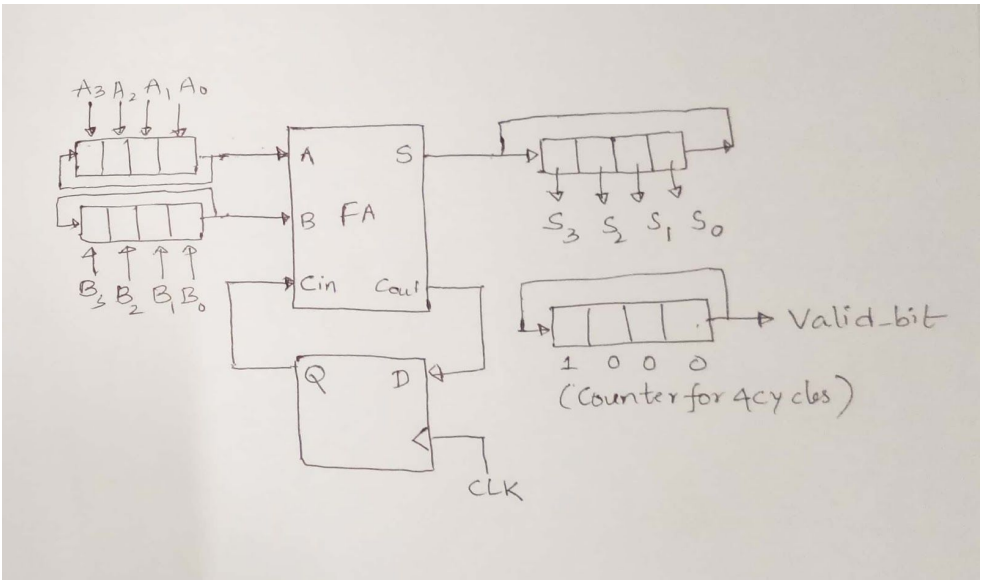
Four registers (16 FlipFlops) + 1 FlipFlop

DESCRIPTION:

INPUT : (A) := 4 bit bus and (B) := 4 bit bus and (add) := 1 bit binary
OUTPUT : (sum) := 4 bit bus and (carry) := 1 bit binary and (sum_valid) := 1 bit binary.

2 inputs - 4 bit shift registers for storing A and B.
1 output - 4 bit shift register for storing sum.
1 four bit shift register to keep the track of number of bits added and to make sum_valid to output 1 after the completion.
1 Flipflop to store the carry at every round and to propagate it to the next round.

SIMPLIFIED CIRCUIT:



Delay:

1 clock cycle : 10 ns
Total delay : 50 ns (1 cycle for reading input into registers and 4 cycles to calculate the sum)