**Lab Assignment**: Aribiter

We have a 4 queue arbiter.

Each queue is 200 bits capacity.

Packets arrive randomly of length 8 bits to 24 bits and fill up a queue. Each packet arrives sequentially (one-bit at a time).

We have a sum function that connects all 4 queues to an output

If the queue gets full you have to drop the entire last packet that enters the queue

You have to count the number of packets dropped

Design an arbiter that is (a) round robin and (b) deficit round robin.

Design test-bench and test the RR and DRR.

Assume that the arbiter runs at 200MHz, while each queue is getting packets at 50MHz.

Calculate cycle time

**At home:**

Part 2:

Now code DRR algorithm

You have to maintain quantum and deficit as two register values in addition to buffer.

In each cycle you can send max data of quantum.

If some extra data remains, then it can be sent if you have excess deficit.

Read the paper:

<https://ieeexplore.ieee.org/document/502236>

Subsequently assume that the 4 channels are generating data at rates of 20, 30, 40 and 10 Mbps.

Now design the system.

Calculate average delay.

Packet size is max 250 bytes.

Show result via test-bench.