Assignment#1- Lab1

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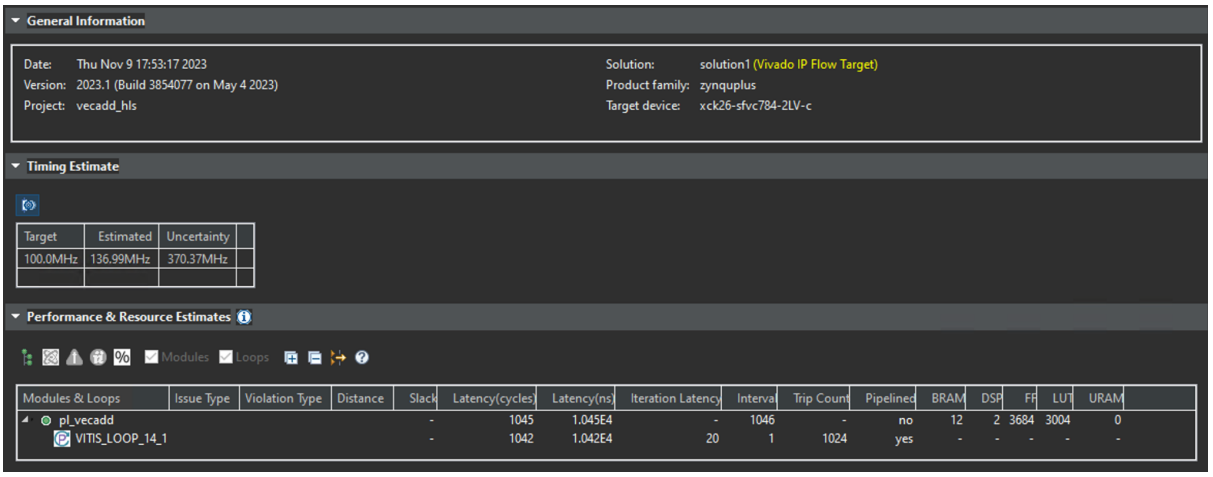
Part I: Vector Addition Example

* Code (Vitis HLS)

```
#include "ap_int.h"
#include "ap_fixed.h"
#include "hls_math.h"
void pl_vecadd(float a[1024], float b[1024], float c[1024])
{
  #pragma HLS INTERFACE m_axi port=a offset=slave bundle=data0
  #pragma HLS INTERFACE s_axilite register port=a bundle=ctrl
  #pragma HLS INTERFACE m_axi port=b offset=slave bundle=data1
  #pragma HLS INTERFACE s_axilite register port=b bundle=ctrl
  #pragma HLS INTERFACE m_axi port=c offset=slave bundle=data2
  #pragma HLS INTERFACE s_axilite register port=c bundle=ctrl
  #pragma HLS INTERFACE s_axilite register port=return bundle=ctrl
  for (int i = 0; i < 1024; i += 1)
  {
    #pragma HLS pipeline
    c[i] = a[i] + b[i];
  }
}
```

* Synthesis Summary report (Vitis HLS)



General Information

Date: Thu Nov 9 17:53:17 2023
Version: 2023.1 (Build 3854077 on May 4 2023)
Project: vecadd_hls
Solution: solution1 (Vivado IP Flow Target)
Product family: zynquplus
Target device: xck26-sfvc784-2LV-c

Timing Estimate

Target	Estimated	Uncertainty
100.0MHz	136.99MHz	370.37MHz

Performance & Resource Estimates

Modules Loops

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
pl_vecadd				-	1045	1.045E4	-	1046	-	no	12	2	3684	3004	0
VITIS_LOOP_14_1				-	1042	1.042E4	20	1	1024	yes	-	-	-	-	-

* Report utilization (Vivado)

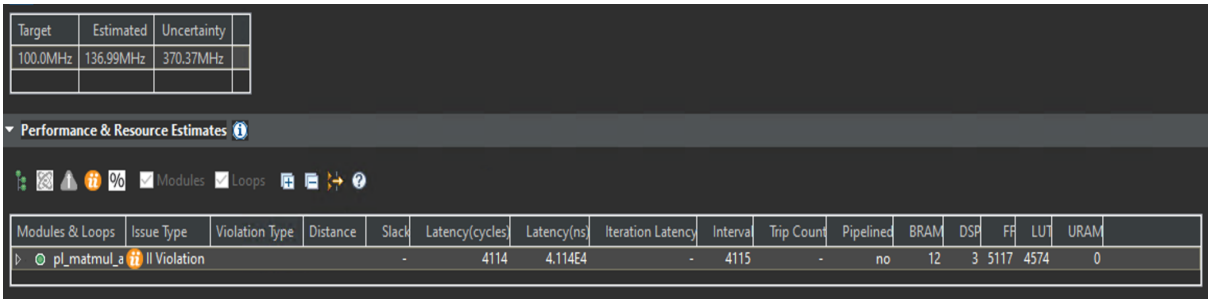
Name	CLB LUTs (117120)	CLB Registers (234240)	CARRY8 (14640)	F7 Muxes (58560)	CLB (14640)	LUT as Logic (117120)	LUT as Memory (57600)	Block RAM Tile (144)	DSPs (1248)	GLOBAL CLOCK BUFFERs (352)	PS8 (1)
design_1_jp_wrapper	4020	5450	97	2	877	3269	751	1.5	2	2	1
design_1_jp_i (design_1_jp)	4020	5450	97	2	877	3269	751	1.5	2	2	1
axi_smc (design_1_jp_axi_s	368	349	0	0	71	200	168	0	0	0	0
axi_smc_1 (design_1_jp_ax	367	349	0	0	73	199	168	0	0	0	0
axi_smc_2 (design_1_jp_ax	414	554	0	0	88	247	167	0	0	0	0
pl_vecadd_0 (design_1_jp_	1869	3183	97	0	499	1703	166	1.5	2	0	0
ps8_0_axi_periph (design_	994	981	0	2	203	913	81	0	0	0	0
rst_ps8_0_96M (design_1_j	14	34	0	0	7	13	1	0	0	1	0
zynq_ultra_ps_e_0 (design_	0	0	0	0	0	0	0	0	0	1	1

Part II: Matrix Multiplication - (a) a plain version without any HLS pragmas

* Code (Vitis HLS)

```
#include "ap_int.h"
#include "ap_fixed.h"
#include "hls_math.h"
void pl_matmul_a(int A[16][16], int B[16][16], int AB[16][16])
{
  int M = 16;
  int K = 16;
  int N = 16;
  #pragma HLS INTERFACE m_axi port=A offset=slave bundle=data0
  #pragma HLS INTERFACE s_axilite register port=A bundle=ctrl
  #pragma HLS INTERFACE m_axi port=B offset=slave bundle=data1
  #pragma HLS INTERFACE s_axilite register port=B bundle=ctrl
  #pragma HLS INTERFACE m_axi port=AB offset=slave bundle=data2
  #pragma HLS INTERFACE s_axilite register port=AB bundle=ctrl
  #pragma HLS INTERFACE s_axilite register port=return bundle=ctrl
  for(int i = 0; i < M; ++i)
  {for(int j = 0; j < N; ++j)
                {
                        int ABij = 0;
                        for(int k= 0; k < K; ++k)
                        {
                                ABij += A[i][k] * B[k][j];
                        }
                        AB[i][j] = ABij;
                }
  }
}
```

* Synthesis Summary report (Vitis HLS)



Target	Estimated	Uncertainty
100.0MHz	136.99MHz	370.37MHz

Performance & Resource Estimates

Modules Loops

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interva	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
pl_matmul_a	II Violation			-	4114	4.114E4	-	4115	-	no	12	3	5117	4574	0

* Report utilization (Vivado)

Name	CLB LUTs (117120)	CLB Registers (234240)	CARRY8 (14640)	F7 Muxes (58560)	CLB (14640)	LUT as Logic (117120)	LUT as Memory (57600)	Block RAM Tile (144)	DSPs (1248)	GLOBAL CLOCK BUFFERs (352)	PS8 (1)
design_1_wrapper	4943	7639	241	2	1154	4196	747	1.5	3	2	1
design_1_i (design_1)	4943	7639	241	2	1154	4196	747	1.5	3	2	1
axi_smc (design_1_	413	501	0	0	95	245	168	0	0	0	0
axi_smc_1 (design_	412	501	0	0	104	244	168	0	0	0	0
axi_smc_2 (design_	462	706	0	0	106	295	167	0	0	0	0
pl_matmul_a_0 (des	2661	4916	241	0	759	2499	162	1.5	3	0	0
ps8_0_axi_periph (d	983	981	0	2	187	902	81	0	0	0	0
rst_ps8_0_99M (des	15	34	0	0	6	14	1	0	0	1	0
zynq_ultra_ps_e_0 (	0	0	0	0	0	0	0	0	0	1	1

Part II: Matrix Multiplication - (b)
an optimized version that uses ARRAY_PARTITION and PIPELINE pragrmas

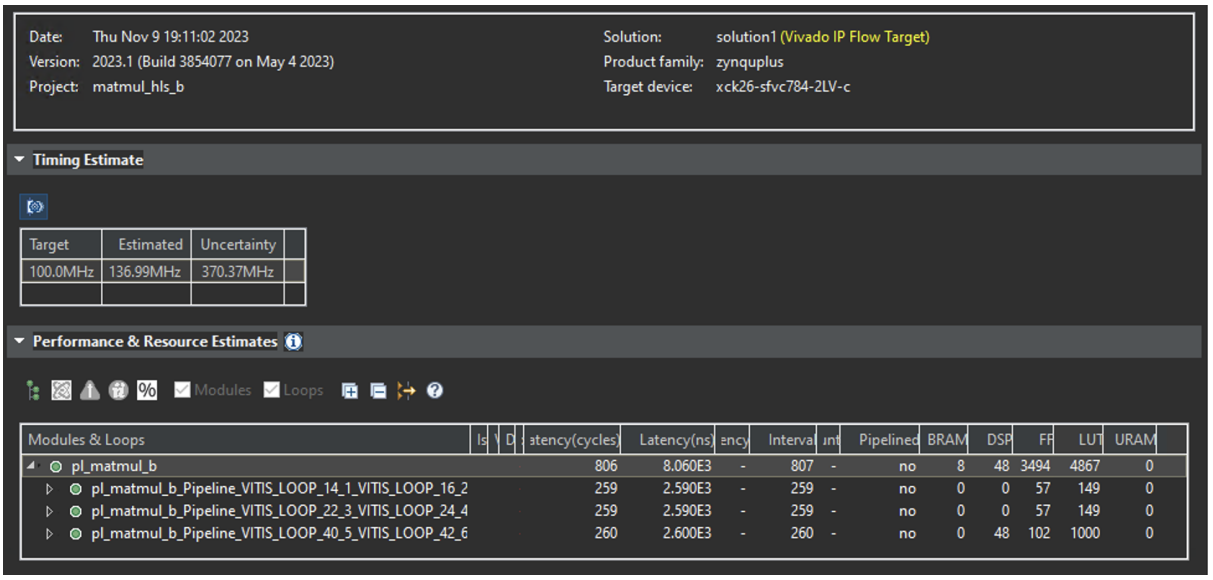
* Code (Vitis HLS)

```
#include "ap_int.h"
#include "ap_fixed.h"
#include "hls_math.h"
void pl_matmul_b(int A[16][16], int B[16][16], int AB[16][16])
{
  int M = 16;
  int K = 16;
  int N = 16;

// local buffer array
  int A_buff[16][16];
  int B_buff[16][16];

// assign the values of A and B into buffer variable
        for(int i= 0 ; i < 16; ++i)
        {
          for(int j = 0; j < 16; ++j)
          {
            A_buff[i][j] = A[i][j];
          }
        }
        for(int i = 0; i < 16; ++i)
        {
          for(int j = 0; j < 16; ++j)
          {
            B_buff[i][j] = A[i][j];
          }
        }
  #pragma HLS INTERFACE m_axi port=A offset=slave bundle=data0
  #pragma HLS INTERFACE s_axilite register port=A bundle=ctrl
  #pragma HLS INTERFACE m_axi port=B offset=slave bundle=data1
  #pragma HLS INTERFACE s_axilite register port=B bundle=ctrl
  #pragma HLS INTERFACE m_axi port=AB offset=slave bundle=data2
  #pragma HLS INTERFACE s_axilite register port=AB bundle=ctrl
  #pragma HLS INTERFACE s_axilite register port=return bundle=ctrl
  #pragma HLS ARRAY_PARTITION variable=A_buff complete dim=2
  #pragma HLS ARRAY_PARTITION variable=B_buff complete dim=1
  for(int i = 0; i < M; ++i)
  {
      for(int j = 0; j < N; ++j)
              {
          #pragma HLS PIPELINE II=1
                        int ABij = 0;
                        for(int k= 0; k < K; ++k)
                        {
                                ABij += A_buff[i][k] * B_buff[k][j];
                        }
                        AB[i][j] = ABij;
              }
  }
}
```

* Synthesis Summary report (Vitis HLS)



Date: Thu Nov 9 19:11:02 2023
Version: 2023.1 (Build 3854077 on May 4 2023)
Project: matmul_hls_b

Solution: solution1 (Vivado IP Flow Target)
Product family: zynquplus
Target device: xck26-sfvc784-2LV-c

Timing Estimate

Target	Estimated	Uncertainty
100.0MHz	136.99MHz	370.37MHz

Performance & Resource Estimates

Modules Loops

Modules & Loops	Latency(cycles)	Latency(ns)	Interval	Pipelined	BRAM	DSP	FF	LUT	URAM
pl_matmul_b	806	8.060E3	- 807	- no	8	48	3494	4867	0
pl_matmul_b_Pipeline_VITIS_LOOP_14_1_VITIS_LOOP_16_2	259	2.590E3	- 259	- no	0	0	57	149	0
pl_matmul_b_Pipeline_VITIS_LOOP_22_3_VITIS_LOOP_24_4	259	2.590E3	- 259	- no	0	0	57	149	0
pl_matmul_b_Pipeline_VITIS_LOOP_40_5_VITIS_LOOP_42_6	260	2.600E3	- 260	- no	0	48	102	1000	0

* Report utilization (Vivado)

Name	CLB LUTs (117120)	CLB Registers (234240)	CARRY8 (14640)	F7 Muxes (58560)	CLB (14640)	LUT as Logic (117120)	LUT as Memory (57600)	Block RAM Tile (144)	DSPs (1248)	GLOBAL CLOCK BUFFERs (352)	PS8 (1)
design_1_wrapper	4607	4901	122	2	925	3477	1130	1	48	2	1
design_1_i (design_1)	4607	4901	122	2	925	3477	1130	1	48	2	1
axi_smc (design_1_a	413	501	0	0	96	245	168	0	0	0	0
axi_smc_1 (design_1	189	182	0	0	44	116	73	0	0	0	0
axi_smc_2 (design_1	461	706	0	0	105	294	167	0	0	0	0
pl_matmul_b_0 (desi	2546	2497	122	0	534	1906	640	1	48	0	0
ps8_0_axi_periph (de	987	981	0	2	188	906	81	0	0	0	0
rst_ps8_0_99M (desig	14	34	0	0	9	13	1	0	0	1	0
zynq_ultra_ps_e_0 (d	0	0	0	0	0	0	0	0	0	1	1