**Sathish**

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## Technical Skills:

### Verilog, System Verilog, UVM, C/C++, Python, Perl Scripting.

* **Questa Sim, Cadence, Xilinx Linux & GVIM** Editing tools.

# Profile Summary:

### Total 6 years 5 months as a Design & Verification Engineer.

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* Experience in **SOC And IP Verification.**
* Knowledge on **Verilog**
* Proficient in (**SV**) **System Verilog**.
* Hands on experience on (**UVM**) **Universal Verification Methodology.**
* Skilled in Handling **Simulation Tools**
* Hands on experience in **TB Architecture development**
* Hands on **Experience on Debugging Testbench.**
* Good Understanding on **Python, C++** Languages.
* High Speed Protocol Knowledge **USB 3.0**
* High Speed Protocol Knowledge **JTAG**
* Proficient in **APB & AXI** protocol.
* Good Knowledge in **GLS.**
* Serial Protocol Knowledge **I2C &SPI**
* Experienced in developing **Test Bench Components**.
* Writing **Test Cases** & **Coverage driven Verification.**
* Worked on **Linux terminal,**

# Work Experience: 6 Years 4 months

* Currently Working with **Lancesoft India pvt ltd** (**From** 17th June 2024 to Till Date)
* Worked as a **Senior Verification Engineer** in **Capgemini** Hyderabad (**From** 22nd Aug 2022 to 03rd Aug 2023)
* Worked as **Senior** **Design and Verification Engineer** in **Tech Mahindra (Cerium Systems)**, Bangalore (**From** 05th Oct-2020 **To** 22nd July-2022)
* Worked as **Design and Verification Engineer** in **Adept Chips Services PVT Ltd**, Bangalore (**From** 08th Oct-2016 **To** 24th Sep-2019)

**PROJECT 1: Kracken**

**Description:**

Kracken is a monolithic die. The architecture is based on utilization of wafer level fan out technology, which consists of single IOD chiplet and CCD chiplet with 8 GPU cores and memory support of LPDDR5X. Design focus on CPU and GPU performance, Battery life, idle mode use cases.

**Roles and Responsibilities:**

* + Understand the JTAG and BSCAN specifications.
  + Understanding the chain order.
  + Running testcases and debugging.
  + Generating BSDL, Testbench and Tests.
  + Running regression in local as well CRDB.
  + Debug of waveform using Verdi.

**Tools &Language used:** Synopsys VCS, Verdi simulator, Cpp, perl

**PROJECT 2: CWF (GLS)**

**Description:**

CWF is a test chip, it is a part server chip.

**Roles and Responsibilities:**

* Contributed to project involving RTL simulations, and GLS simulations
* Conducted X-propagation, functional, and SDF debug.
* Working with Junior Engineers and assigning basic tasks.

**Tools &Language used:** Synopsys VCS & Verilog and system Verilog.

**PROJECT 3: GTCHE\_Project (Graphics Technology, Intel)**

**Description:**

Product Development - HW Valid & Tools - Pre-Silicon HW Verification &Validation. Working on Graphics & Throughput Computing Hardware Engineering Project (GTCHE) which is delivering industry-leading GPU (3D, media, compute, and display) hardware intellectual property (IP) blocks and system-on-a-chip (SoC) products for discrete graphics and throughput computing. Working on GPU 3D and compute pipeline. Responsible for Functional Pre-Silicon Verification of next gen graphics features, Intel discrete and integrated GPU’s.

**Role & Responsibilities:**

* Understanding the Graphics Verification of GPU's.
* Managed weekly regression, triaged failures
* Functional debugging of regression failures and working with design and architecture teams to fix the issues.

**Tools &Language used:** ATS Tool and Zebu Tool (Emulation Project).

**PROJECT 4: Leonardo Industrial camara**

**Description:**

The Leonardo project is about high-performance industrial cameras with a large choice of sensors, modular options and built-in image optimization. This ASIC majorly consists of CPU sub system, front-end interface, IPL unit and back-end interface. Front end interface consists of Sensor, PixMix and Sensor controller. IPL unit consists of Image pre-processing and Pipelining. The backend interface consists of various interfaces such as MIPI, PCI and USB.

**Role & Responsibilities:**

* Worked on backend interface**-USB.**
* Responsible for verification (Debugging of failure test cases, code coverage) of UVC. (USB3 Vision top level verification).
* Responsible for regression of USB (UVC) module, Code coverage improvement and achieved 95% code coverage.

**Tools &Language used:** Cadence NcSim, Simvision, SV, UVM, C language**.**

**PROJECT 5: DMA Ip Level Verification**

**Description:**

Direct Memory Access uses hardware for accessing the memory, that hardware is called a DMA Controller. It has the work of transferring the data between Input Output devices and main memory with very less interaction with the processor. The direct Memory Access Controller is a control unit, which has the work of transferring data.

# Role & Responsibilities:

* + - Listed down DMA features and test plan for validating DMA.
    - Written sequences and Test Cases to verify the functionalities listed in the feature Extraction list.
    - Worked on developing environment on sequencer, driver, monitor components
    - Worked on coverage driven implementation.
    - Worked on constrained random verification (CRV) to explore corner cases.
    - Collaborated with design engineers to resolve bugs.

**Tools &Language used:** Cadence 64-bit ncsim, imc, Vmanger, Sim Vision**.**

**PROJECT 6: I2c Bus Master**

**Description:**

I2C stands for inter-integrated circuit. It is a bus interface connection protocol incorporated into devices for serial communication. I2C combines the features of SPI and UARTs. With I2C, you can connect multiple slaves to a single master (like SPI) and you can have multiple masters controlling signal or multislaves. This is useful when you want to have more than one microcontroller logging data to a single memory card or displaying test to a single LCD.

**Role & Responsibilities:**

* Running test cases and debugging.
* Running regressions in vmanager.
* Involved in developing scoreboard part from the scratch
* Involving functional coverage.
* Writing directed test cases from the spec and to reach 100% coverage.
* Verifying the masters by using slave here we are using single master and single slave environment.
* Developing the test component in that we are writing all test cases.
* Debugging using waveforms in simvision.
* Writing seq\_item and implementing monitor and driver.

**Tools &Language used:** Cadence 64-bit ncsim, imc, Vmanger, Sim Vision**.**

**PROJECT 7: SPI Bus Master**

**Description :**

The Serial Peripheral Interface (SPI) bus was developed by Motorola to provide full-duplex synchronous serial communication between master and slave devices. The SPI bus is commonly used for communication with flash memory, sensors, real-time clocks (RTCs), analog-to-digital converters, and more. **S**erial **P**eripheral **I**nterface, or **SPI**, is a very common communication protocol used for two-way communication between two devices.

**Role & Responsibilities:**

* Responsible for design verification of SPI Master Interface.
* Developed UVM components like sequencer, driver, monitor, agents and environment.
* Written the read and write test cases.

**Tools &Language used:** Cadence 64-bit ncsim, imc, Vmanger, Sim Vision**.**

**PROJECT 8: AXI VIP - AMBA AXI 3&AXI 4 Protocol**

**Description:**

AXI4 is a family of buses defined as part of the fourth generation of the ARM Advanced Microcontroller Bus Architecture (AMBA) standard. AXI Protocol is targeted at high-performance memory mapped data and address interface, high-frequency system and includes a few features that make it suitable for a high- speed submicron interconnect.

**Role & Responsibilities:**

* Understood the AMBA AXI specification.
* Running test cases and debugging.
* Running regressions in vmanager.
* Involved in developing scoreboard part from the scratch
* Involving functional coverage.
* Writing directed test cases from the spec and to reach 100% coverage.
* Verifying the masters by using slave here we are using single master and single slave environment.
* Developing the test component in that we are writing all test cases.
* Debugging using waveforms in simvision.
* Writing seq\_item and implementing monitor and driver.

**Tools &Language used:** Cadence 64-bit ncsim, imc, Vmanger, Sim Vision.

**PROJECT 9: APB VIP - AMBA APB Protocol**

**Description:**

AMBA APB addresses the requirements of high- performance synthesizable designs. It is a bus interface that supports a single bus master and provides high- band width operation.

**Role & Responsibilities:**

* Understood the AMBA, APB specification.
* Running test cases and debugging.
* Running regressions in vmanager.
* Involved in developing scoreboard part from the scratch
* Involving functional coverage.
* Writing directed test cases from the spec and to reach 100% coverage.
* Verifying the masters by using slave here we are using single master and single slave environment.
* Developing the test component in that we are writing all test cases.
* Debugging using waveforms in simvision.
* Writing seq\_item and implementing monitor and driver.

**Tools &Language used:** Cadence 64-bit ncsim, imc, Vmanger, Sim Vision.

**Education Profile:**

* **M. Tech : VLSI** , in Hyderabad, JNTUH
* **B. Tech : EEE,** in Karimnagar JNTUH

**Declaration:** I hereby declare that all the information provided above is accurate to the best of my knowledge.

### Date:

**Hyderabad Sathish.V** 