

Ram Srivatsa Kannan

Systems Researcher,
Aspiring System Architect



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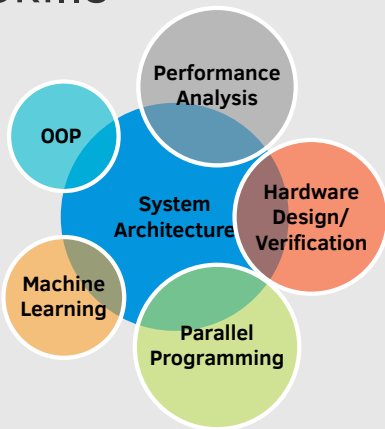


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Skills



Interests

Datacenter Design

Cloud Computing

Virtualization & OS

Software Development

Computer Architecture

Courses

Systems

Computer Architecture
Advanced Compilers
Parallel Architectures
Microarchitecture
Operating Systems

PL

Data Structures
Algorithms
Embedded Systems
OOP

Misc

AI
Probability
Statistics

Education

2013 - 2018

(Expected)

Ph.D. Computer Science

Ann Arbor, Michigan, USA

*Thesis: Enabling Fairness in
Cloud Computing Infrastructures*

University of Michigan

2009 - 2013

B.Tech Information Technology

Madras, Tamil Nadu, India

*Thesis: SCOC IP design for
Application Specific Architectures*

Anna University

Experience

Fall '13

– now

Graduate Research Assistant

University of Michigan, Ann Arbor

- **Proctor: Identifying Interference in Shared datacenters** - Designed a real-time technique for identifying problematic VMs and its root causes in hyper-converged datacenters that executes CPU, Network and I/O intensive applications.
- **Caliper: Interference Estimator for Multi-tenant Environments Sharing Architectural Resources** - Designed a runtime system to estimate performance degradation of applications running in public clouds and to price users accordingly.
- **GrandSLam – Guaranteeing Datacenter SLAs for Microservices executing in Serverless Computing Infrastructures** - Designed a runtime system to guarantee SLAs among applications utilizing microservers in a serverless computing platform. Implemented DNN based machine learning algorithms in serverless framework using tensorflow on docker containers for this purposes.
- **Big Data analytics on GPUs** - Implemented parallel versions of common data analytics queries and compared it with parallel pthreads versions of the queries in terms of performance. Performed a characterization study of how different input formats of data would affect the performance of queries.
- **Prophet: Precise QoS Prediction on Non-Preemptive Accelerators to Improve Utilization in Warehouse Scale Computers** - Collaborated towards building a GPU based datacenter which guarantees Quality-of-Service for latency-sensitive applications for the state of the art web service applications.
- **Tail-Sniping: Tail Latency Troubleshooting Using Causal Inference** - Collaborated towards building a runtime system to detect performance anomalies using microarchitectural resources and to perform causal analysis with them.

Summer '18

Research Intern – VMware Research

VMware Inc.

Worked on a compiler infrastructure that optimizes the compilation times of Verilog in FPGA. Worked on a real time static compiler/scheduler that schedules independent modules present in a Verilog codebase in an optimal order such that emulation time is reduced.

Summer '16

Research Intern – Performance Engineering

VMware Inc.

Worked on real-time, scalable analytics platform which we could automatically detect antagonistic VM behaviors in co-located environments caused due to disk contention using real time system telemetry. Using our technique we were able to identify performance issues and increase individual VM performance by up to 2.5× and 1.8×, on an average.

Tools



TensorFlow Keras Pandas Numpy Lucida



Matplotlib Excel gnuplot Plotly \LaTeX



MySQL Elastic-Search Hadoop Spark Storm

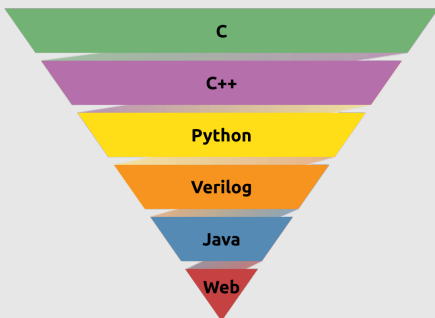


perfmon esxtop io-analyzer netperf



git tmux AWS kvm esxi linux unix

Languages



Hobbies



Winter '18,
Fall '16, '15

Graduate Student Instructor

- EECS 483 – Compiler Construction
- EECS 280 – Programming and Data Structures
- EECS 583 – Advanced Compilers

University of Michigan

Fall '10 –
Summer '13

Research Trainee

Waran Research Foundation (WARFT), India

- Worked in the high performance computer architecture group that is focused in designing CUsm Built hETerogeneous Multi-coreArCHitecture - CUBEMACH a node architecture for future generation supercomputing clusters
- Worked on a model for a supercomputing cluster which deals with solving problems in areas like astrophysics, biological sciences, brain modelling and environmental modelling which in future requires high computational power in the range of exa flops.

other projects

Compilers

Loop Invariant Code Motion

Implemented Loop Invariant code motion using an LLVM pass.

Comp Arch

Design and Implementation of Out of order processor

Part of a team which designed and implemented a 2-way superscalar out of order processor in Verilog. It performs out of order execution with Tomasulo's algorithm. It contains additional features like Load Store Queue, tournament branch predictor, return address stack, unified reservation station.

Parallel Comp Arch

Verified MSI and implemented self downgrade optimization

Verified MSI protocol using a popular tool Murphi. Implemented self downgrade optimization in the existing MSI protocol.

publications

- **Proctor: Identifying Interference in Shared datacenters**, Ram Srivatsa Kannan, Animesh Jain, Michael Laurenzano, Jason Mars, Lingjia Tang, International Symposium on Performance Analysis of Systems and Software (ISPASS-18), April 2018
- **GrandSLam - Guaranteeing SLAs for Microservices executing in Serverless Computing Infrastructures**, Ram Srivatsa Kannan, Lavanya Subramanian, Ashwin Raju, Jeongseob Ahn, Jason Mars, Lingjia Tang, European Conference on Computer Systems (Eurosys-19), March 2019
- **Caliper: Interference Estimator for Multi-tenant Environments Sharing Architectural Resource**, Ram Srivatsa Kannan, Michael Laurenzano, Jeongseob Ahn, Jason Mars, Lingjia Tang, ACM Transactions on Architecture and Code Optimization (TACO), Accepted
- **Prophet: Precise QoS Prediction on Non-Preemptive Accelerators to Improve Utilization in Warehouse Scale Computers**, Quan Chen, Hailong Yang, Minyi Guo, Ram Srivatsa Kannan, Jason Mars, Lingjia Tang, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-17), April 2017
- **Compilation Accelerator on Silicon**, Venkateswaran Nagarajan, Ram Srivatsa Kannan et.al., published in the proceedings of 11th IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2012, University of Massachusetts, Amherst
- **SCOC IP Cores for Custom Built Supercomputing Nodes**, Venkateswaran Nagarajan, Ram Srivatsa Kannan et.al., published in the proceedings of 11th IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2012, University of Massachusetts, Amherst