

LAB ASSIGNMENT

Demonstration of CMOS NOR2 gate design using Silvaco's EDA Tools

Submitted By:

BATCH 4

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VLSI Design Lab



Gateway

Schematic Editor

Gateway supports flat or hierarchical designs of any technology. Gateway readily accepts legacy designs from other schematic editors through the EDIF 2 0 0 standard. Gateway can be used by large design teams through global preferences and handles multiple designs and technologies with specific workspaces.

Key Features

- Powerful schematic capture and editor functionality to create and modify multi-view, multi-sheet, hierarchical IC designs.
- Gateway Views is licensed at no cost for only viewing and navigating schematic designs
- Seamless integration with Smart Spice Circuit Simulator that creates an interactive design environment with behavioral models, cross-probing, waveform display, and analysis
- Create HSPICE compatible input decks
- Controls multi-user projects with shared work spaces for libraries of cells and symbols used by the design team
- Transition from other schematic capture tools via EDIF 2 0 0
- Create netlists for simulation, NDL and LVS from one schematic
- Silvaco's strong encryption is available to protect valuable customer and third party intellectual property

Full Functionality

- Easy to create symbols, sub circuits, sub schematics, and Verilog models.
- Comprehensive symbol creation and editing features for simulation, schematic-driven-layout, and LVS compatibility
- User-configurable keys for repetitive tasks and to emulate legacy capture tool
 - Comprehensive search and replace to process porting, IP reuse, and interactive design
 - Hierarchical capture for modular, reusable designs, libraries, and working with legacy circuits
 - Powerful edit-in place functions with wires, busses, bus ripping, and bus merging
 - Designer configurable rule checks show electrical drawing rule

violations and illegal names

- Parameterized cells (PCells) source design entry data for auto generation of design-rule-connect layout components

Ease of Use and Adoption

- Easy to use for both new and experienced designers with intuitive left-to-right design approach, tool tips, and batch simulation control
- Easy to set up multi-user environment with libraries and import legacy data using EDIF
- Help functions and tool tips for new users
- Batch mode simulation options directly accessible from schematic
- Parameter minimum/maximum checking eliminates entry errors
- Supports wire to wire, wire to pin, wire by name, and implicit/global connections

Integrated Custom IC Design Platform

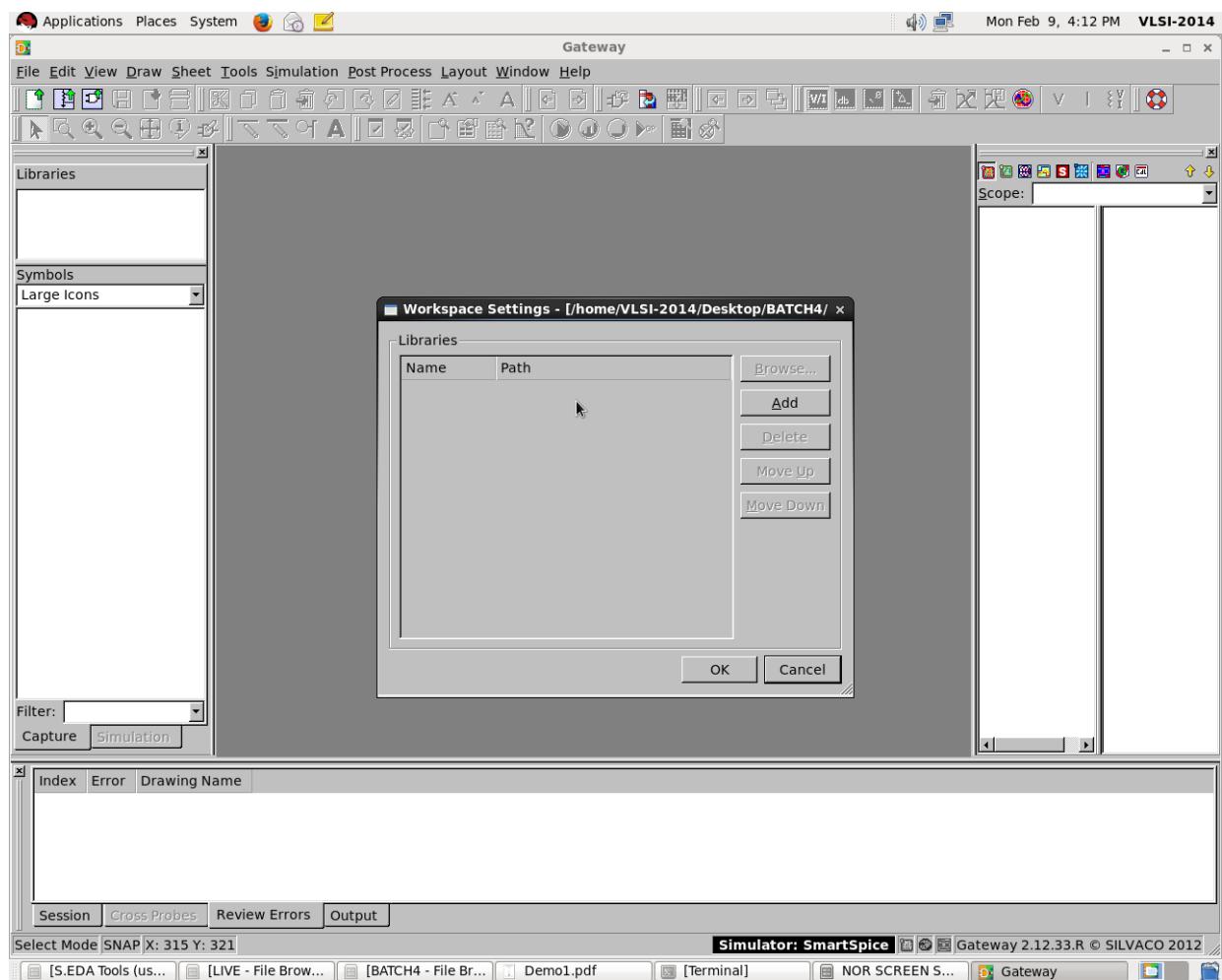
- Front-to-back design automation solution for custom analog circuits
- Connects Silvaco behavioral modeling, schematic, circuit simulation layout, DRC, LVS, and parasitic extraction with proven feedback flows
- Integrated with SmartView Graphical Waveform Postprocessor for overlayed measurements of delays, slopes, overshoots, rise-time, and eye diagrams – complete with vector calculator
- Powerful cross-probing between schematic and post-processing provide real-time design feed back
- Call-backs evaluate expressions in real-time for design rules, tolerances, parametric calculation, and process skews
- DC bias display for currents and voltages throughout hierarchy

Designer Productivity

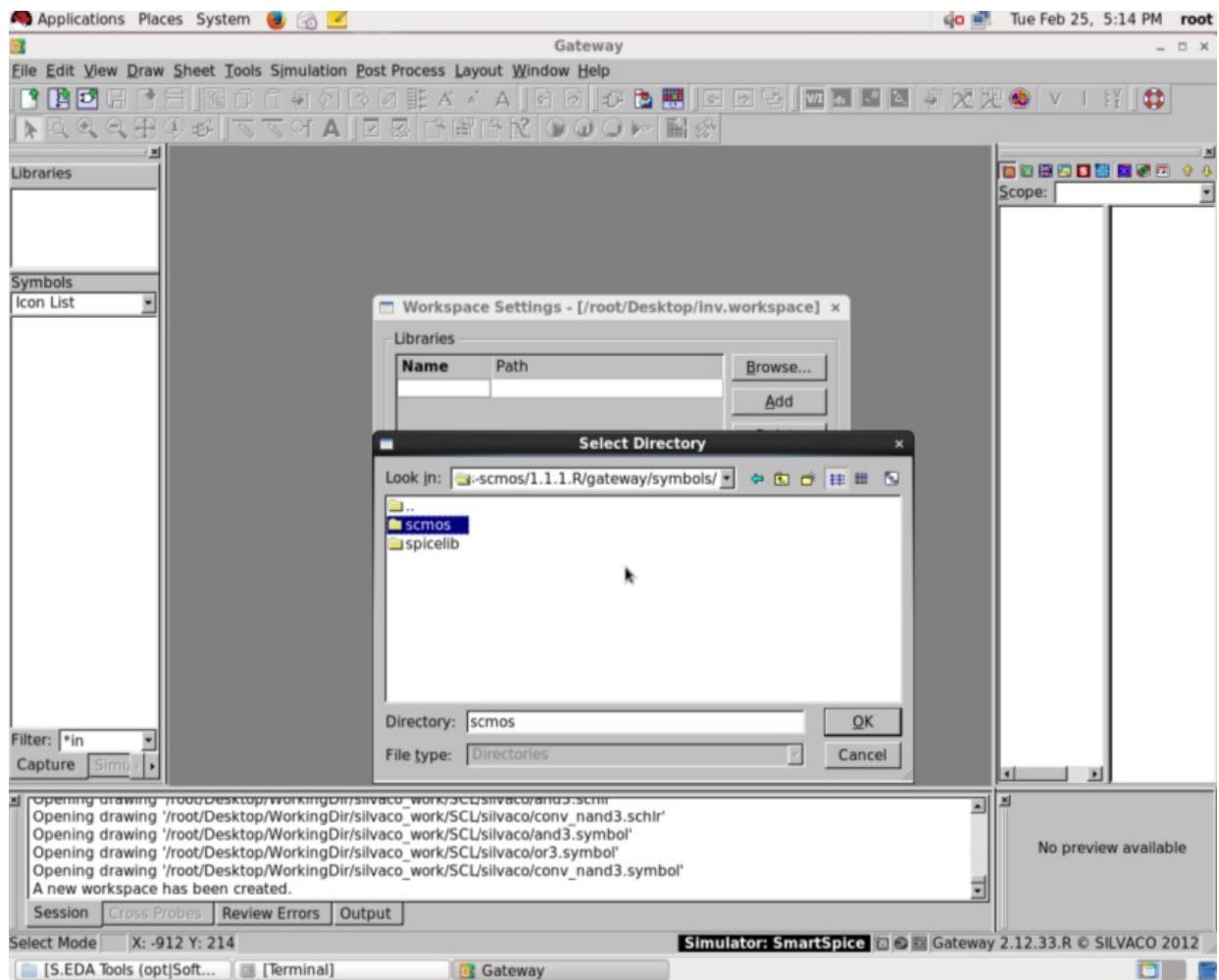
- Creates multiple views for layout, simulation, and LVS for design integrity and smooth tapeouts
- Spreadsheet data entry, netlist import, EDIF reader, and automatic symbol generation for easy re-use of legacy circuits
- Supports encrypted netlists behind symbols in design kits for IP distribution
- Marching waveforms allow real-time viewing of simulation results to check on long simulations
- Efficient control of the design flow between schematic, simulation, and analysis
- Highlights errors and zooms to schematic location/level for correction
- DC bias for currents and voltage for hierarchical and flat drawings

Schematic design of CMOS NOR2

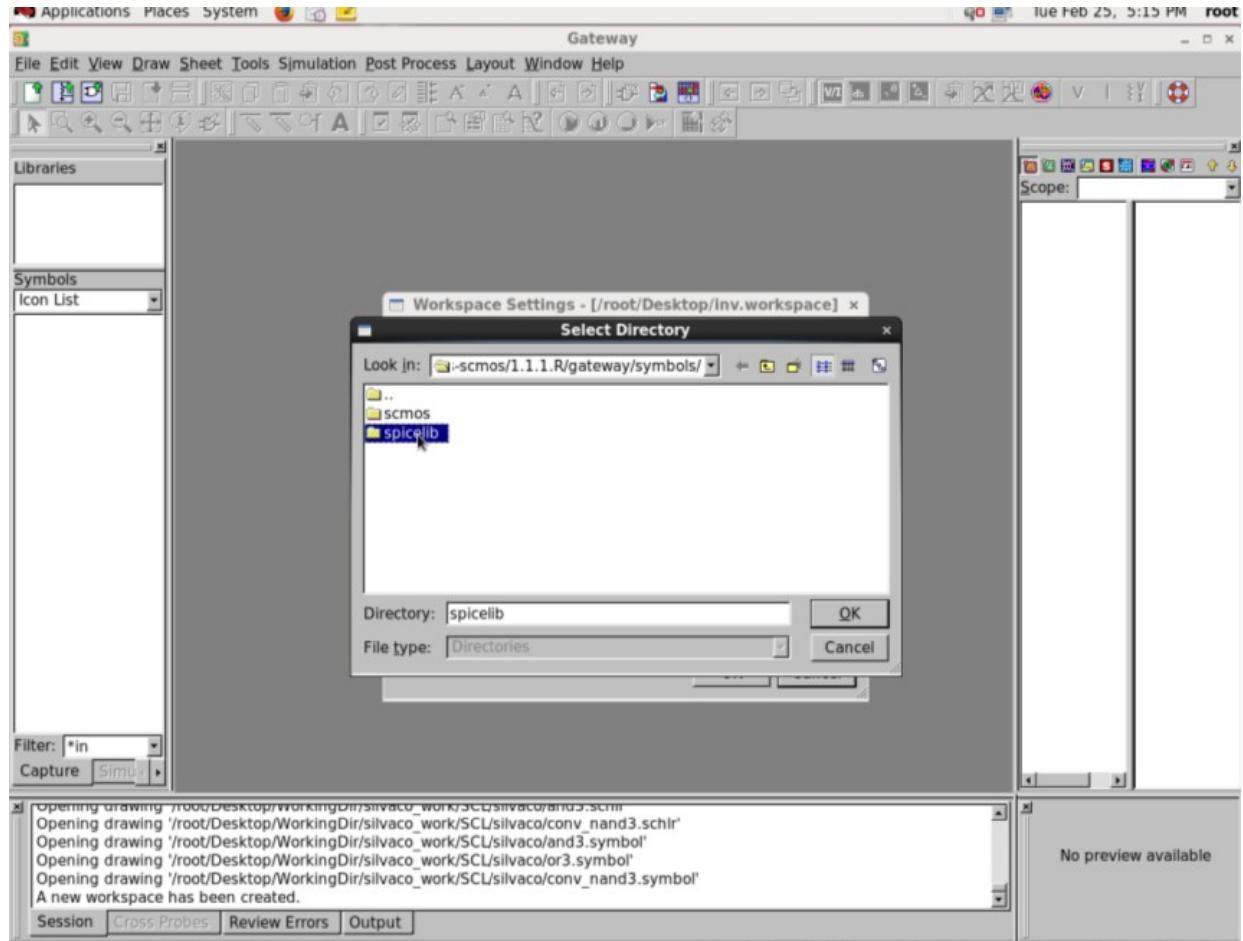
- Open Gateway by double click on Gateway icon which is in S. EDA shortcuts folder.
- A Gateway window will be open.
- Open new workspace, File-New-Workspace.



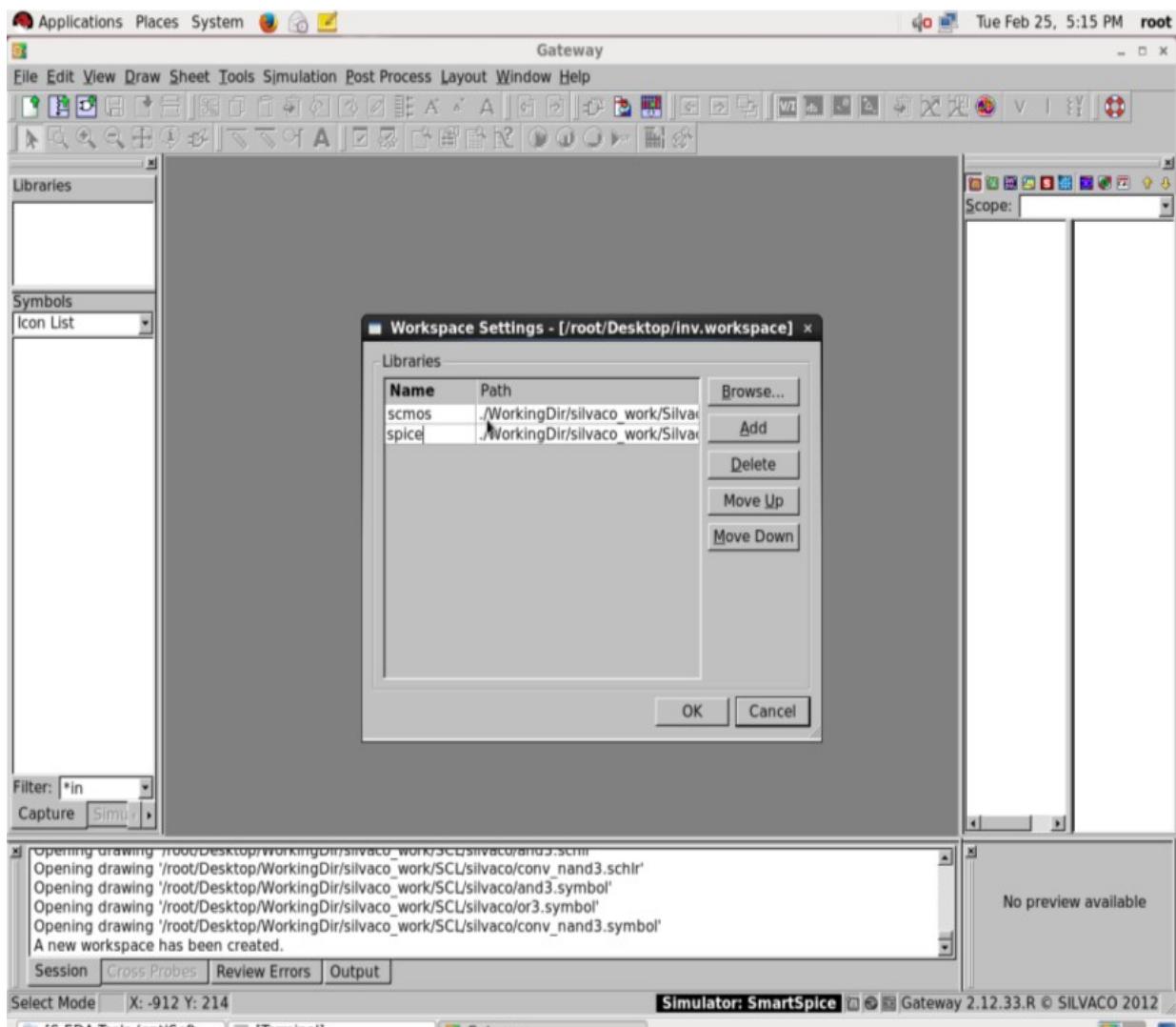
- Add library symbols by selecting the proper directory.



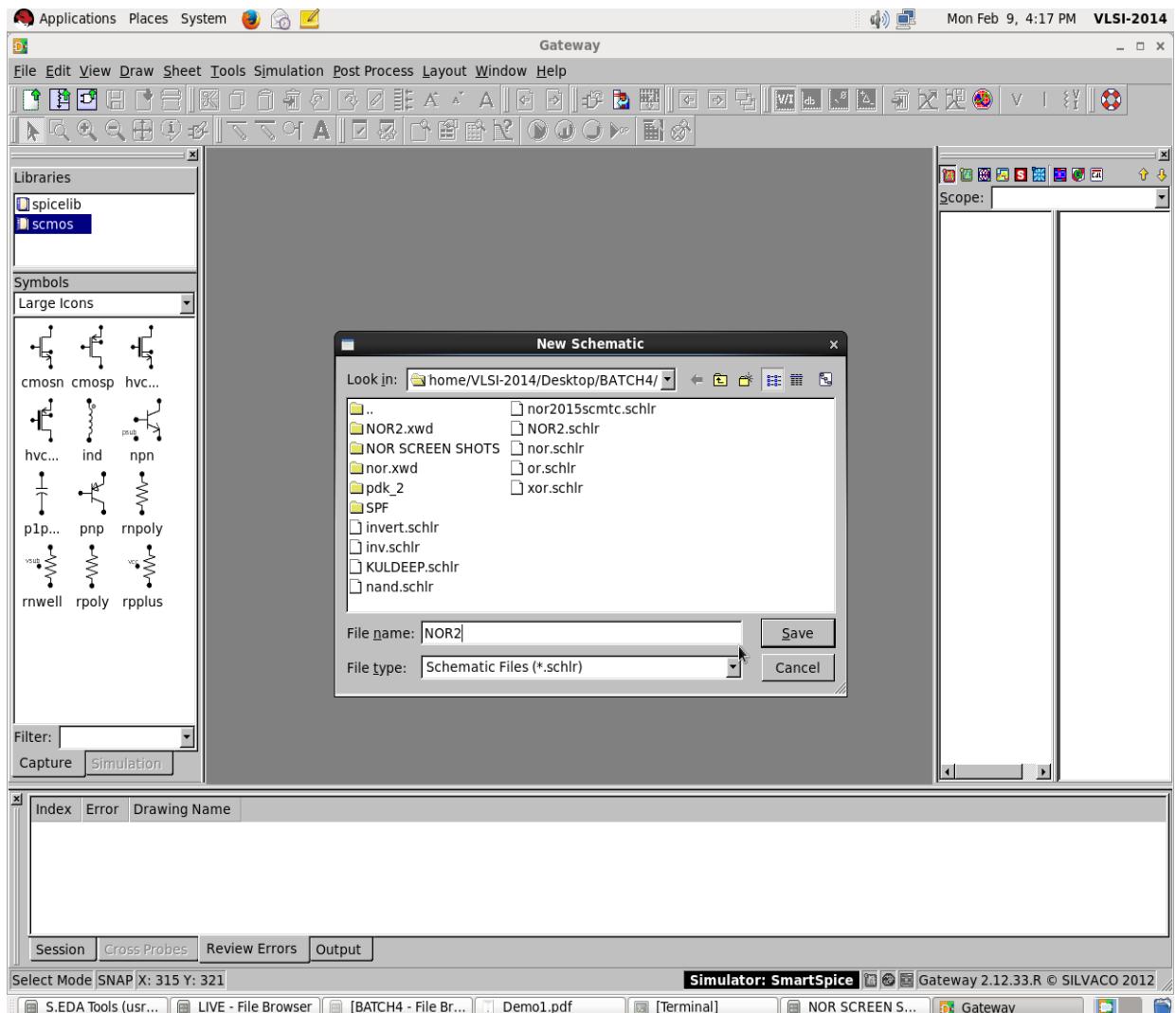
- Add another library symbols for various input output functions.



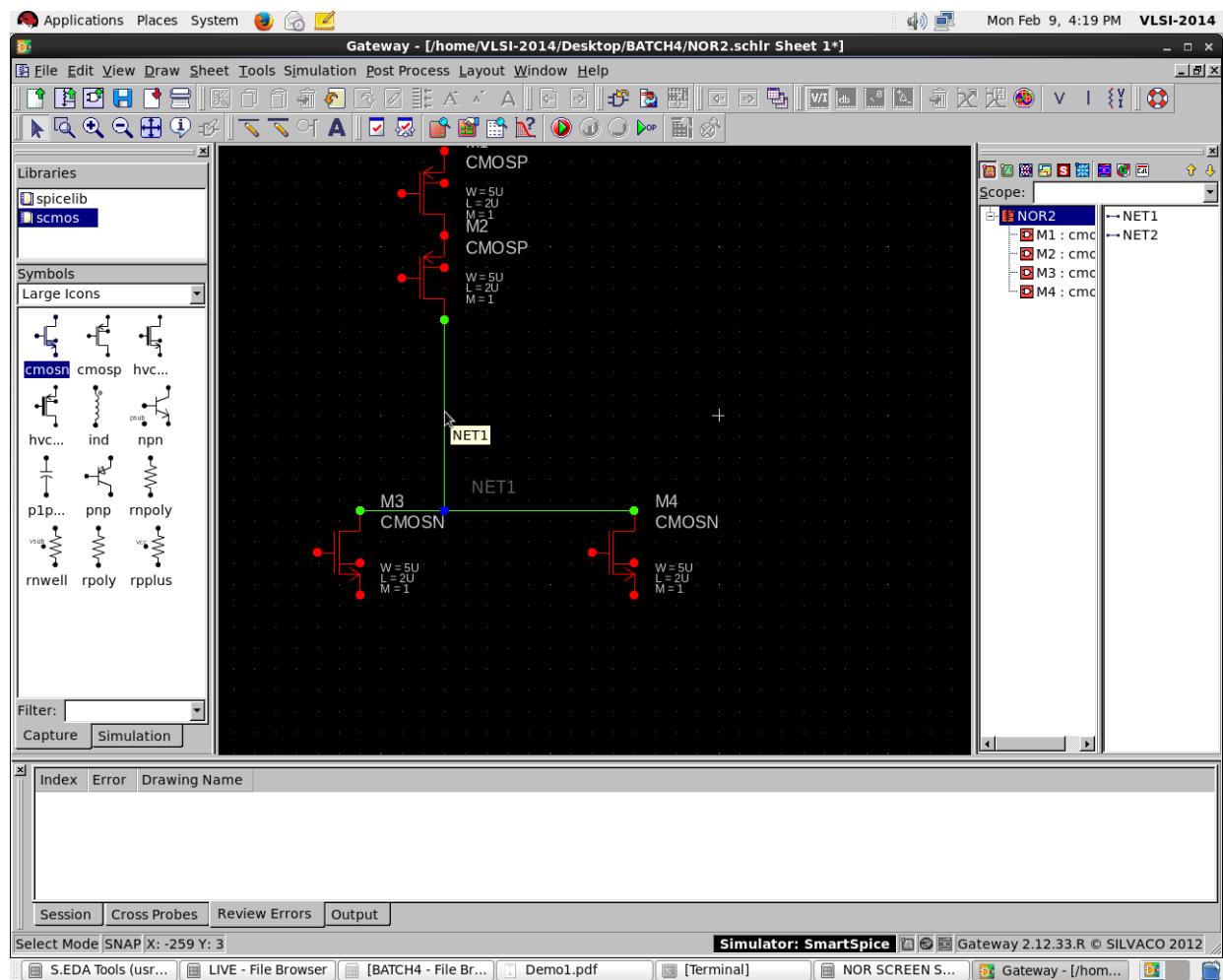
- Edit the library names as per whenever needed.



- Open new schematic, File-New-Schematic.
- Give the name of your design.

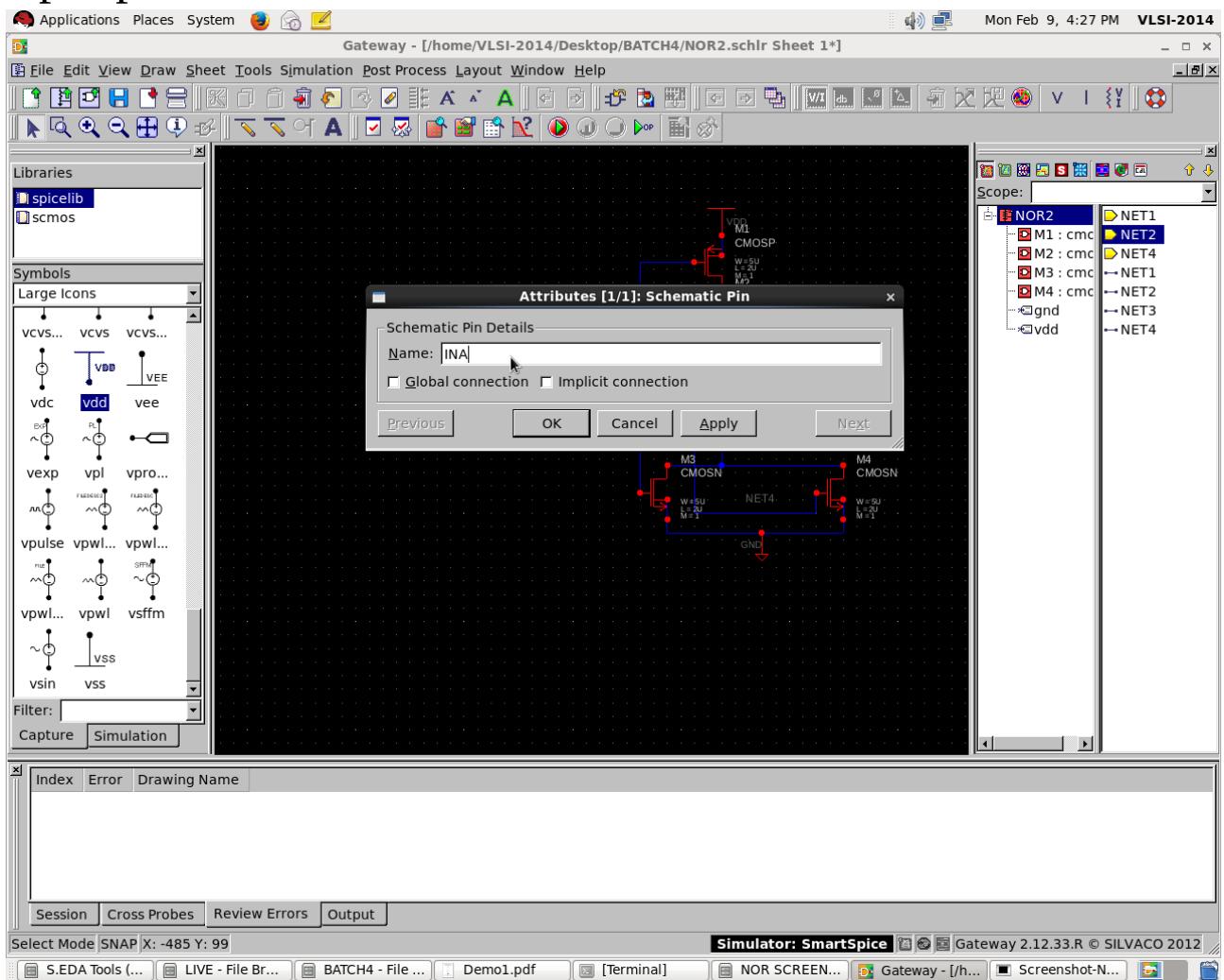


- A new schematic window will open.
- Select any library and put the symbols in schematic window.
- Draw CMOSP and CMOSN transistors from the scmos library.

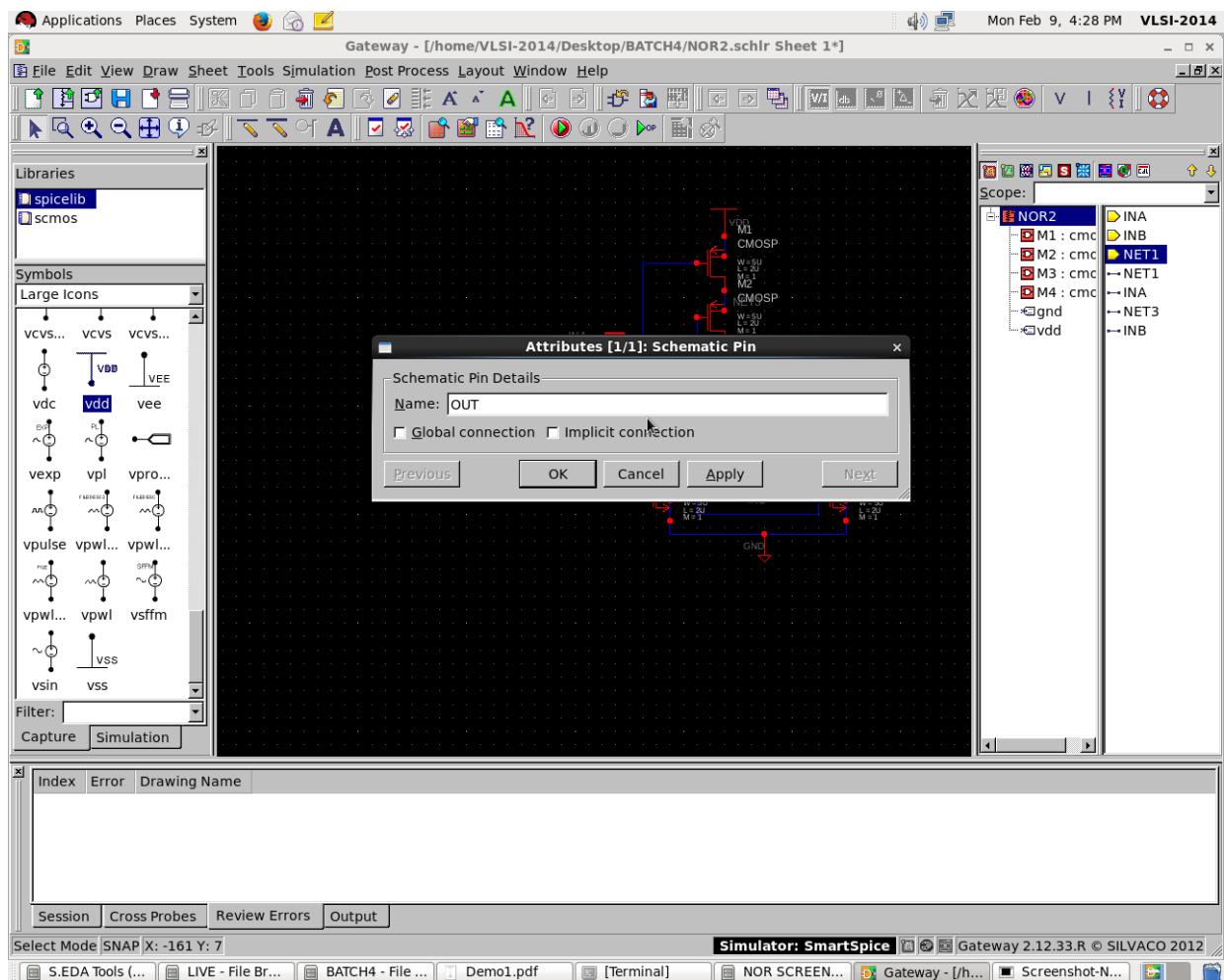


- Add VDD and GND from spice library.
- Edit pin names by double clicking on them.

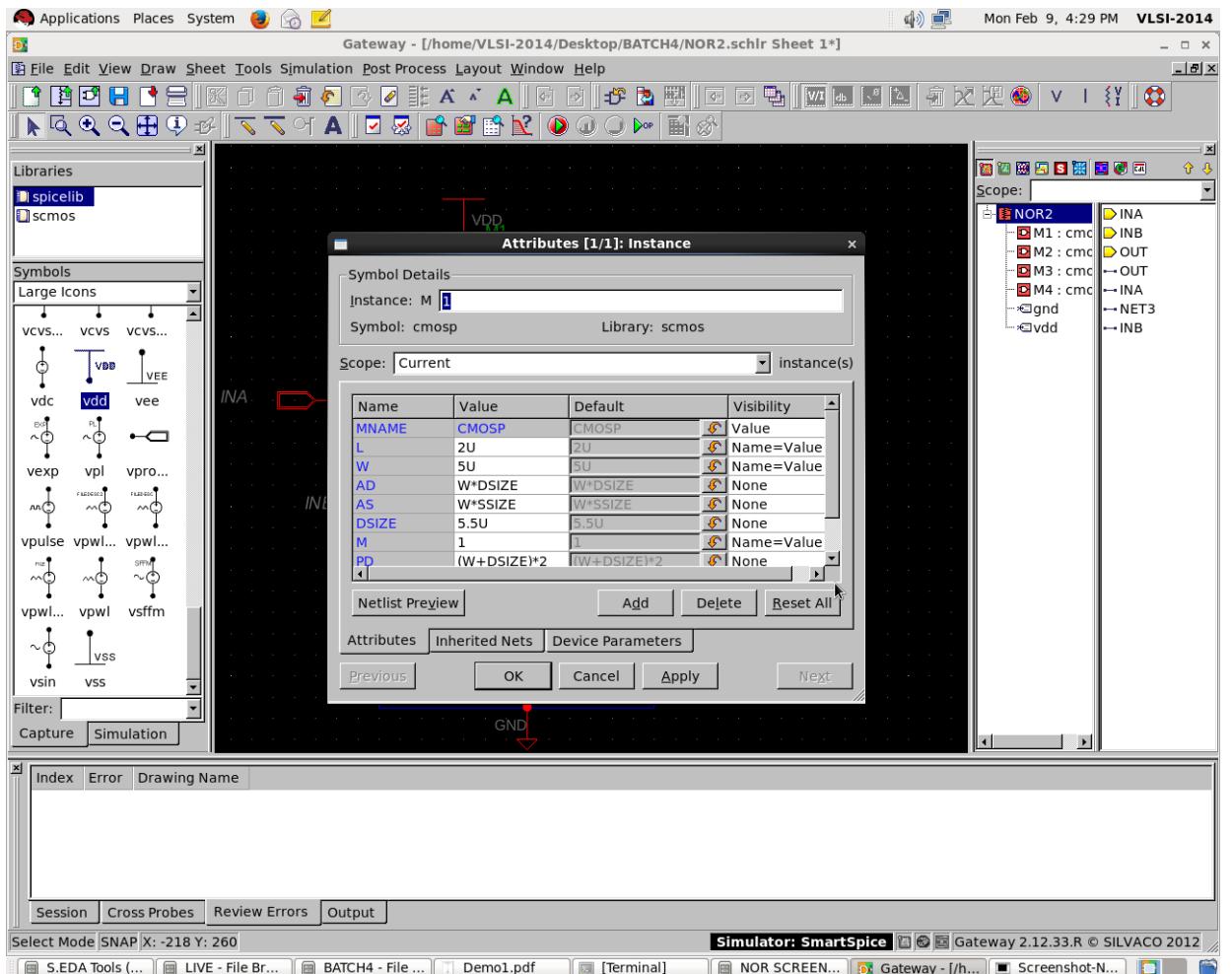
Input pin



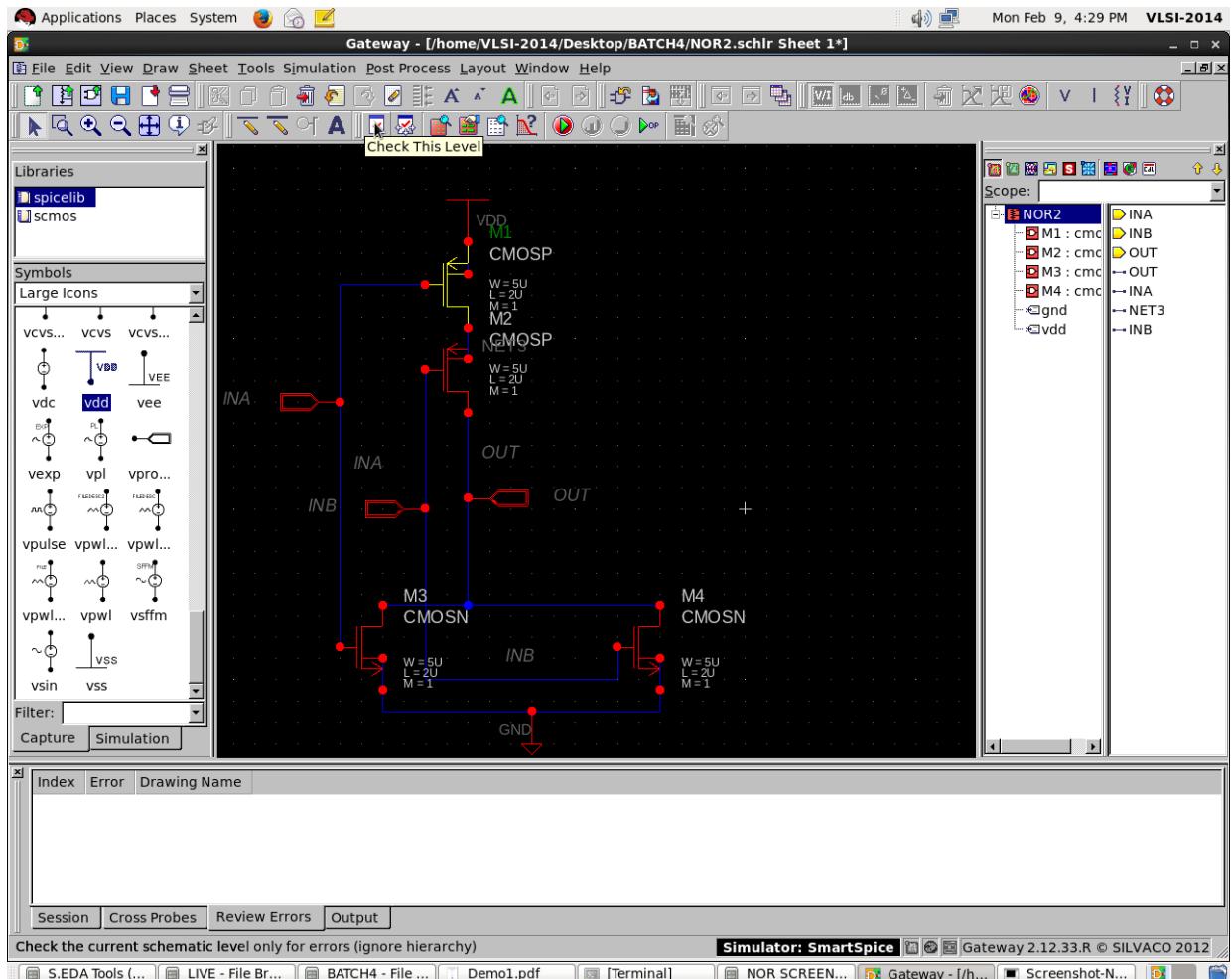
Output pin:



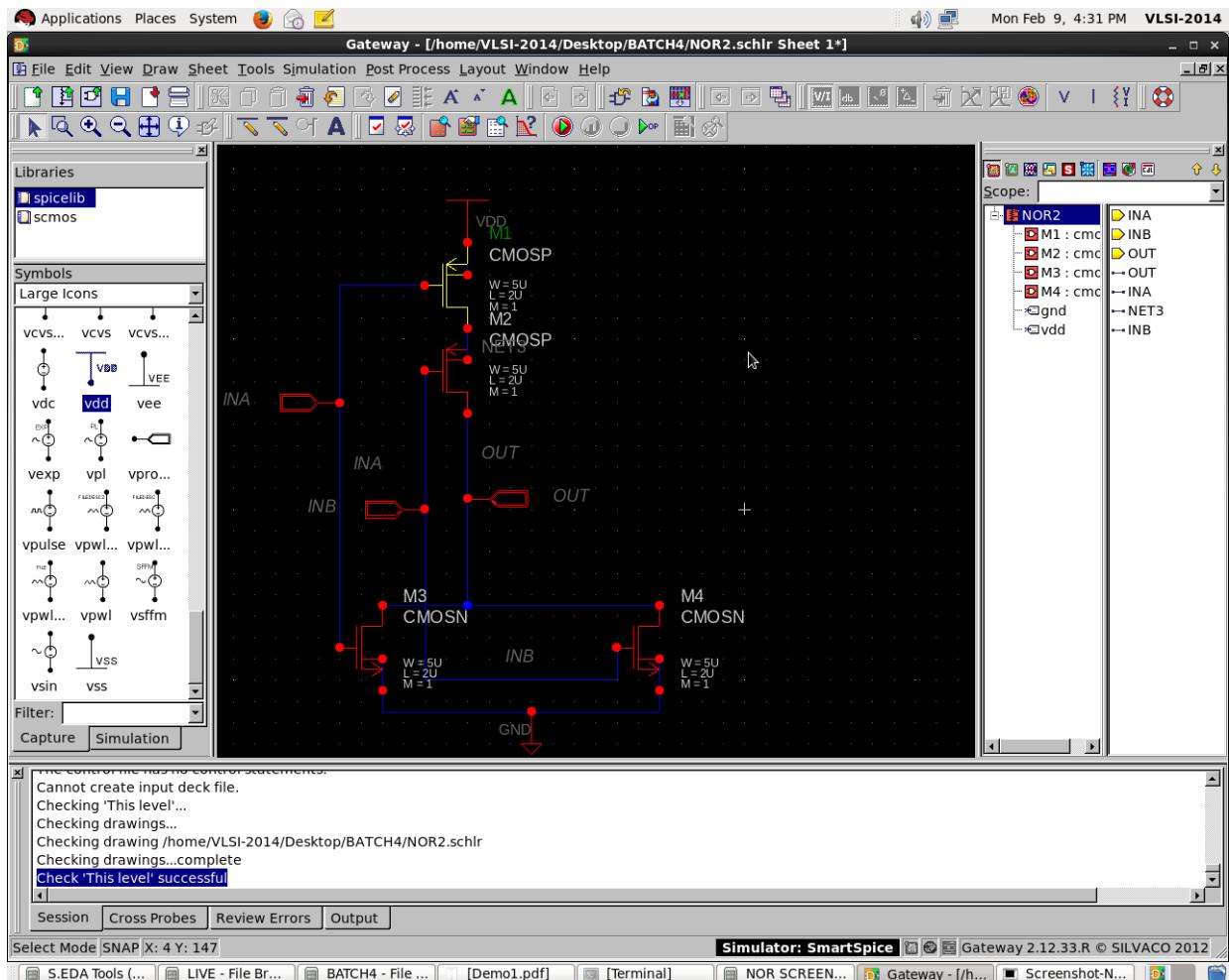
- Property window will be open by double clicking on MOS transistors.



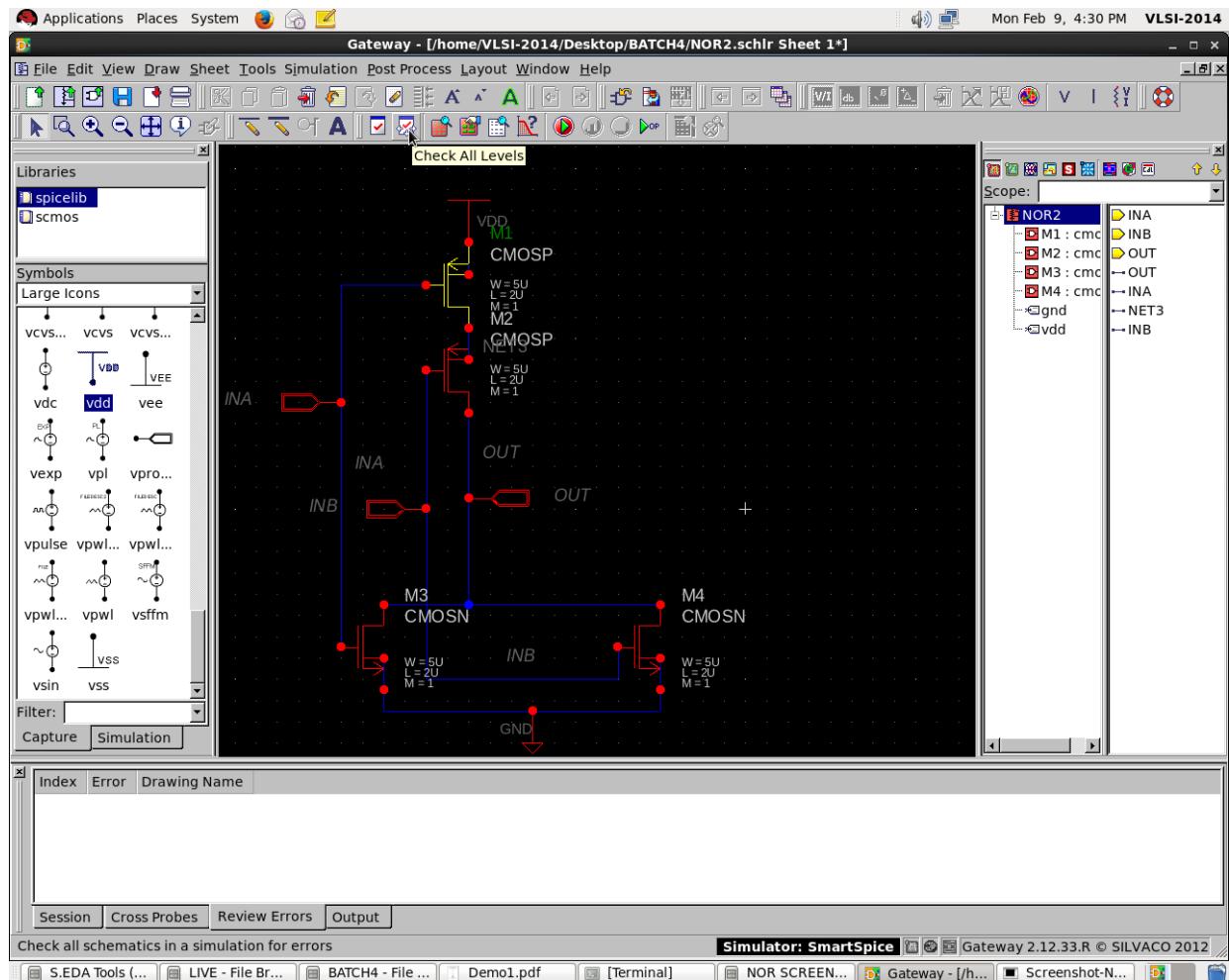
- After drawing the design, check this level.



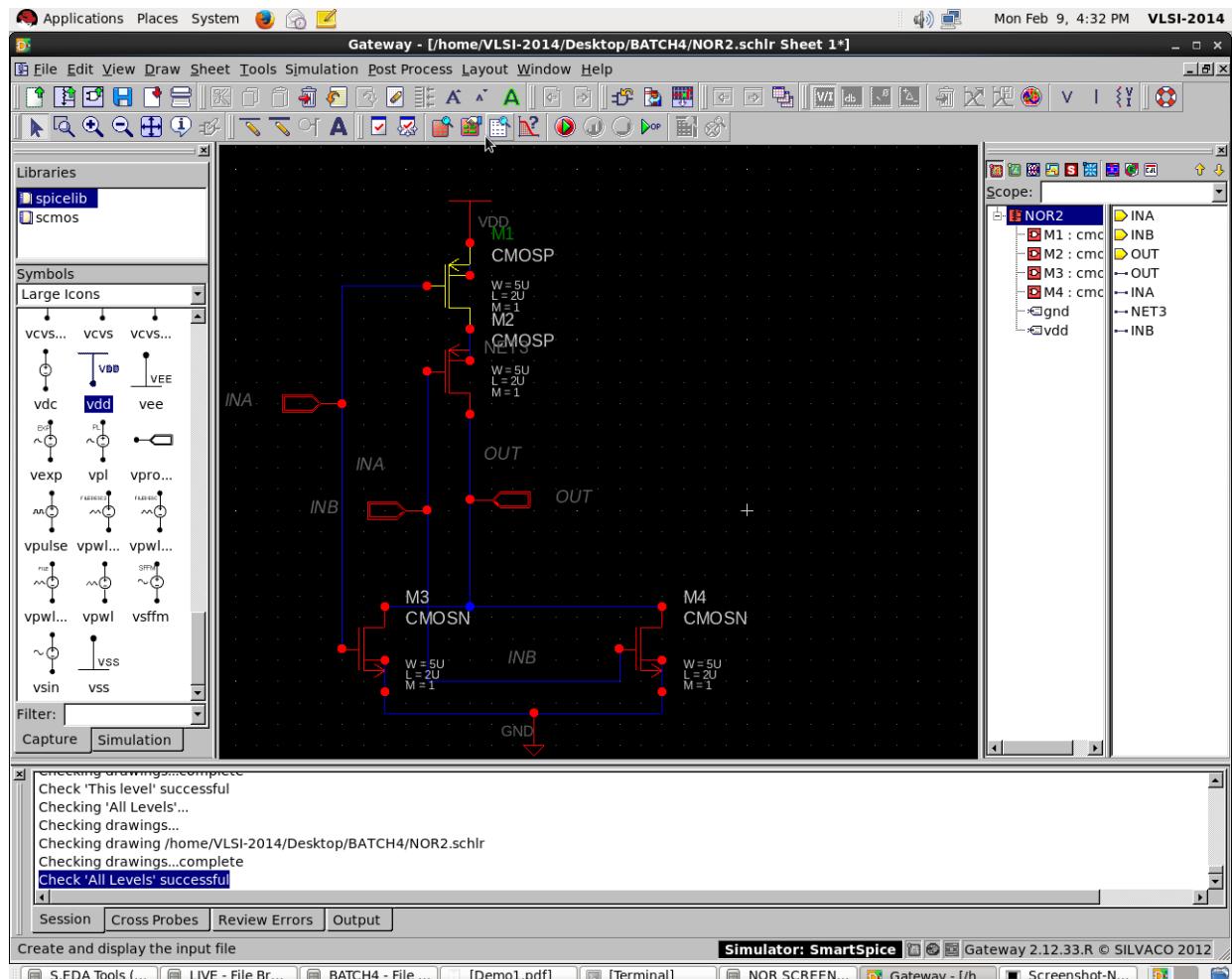
- A notice will appear showing “check this level successful”.
- If it is not ok then check the schematic carefully.



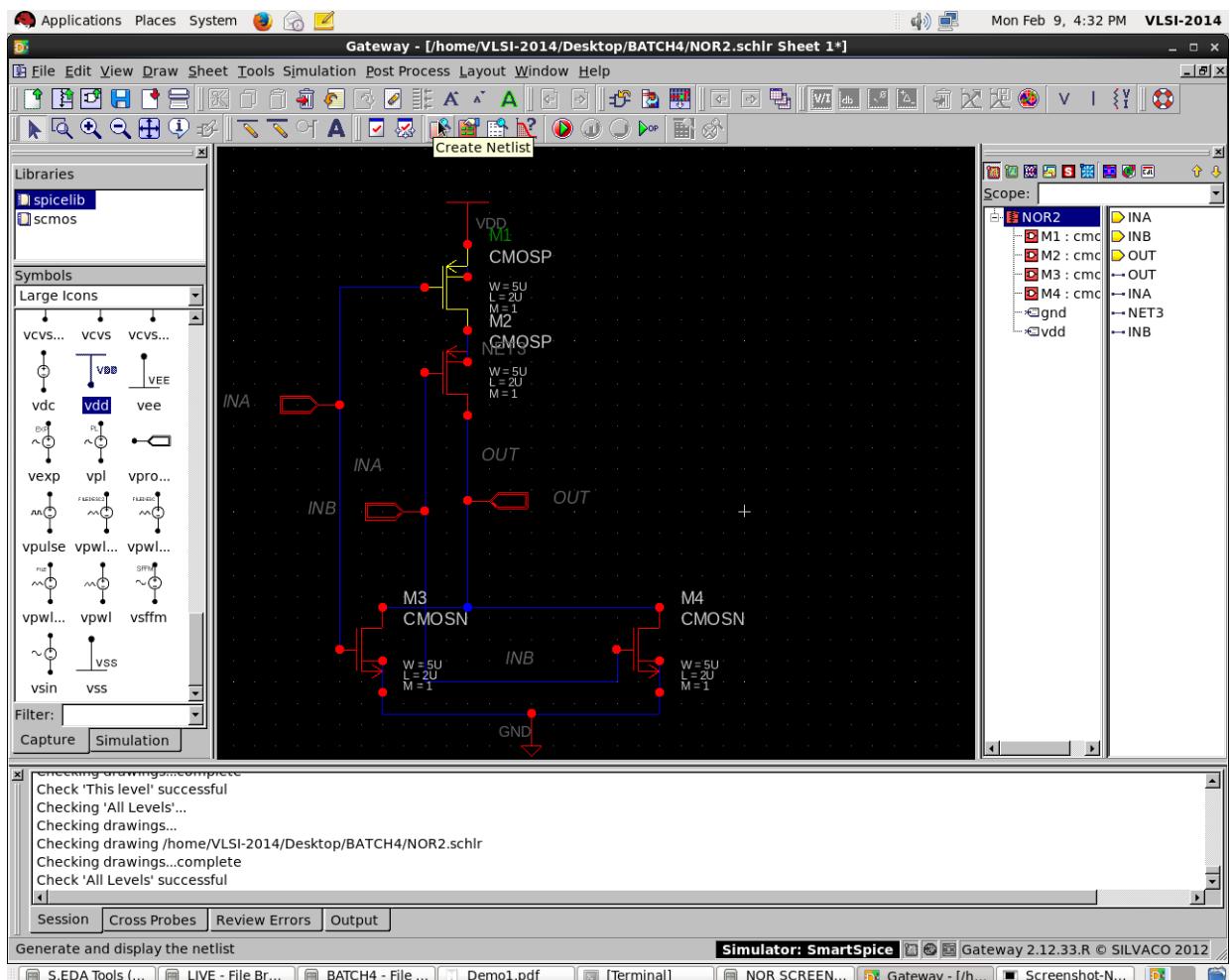
- After checking this level, check all levels.



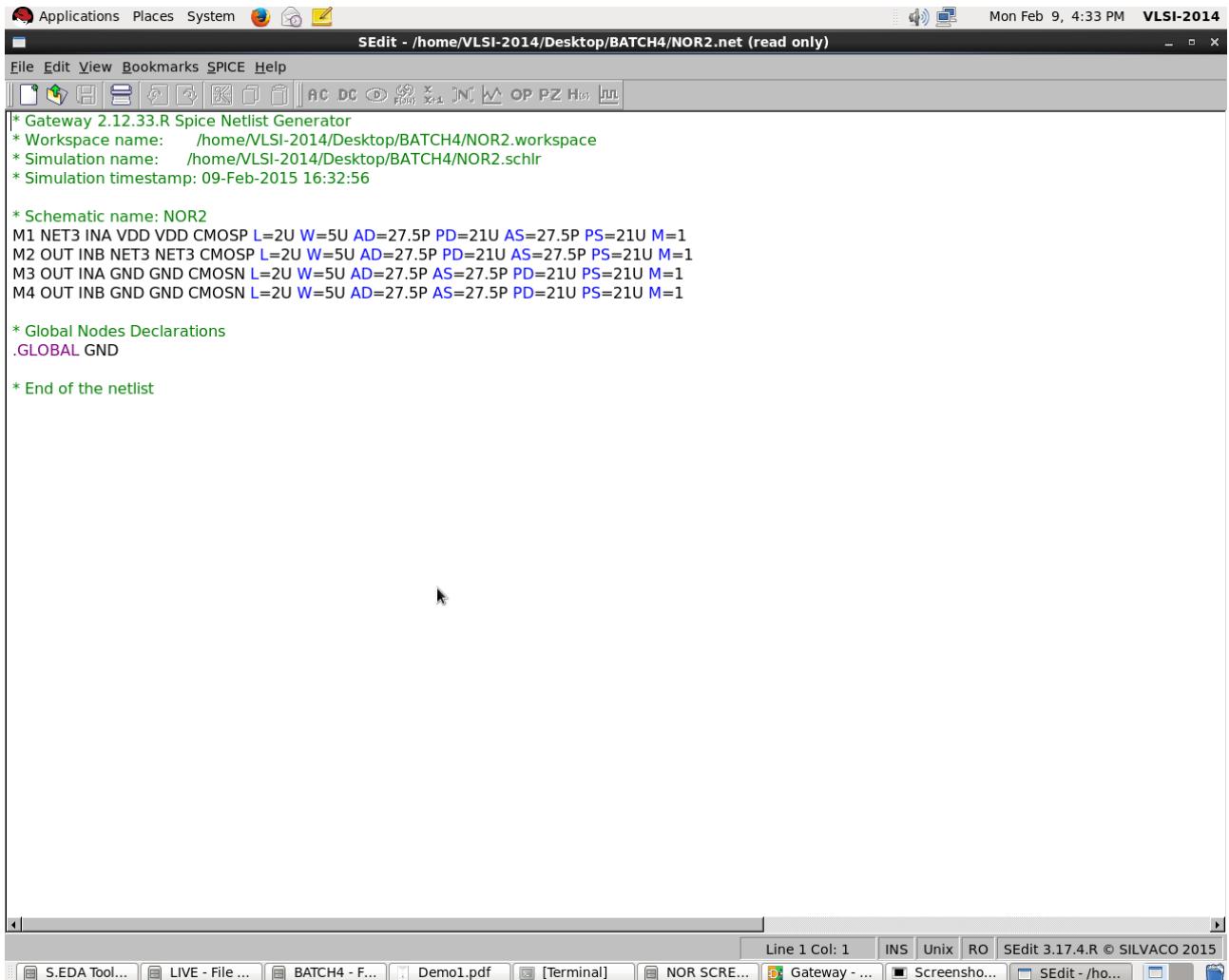
- Message will appear, check all levels successful.



- Create spice netlist by clicking on “Create Netlist” icon.



- A new SEdit window will be open.



The screenshot shows the SEdit 3.17.4.R software interface. The title bar reads "SEdit - /home/VLSI-2014/Desktop/BATCH4/NOR2.net (read only)". The menu bar includes File, Edit, View, Bookmarks, SPICE, Help, and various simulation icons (AC, DC, transient, etc.). The main window displays a SPICE netlist for a NOR2 gate. The netlist content is as follows:

```

* Gateway 2.12.33.R Spice Netlist Generator
* Workspace name: /home/VLSI-2014/Desktop/BATCH4/NOR2.workspace
* Simulation name: /home/VLSI-2014/Desktop/BATCH4/NOR2.schlr
* Simulation timestamp: 09-Feb-2015 16:32:56

* Schematic name: NOR2
M1 NET3 INA VDD VDD CMOSP L=2U W=5U AD=27.5P PD=21U AS=27.5P PS=21U M=1
M2 OUT INB NET3 NET3 CMOSP L=2U W=5U AD=27.5P PD=21U AS=27.5P PS=21U M=1
M3 OUT INA GND GND CMOSN L=2U W=5U AD=27.5P AS=27.5P PD=21U PS=21U M=1
M4 OUT INB GND GND CMOSN L=2U W=5U AD=27.5P AS=27.5P PD=21U PS=21U M=1

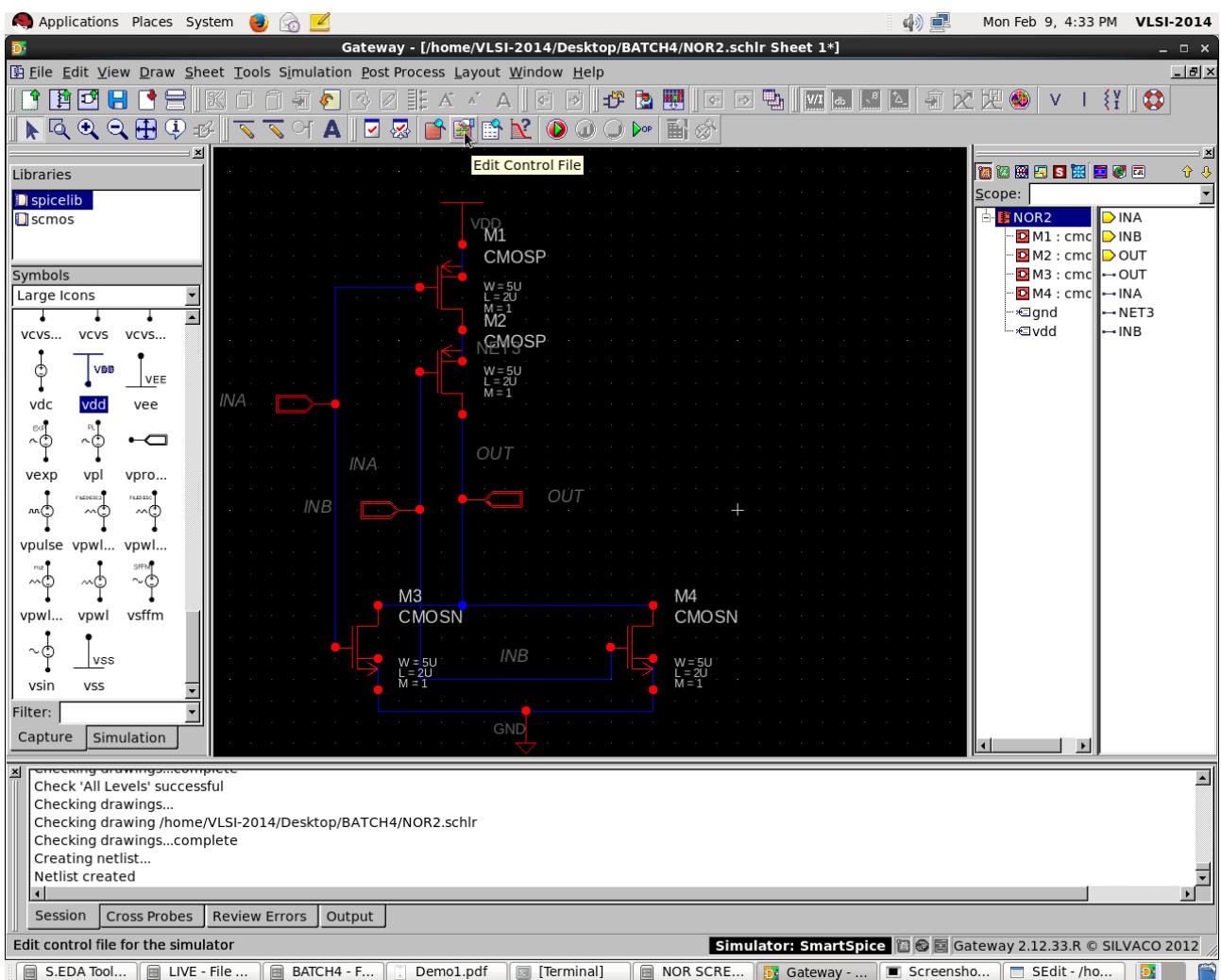
* Global Nodes Declarations
.GLOBAL GND

* End of the netlist

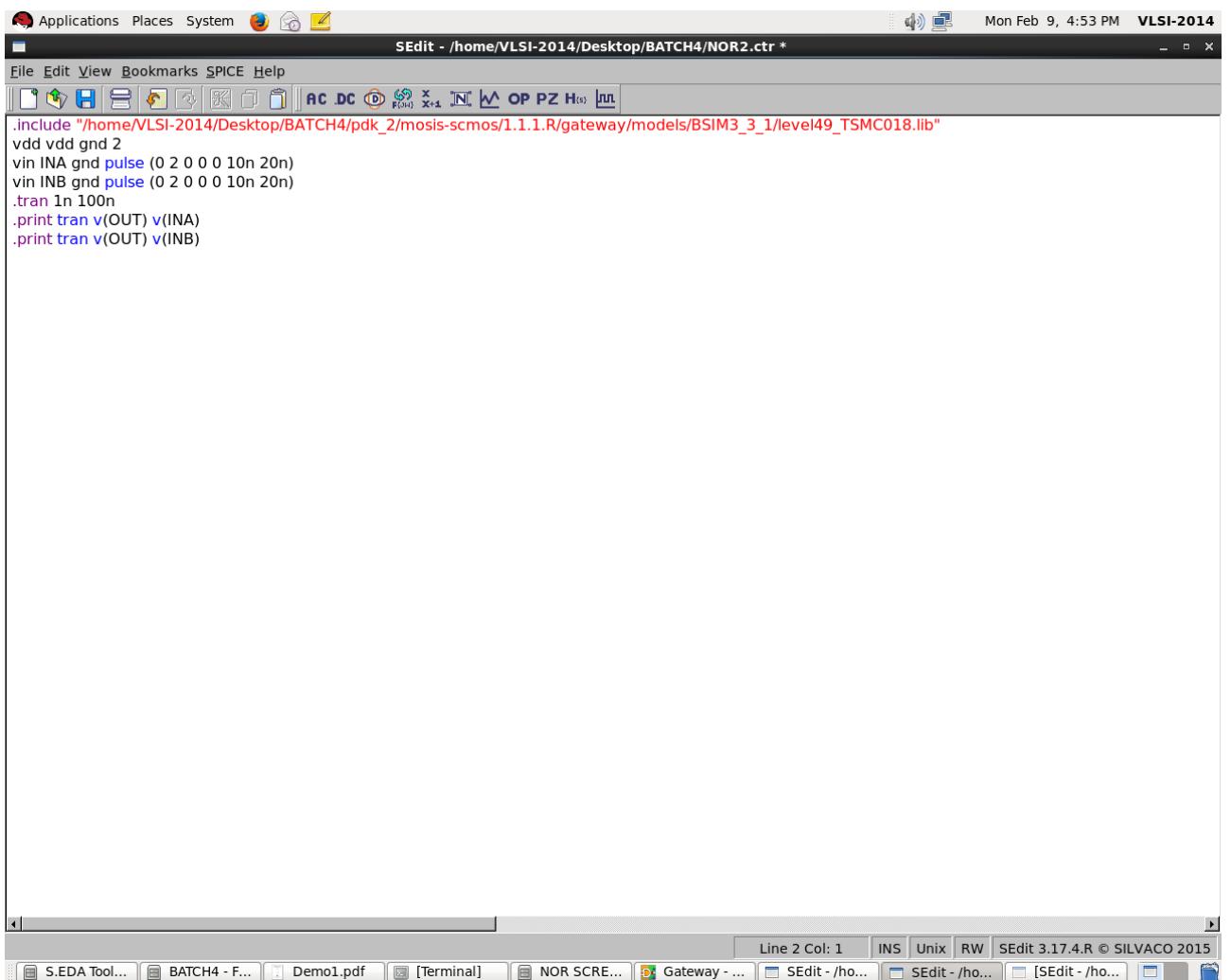
```

The bottom of the window shows a toolbar with various icons and a status bar indicating "Line 1 Col: 1". The taskbar at the bottom of the screen lists several open applications, including S.EDA Tool..., LIVE - File ..., BATCH4 - F..., Demo1.pdf, [Terminal], NOR SCRE..., Gateway - ..., Screensho..., and SEdit - /ho...".

- Edit the spice netlist by clicking on “Edit Control File”.



- A new SEdit window will be open.
- Provide the model file definition and analysis type here.
- Edit in the SEdit window whatever you want.



The screenshot shows a Linux desktop environment with a terminal window titled "SEdit - /home/VLSI-2014/Desktop/BATCH4/NOR2.ctr *". The terminal window contains the following SPICE script:

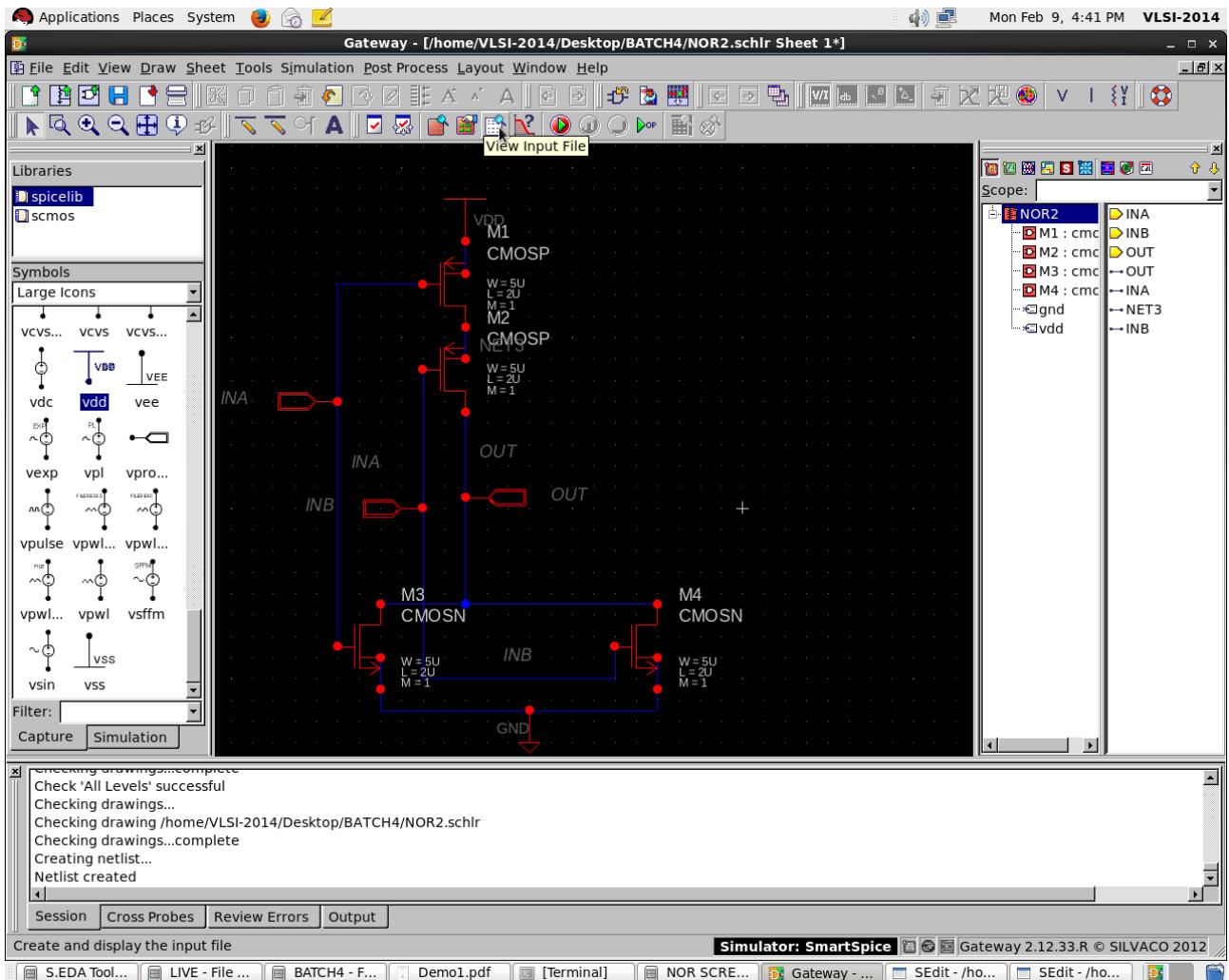
```

.include "/home/VLSI-2014/Desktop/BATCH4/pdk_2/mosis-scmos/1.1.1.R/gateway/models/BSIM3_3_1/level49_TSMC018.lib"
vdd vdd gnd 2
vin INA gnd pulse (0 2 0 0 0 10n 20n)
vin INB gnd pulse (0 2 0 0 0 10n 20n)
.tran 1n 100n
.print tran v(OUT) v(INA)
.print tran v(OUT) v(INB)

```

The terminal window also displays the system menu bar at the top and a taskbar at the bottom with various application icons and windows.

- View complete spice file by clicking on “View Input File”.



- A complete spice file will be open in new window.

Applications Places System

SEdit - /home/VLSI-2014/Desktop/BATCH4/NOR2.in (read only) Mon Feb 9, 4:54 PM VLSI-2014

File Edit View Bookmarks SPICE Help

AC DC IN OUT OP PZ H_o

```

* /home/VLSI-2014/Desktop/BATCH4/NOR2
* Gateway 2.12.33.R Spice Netlist Generator
* Workspace name: /home/VLSI-2014/Desktop/BATCH4/NOR2.workspace
* Simulation name: /home/VLSI-2014/Desktop/BATCH4/NOR2.schrl
* Simulation timestamp: 09-Feb-2015 16:54:50

* Schematic name: NOR2
M1 NET3 INA VDD CMOSP L=2U W=5U AD=27.5P PD=21U AS=27.5P PS=21U M=1
M2 OUT INB NET3 NET3 CMOSP L=2U W=5U AD=27.5P PD=21U AS=27.5P PS=21U M=1
M3 OUT INA GND GND CMOSN L=2U W=5U AD=27.5P AS=27.5P PD=21U PS=21U M=1
M4 OUT INB GND GND CMOSN L=2U W=5U AD=27.5P AS=27.5P PD=21U PS=21U M=1

* Global Nodes Declarations
.GLOBAL GND

* End of the netlist
* Schematic Netlist rebuilt at runtime

.include "/home/VLSI-2014/Desktop/BATCH4/pdk_2/mosis-scmos/1.1.1.R/gateway/models/BSIM3_3_1/level49_TSMC018.lib"
vdd vdd gnd 2
vin INA gnd pulse (0 2 0 0 0 10n 20n)
vin INB gnd pulse (0 2 0 0 0 10n 20n)
.tran 1n 100n
.print tran v(OUT) v(INA)
.print tran v(OUT) v(INB)

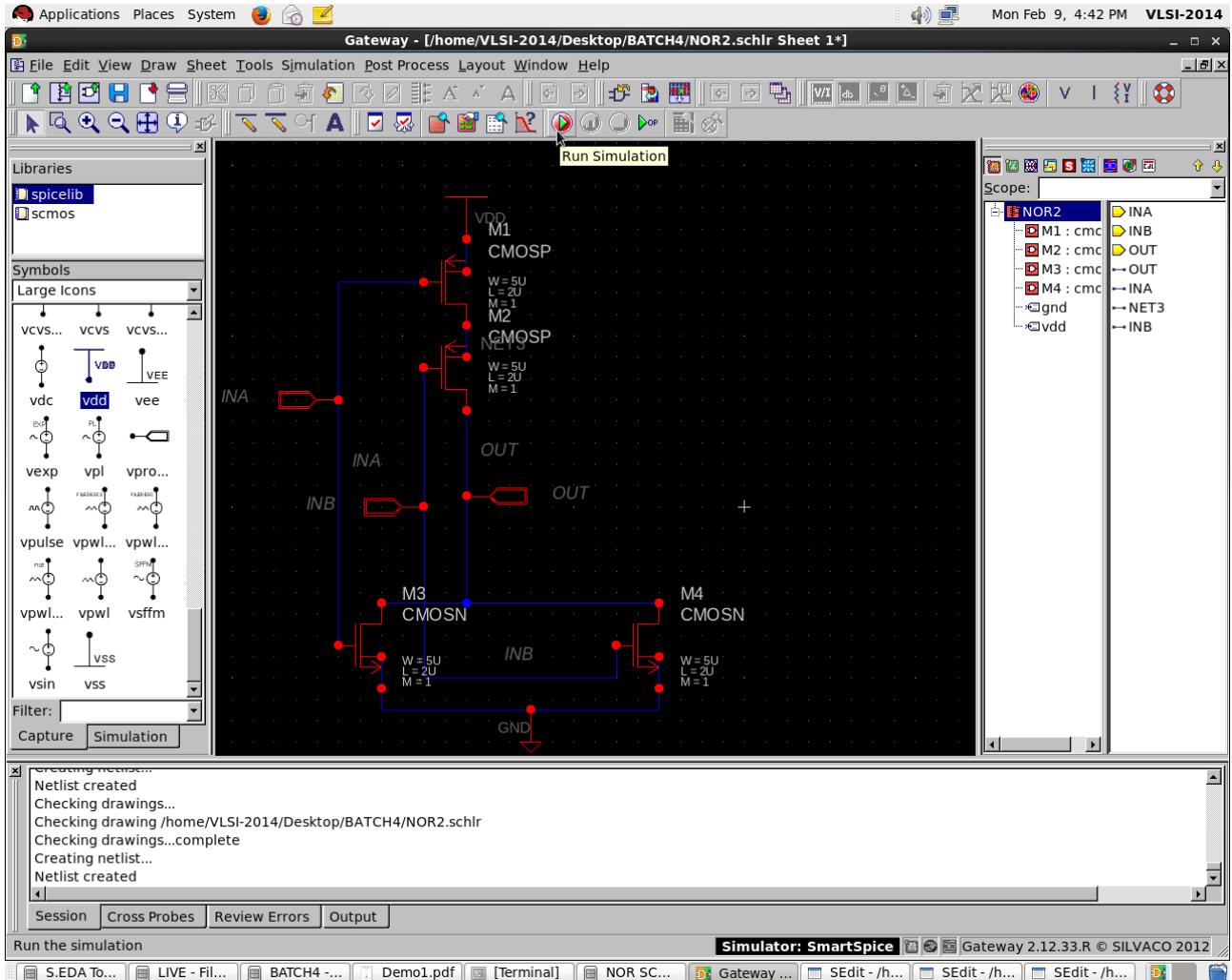
.END

```

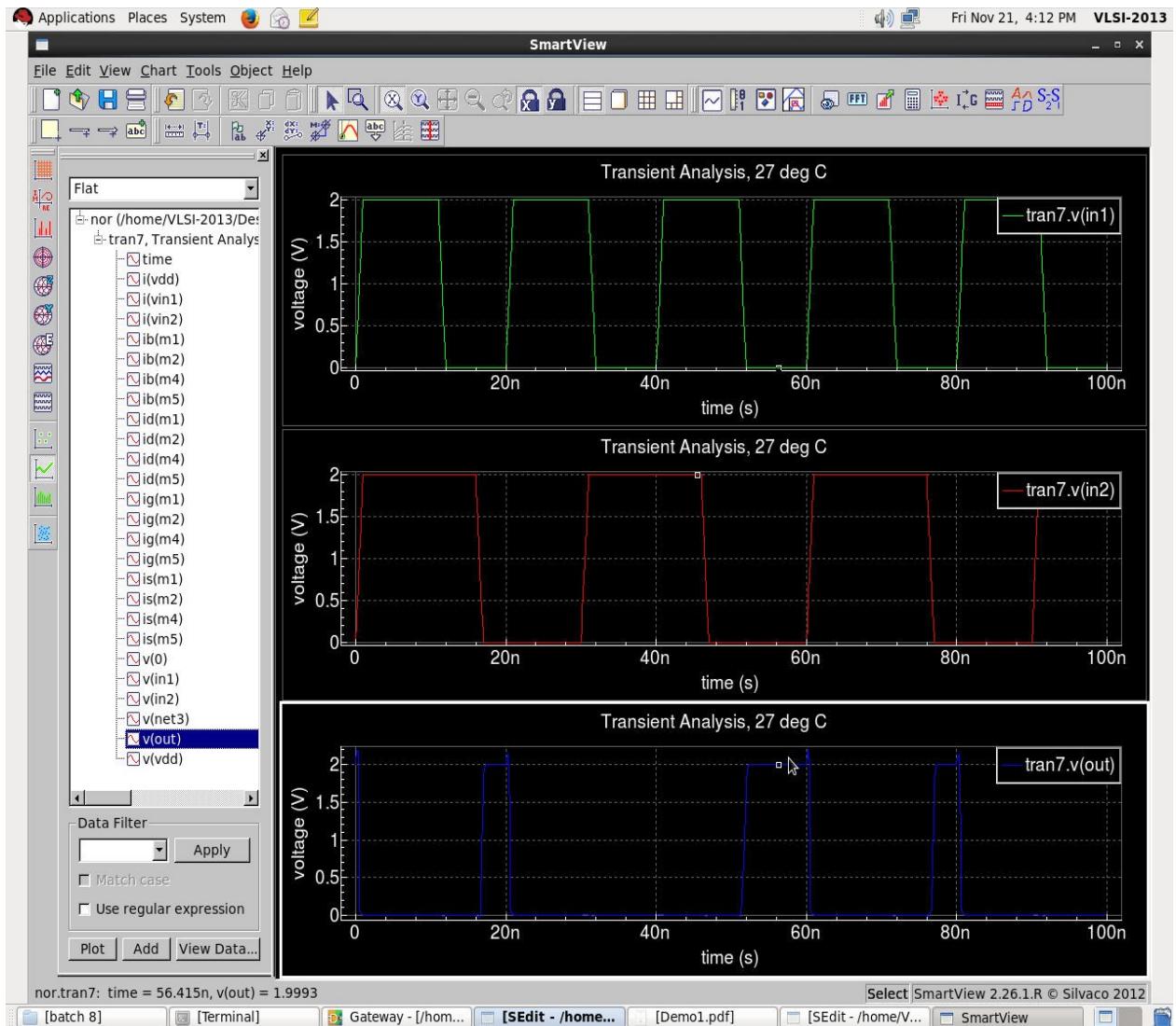
Line 1 Col: 1 INS Unix RO SEdit 3.17.4.R © SILVACO 2015

S.EDA Tool... BATCH4 - F... Demo1.pdf [Terminal] NOR SCRE... Gateway - ... SEdit - /ho... SEdit - /ho... SEdit - /ho...

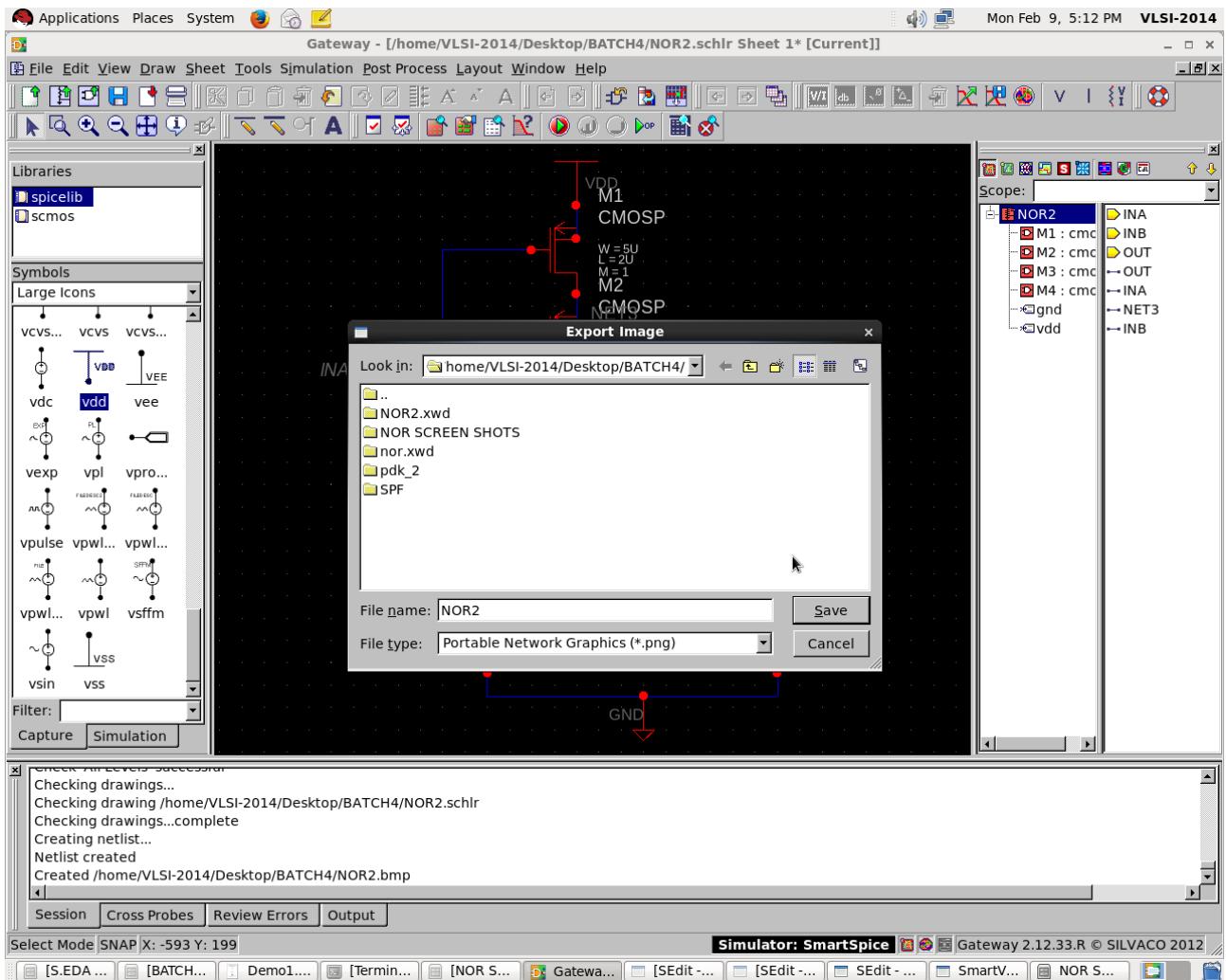
- After checking complete spice file, run the schematic for the simulation by clicking on “Run Simulation”.
- The default simulator is set as SmartSpice.



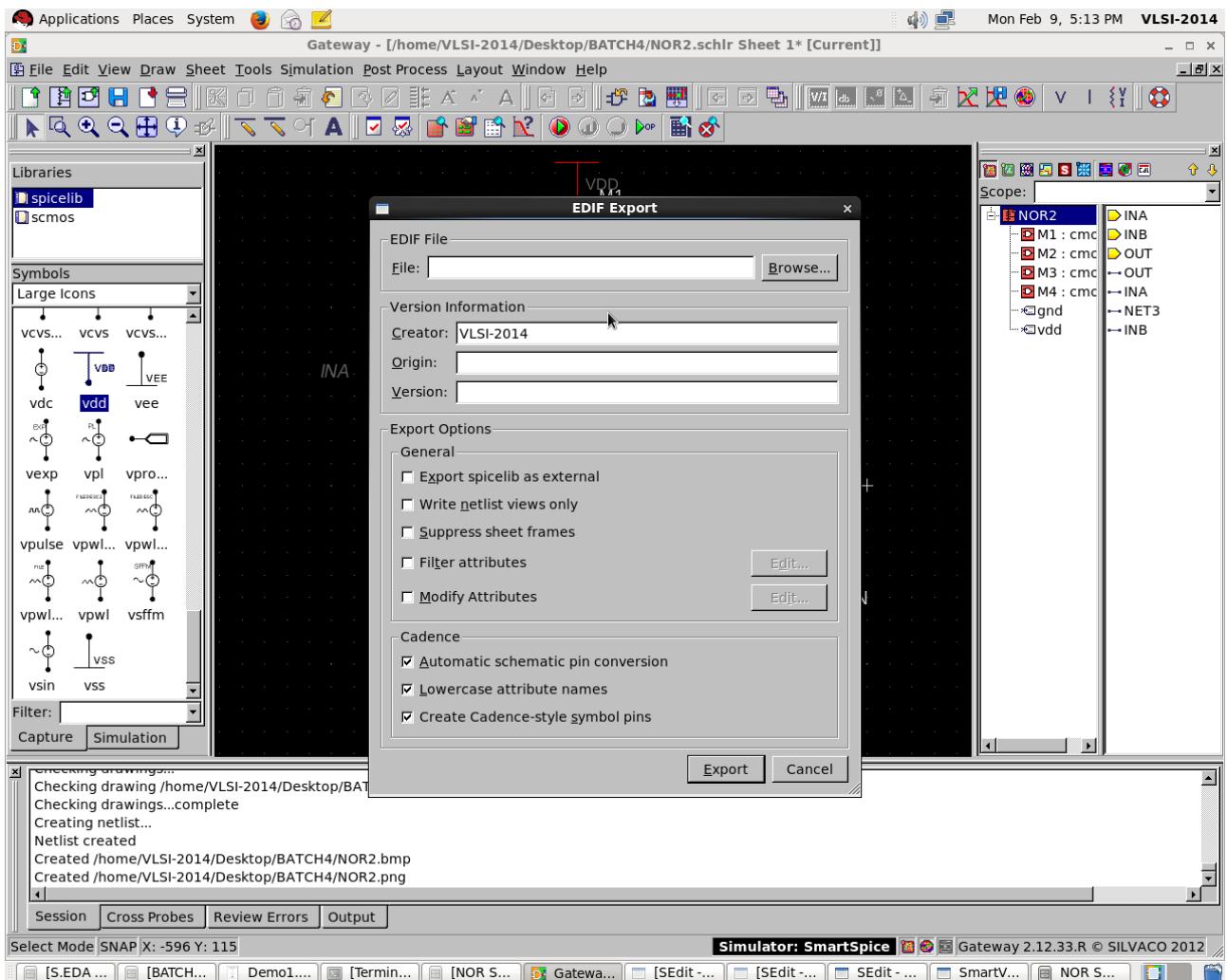
- A new window of SmartView will be open.
- SmartView is the wave viewer of Silvaco's EDA tools.
- A desired waveform can be plotted by selecting them in data browser window.



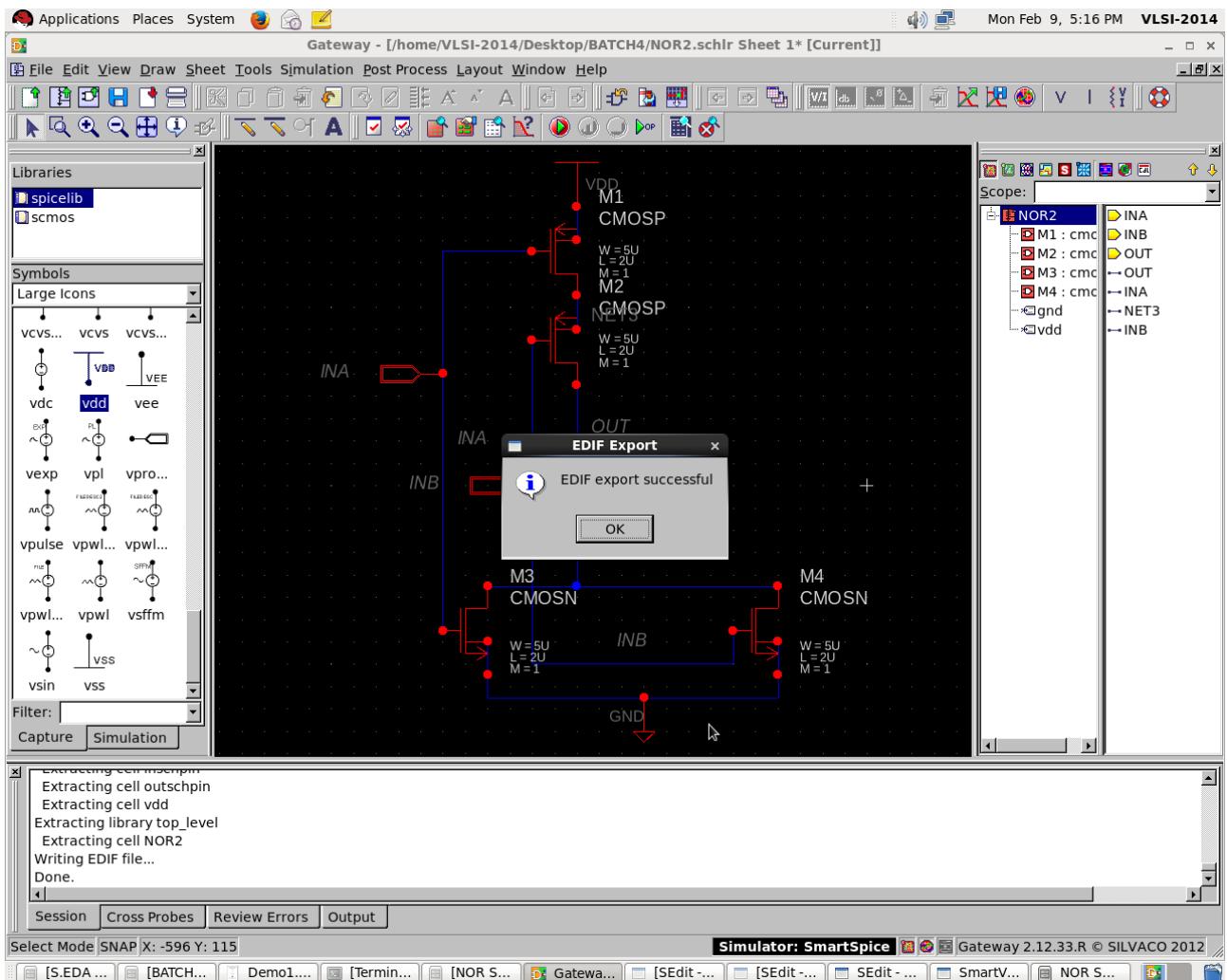
- A message will be displayed in Gateway tool as “simulations has finished”.
- Schematic cell view will be exported through, File-Export-Image.



- EDIF format will be exported through, File-Export-EDIF.
- Select the directory for EDIF view export.



- A message will be displayed as “EDIF export successful”.

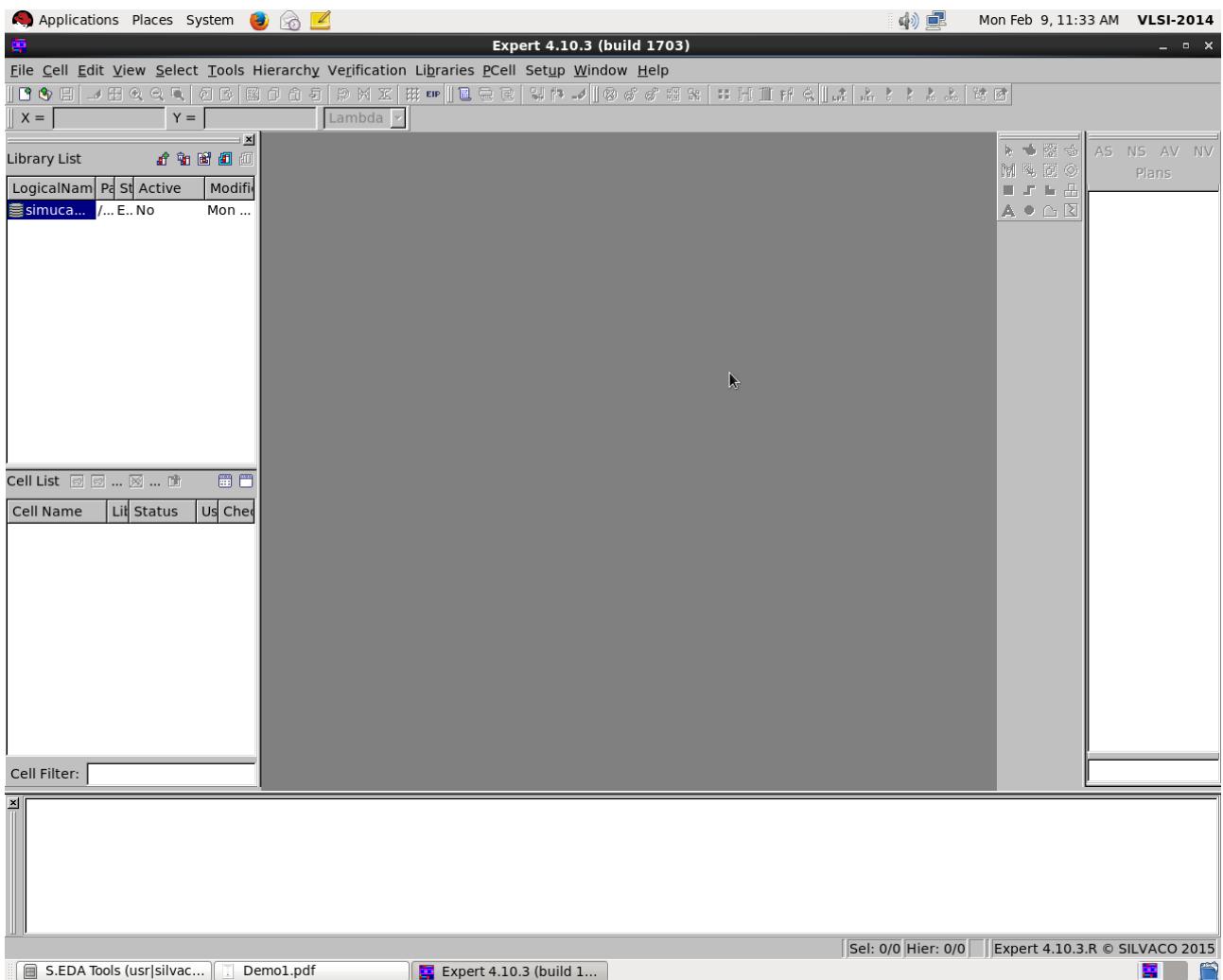


Observations:

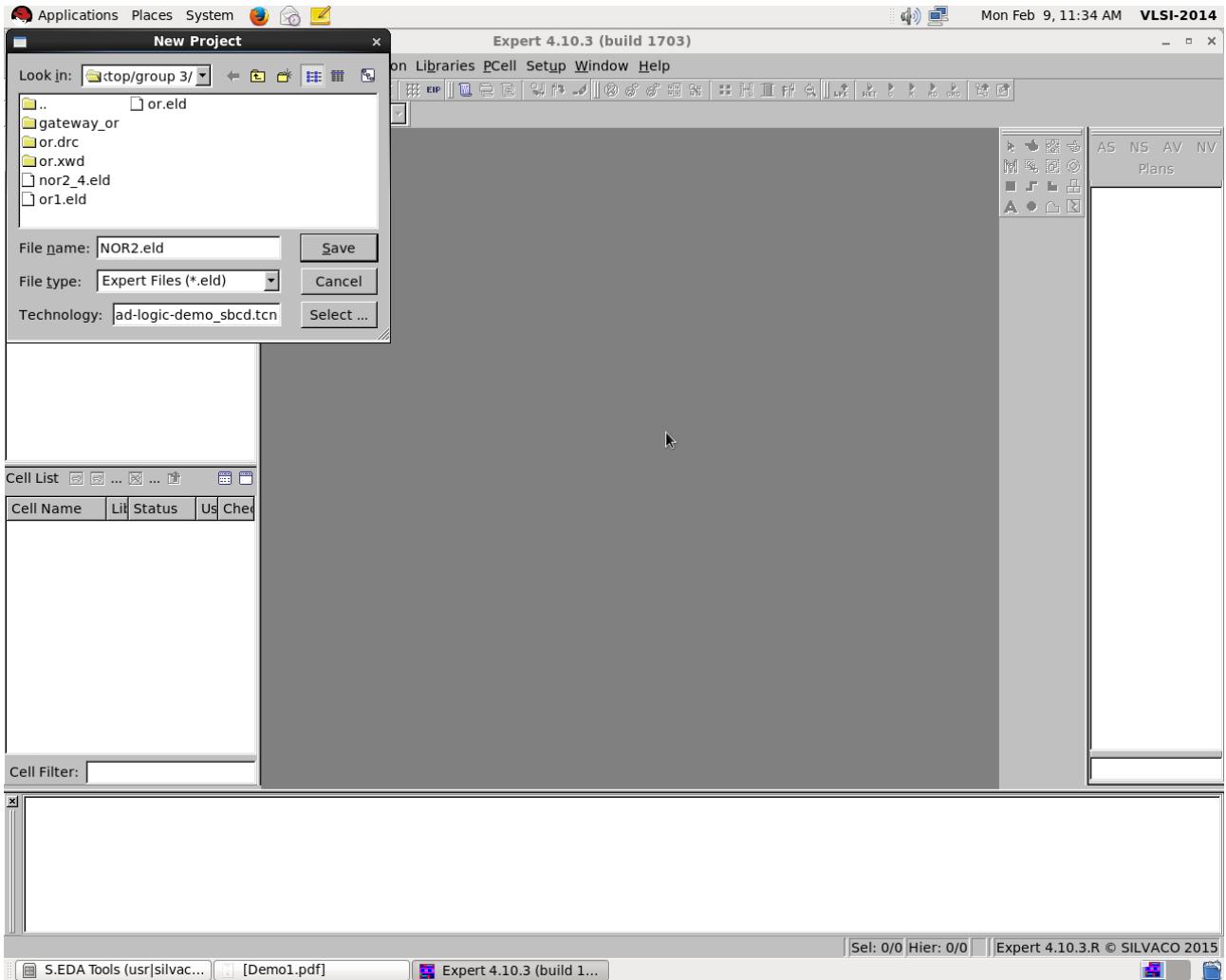
Parameters	Calculated Value	Simulated Value	Change in parameters
Average power dissipation	2uW	2.037uW	increases
Worst case average power dissipation	72uW	69.76uW	increases
Maximum power dissipation	72uW	69.76uW	increases
Minimum power dissipation	40 uW	39.96uW	increases
Leakage current	20nA	18.736nA	decreases
Leakage power	40nW	37.472nW	decreases
Worst case leakage current	30nA	28.56nA	decreases
Worst case leakage power	60nW	57.02nW	decreases
Propagation delay	10.8nsec	11.39nsec	decreases

Layout design of CMOS NOR2

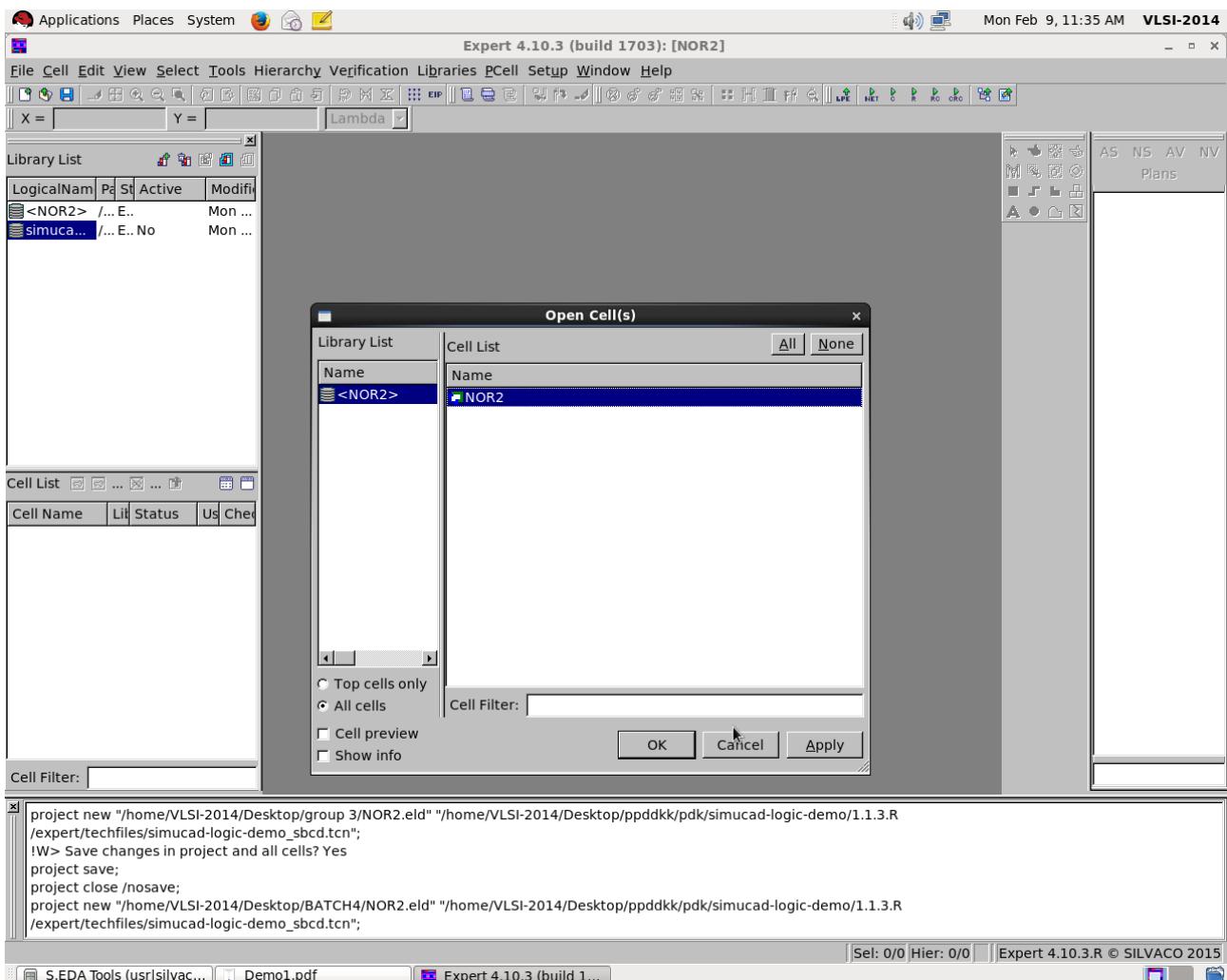
- A layout window will be open by double clicking on Expert icon which is in S. EDA shortcuts folder.



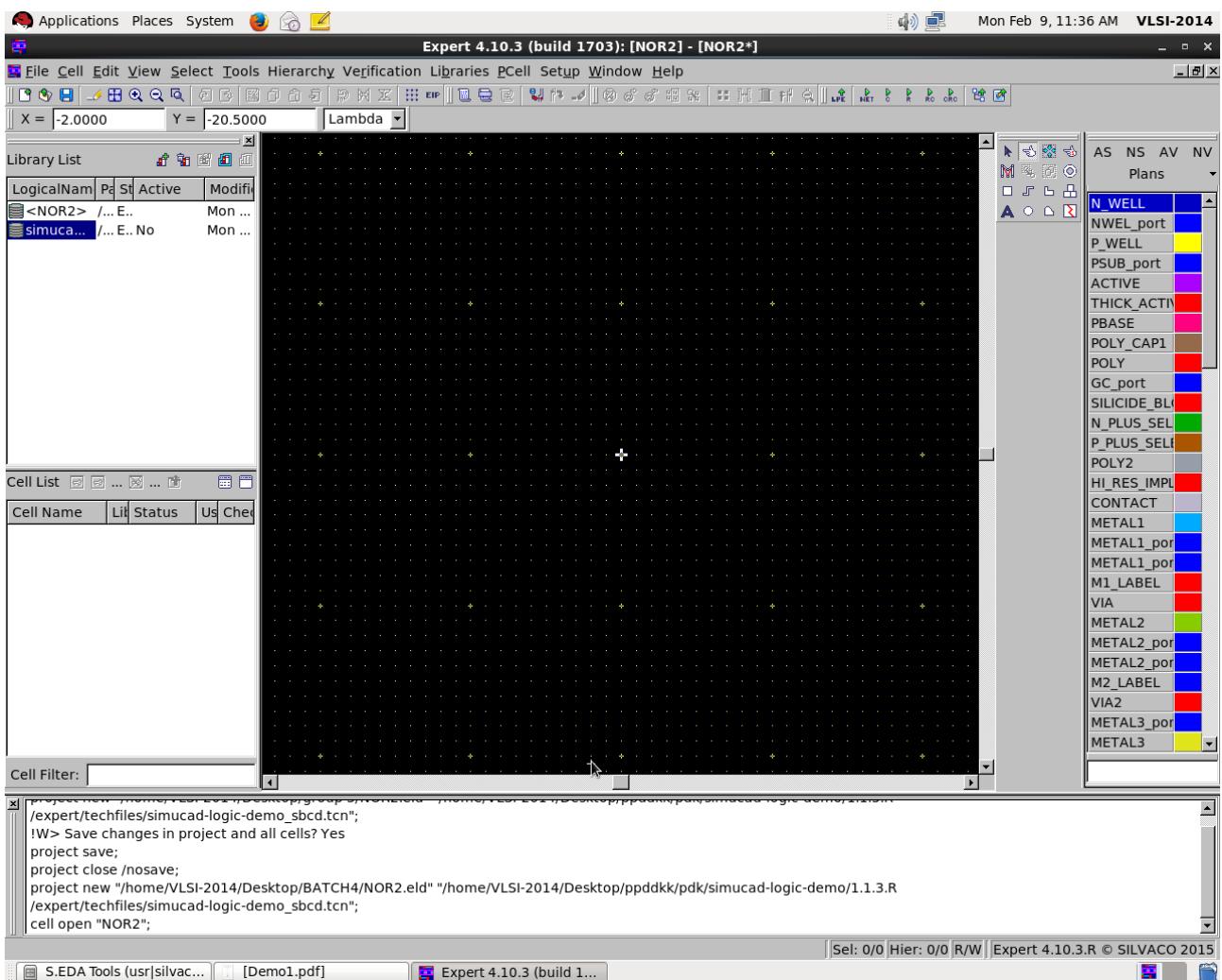
- Add new project by File-New-New Project.
- Enter new project file name.
- Set the technology file by selecting the proper path from your working directory.



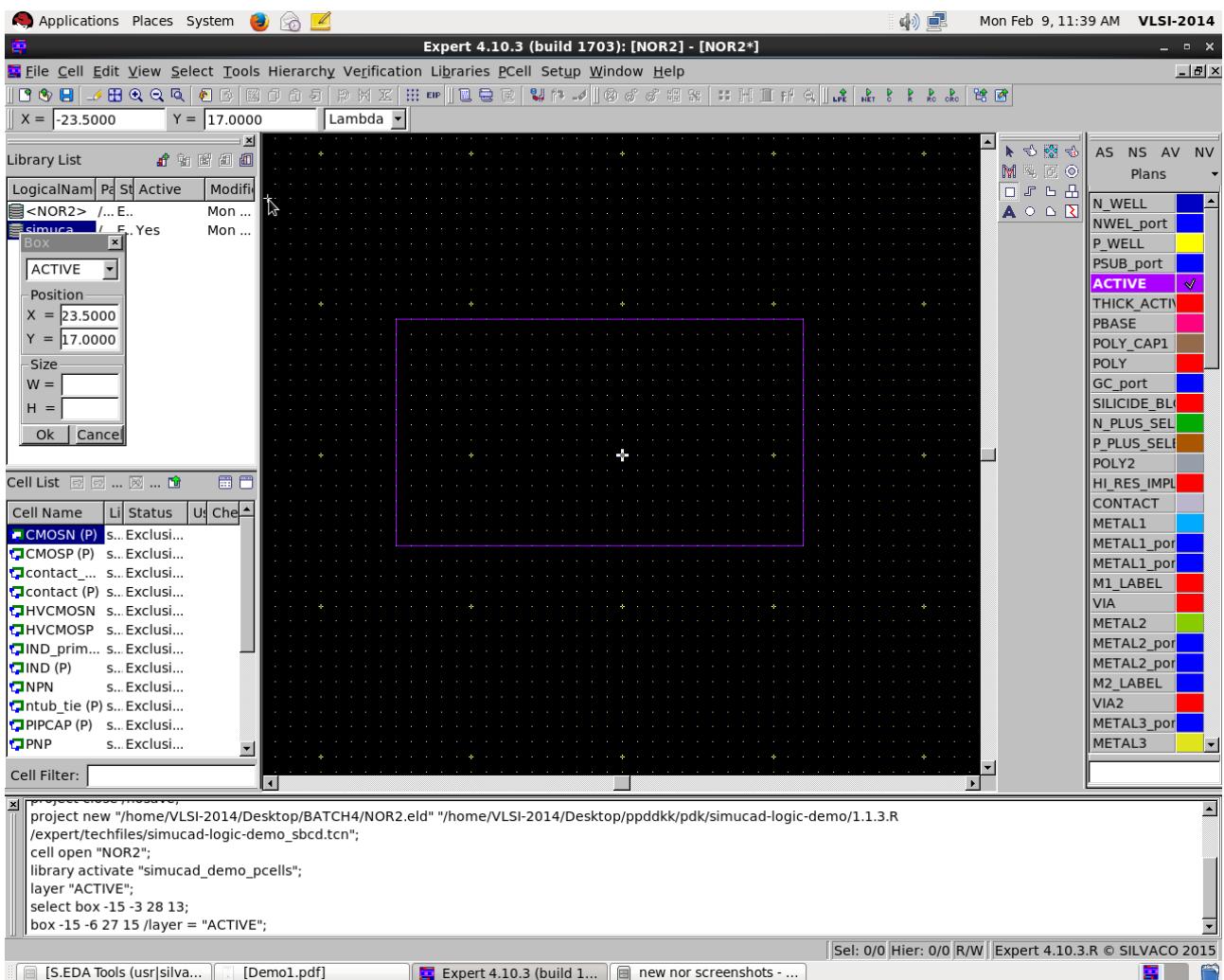
- Save or modified the cell name of the current project.



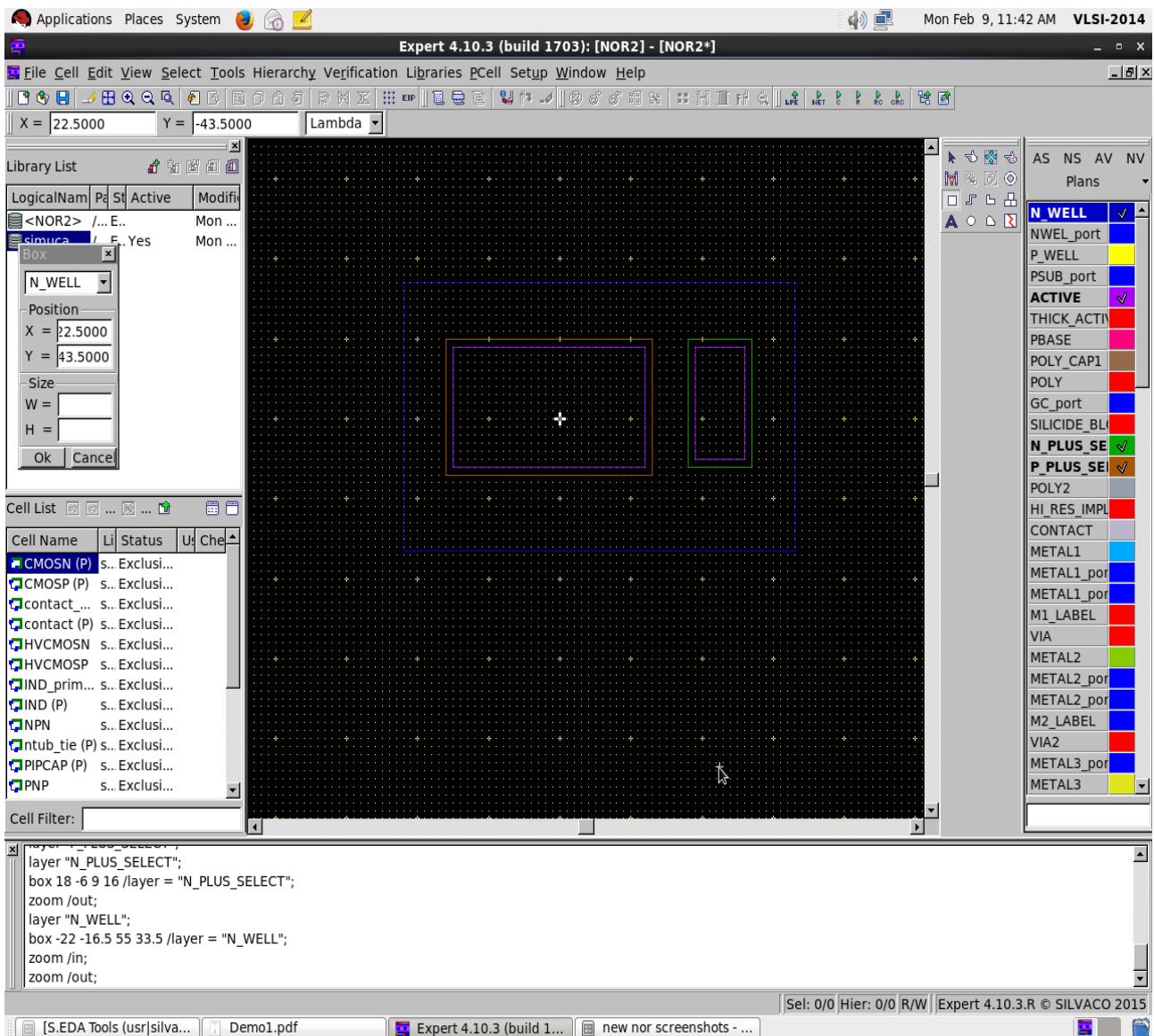
- A work space will be open containing different colour layers.
- Add layout library by clicking on, Libraries-Setup.



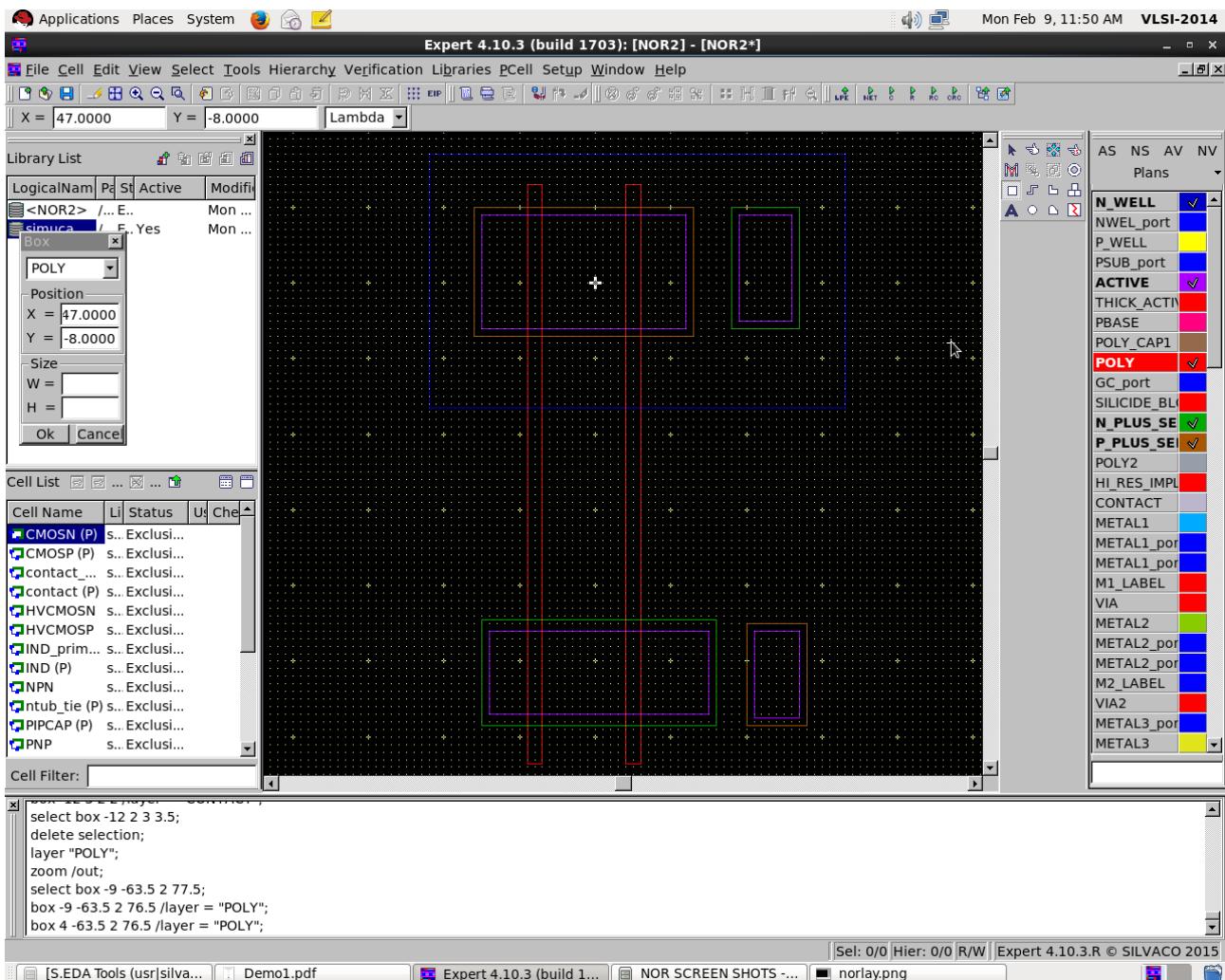
- Activate the current working libraries.
- Start to draw the inverter layout.
- Use design tools for selecting the different shapes of the layers.
- A property window will be open during drawing the layers.
- We can use these property windows for modify the layer dimensions.



- Follow the basic rules of drawing the layout.



- Layout design tools can be used to modify the layers.
- A layer can be move by selecting the move icon in design tool.



- A good practice of layout design is checking the rules layers to layers by clicking on DRC script panel.
 - A DRC Script Panel will be open in new window.
 - Set the DRC rule file by, File-Open-DRC File.
 - DRC file will be open in DRC Script Panel window.
 - Run DRC script.

Applications Places System

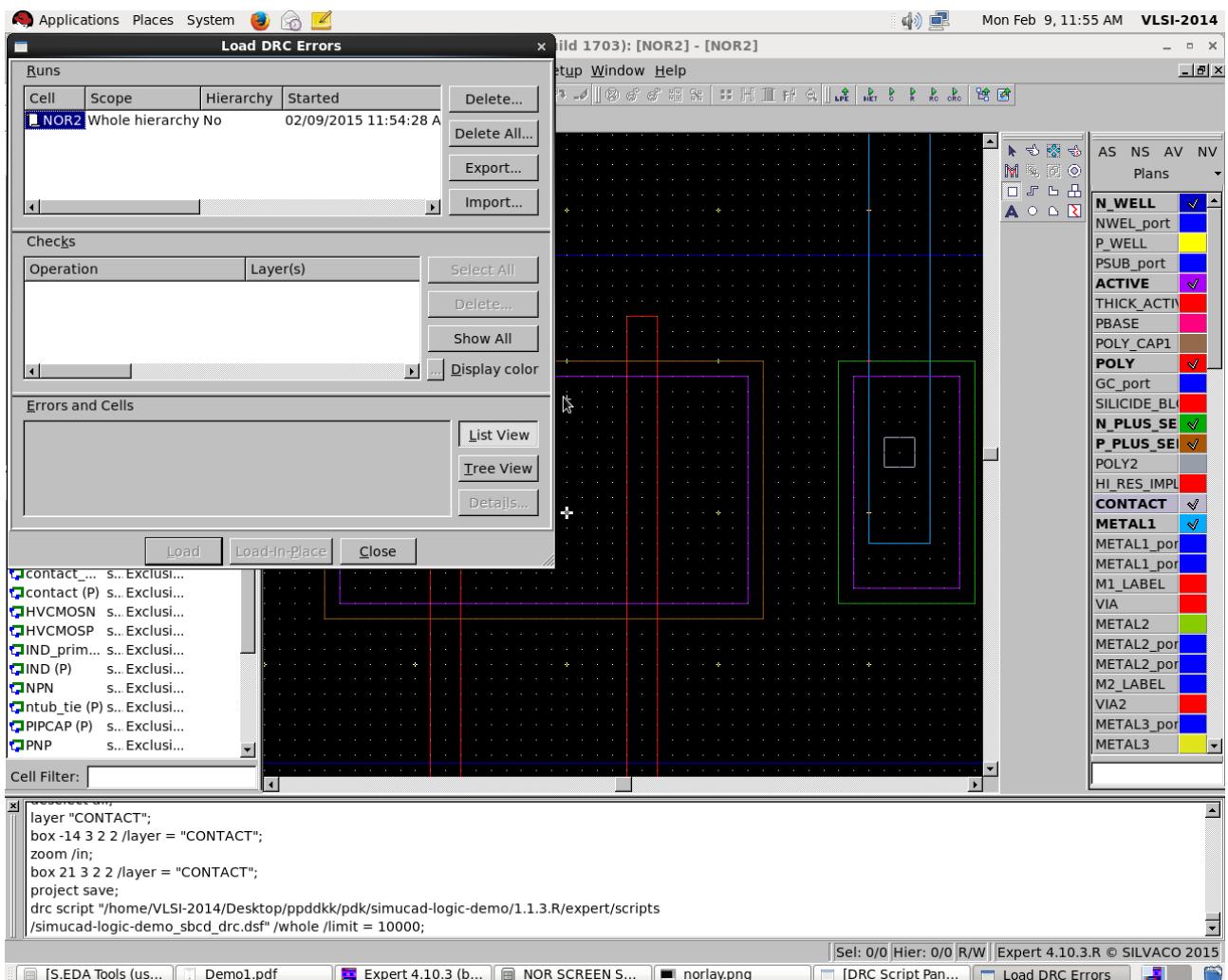
Mon Feb 9, 12:02 PM VLSI-2014

DRC Script Panel - [/home/VLSI-2014/Desktop/ppddkk/pdk/simucad-logic-demo/1.1.3.R/expert/scripts/simucad-logic-demo_sbcd_drc.dsf - [NOR2](auto)]

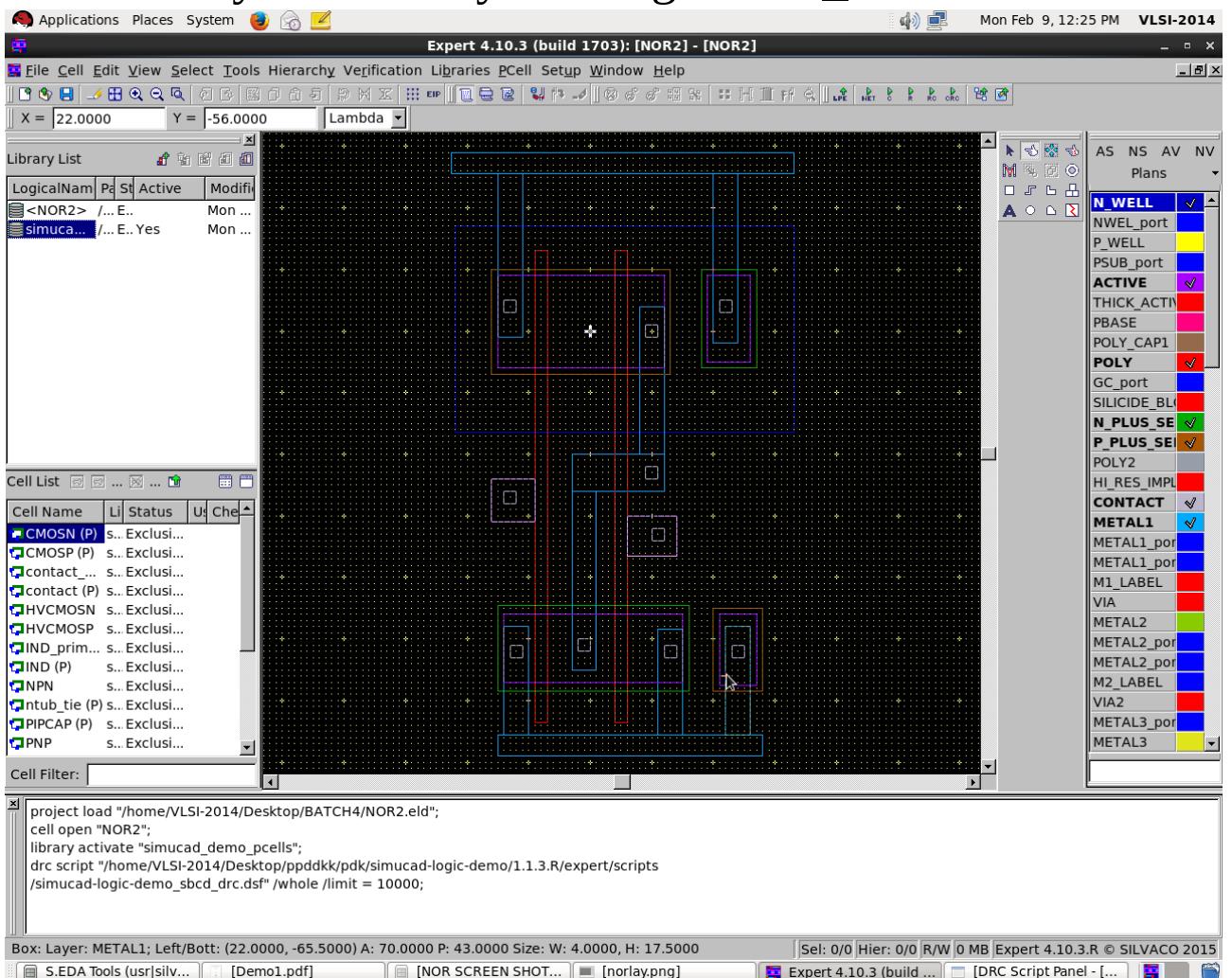
File Edit Find Insert DRC Setup Window

Update_layout: input=no, technology=no, new=no;
output_error_subsegments: yes;
Merge_Input: on;
//////////
// Global Defines //
//////////
Substrate: LayerR=&A;
Logicform: PSUB=&A.dif.(N_WELL.or.DEEP_N_WELL);
Logicform: Nactive_in_PWELL=(N_PLUS_SELECT.and.ACTIVE.and.PSUB);
Logicform: ISOPWELL=DEEP_N_WELL.dif.N_WELL;
Logicform: Nactive_in_ISOPWELL=(N_PLUS_SELECT.and.ACTIVE.and.ISOPWELL);
Logicform: Pactive_in_NWELL=P_PLUS_SELECT.and.ACTIVE.and.N_WELL;
Logicform: NWELL_TIE=N_PLUS_SELECT.and.ACTIVE.AND.N_WELL;
Logicform: PSUB_TIE=(P_PLUS_SELECT.and.ACTIVE).DIF.N_WELL;
Logicform: SD_ACTIVE=(P_PLUS_SELECT.and.ACTIVE.AND.N_WELL).or.((N_PLUS_SELECT.and.ACTIVE).DIF.N_WELL);
Logicform: SUB_TIE_ACTIVE=(NWELL_TIE).or.(PSUB_TIE);
//////////
// Connectivity Defines //
//////////
Connect: Layer1=N_WELL, Layer2=NWELL_TIE ,LayerC=CONTACT, Options =(l-);
Connect: Layer1=PSUB, Layer2=PSUB_TIE ,LayerC=CONTACT, Options =(l-);
//////////
//Rules for N_WELL
//////////
//1.1 Minimum width
Select: Relation=overlap, Layer1=N_WELL, layer2=THICK_ACTIVE, LayerR=REG_NWELL, Options=(not);
Width: Layer = REG_NWELL, Limits<10, ID= "1.1 Minimum width";
//1.2 Minimum spacing between wells at different potential
OutDistance: Layer = N_WELL, Limits<9 , Options=(C), ID= "1.2 Minimum spacing between wells at different potential";
//1.3 Minimum spacing between wells at same potential
OutDistance: Layer = N_WELL, Limits<6, Options=(N,C'), ID= "1.3 Minimum spacing between wells at same potential";
//1.4 Minimum spacing between wells of different type (if both are drawn)
Logicform: OVERLAPPING_WELLS=(N_WELL).and.(P_WELL);
Copy: Layer=OVERLAPPING_WELLS, ID="1.4 Minimum spacing between wells of different type (if both are drawn)";
//////////
//Rules for ACTIVE
//////////
//2.1 Minimum width
Width: Layer = ACTIVE, Limits<2.5 , ID= "2.1 Minimum width";
//2.2 Minimum spacing
OutDistance: Layer = ACTIVE, Limits<3 , Options=(N), ID= "2.2 Minimum spacing";
//2.3 Source/drain active to well edge
InDistance: Layer1 = SD_ACTIVE, Layer2 = N_WELL, Limits<5 , Options=(T), ID= "2.3 Source/drain active to well edge";

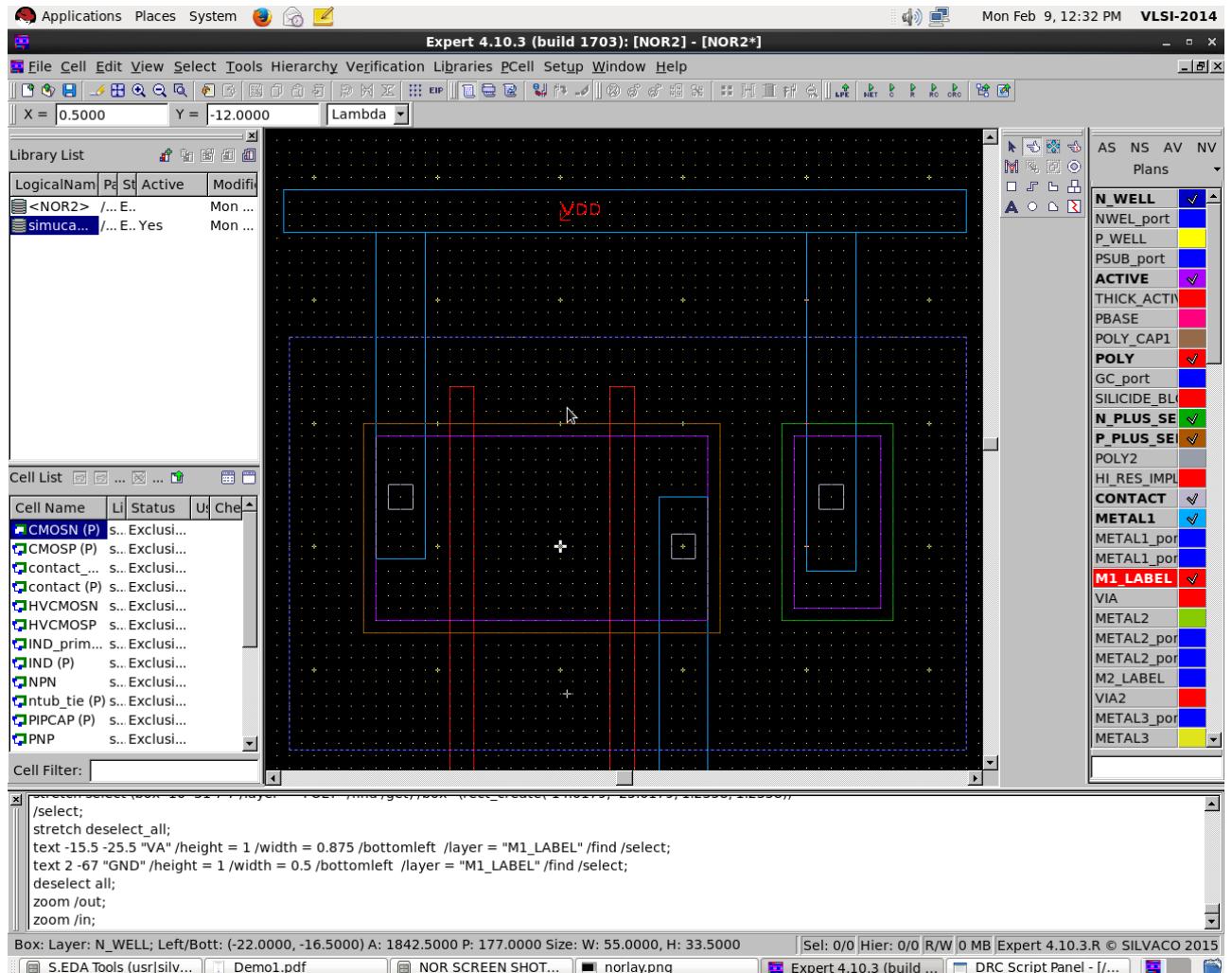
- After running DRC Script, click on “Load Errors” icon in Expert layout window.
- A new window showing DRC Errors will be open.
- If there is any error, then it will display under Checks category in Load DRC Errors window.



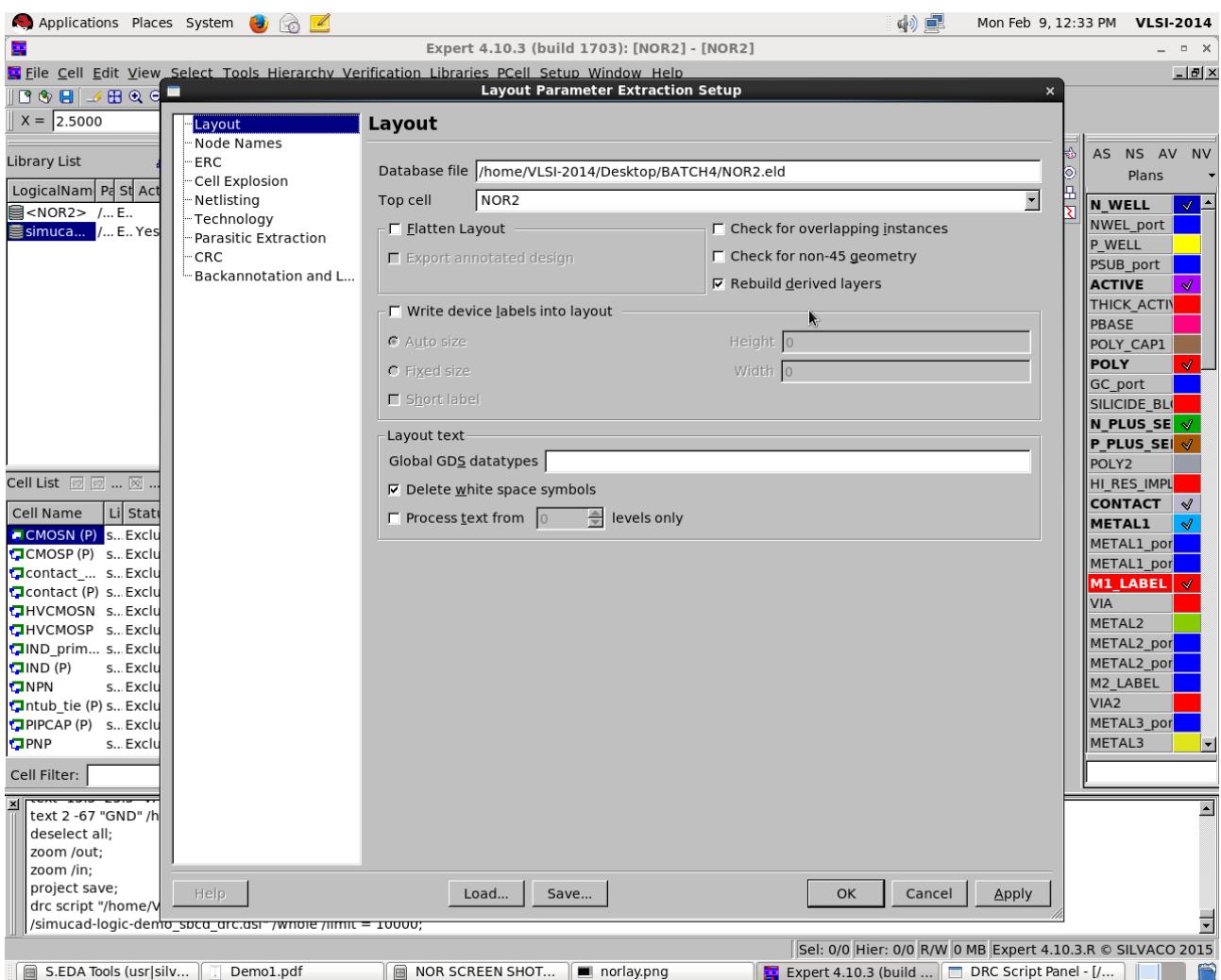
- Add layers name by clicking on M1_LABEL.



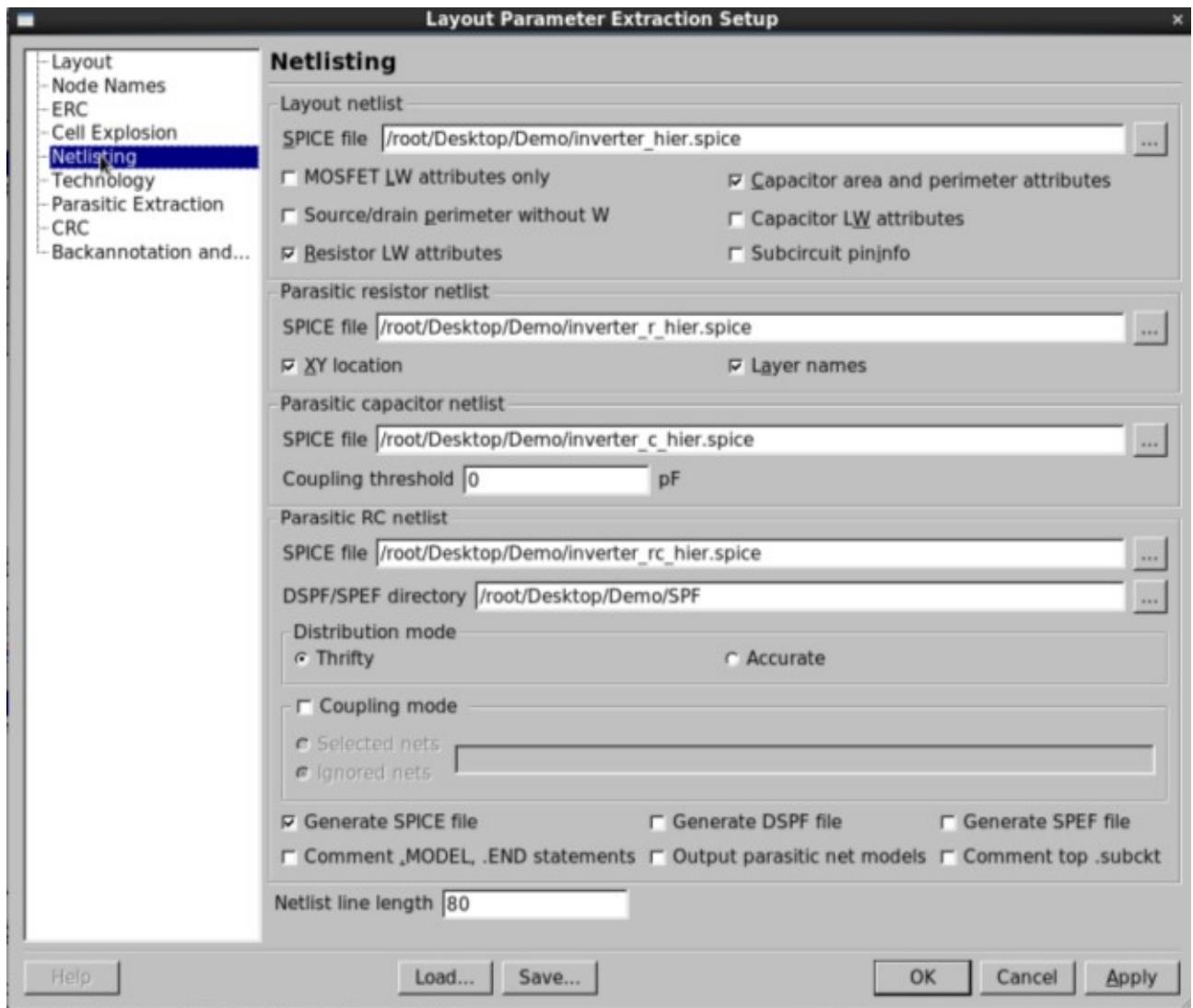
- Use create text tool for layers naming.



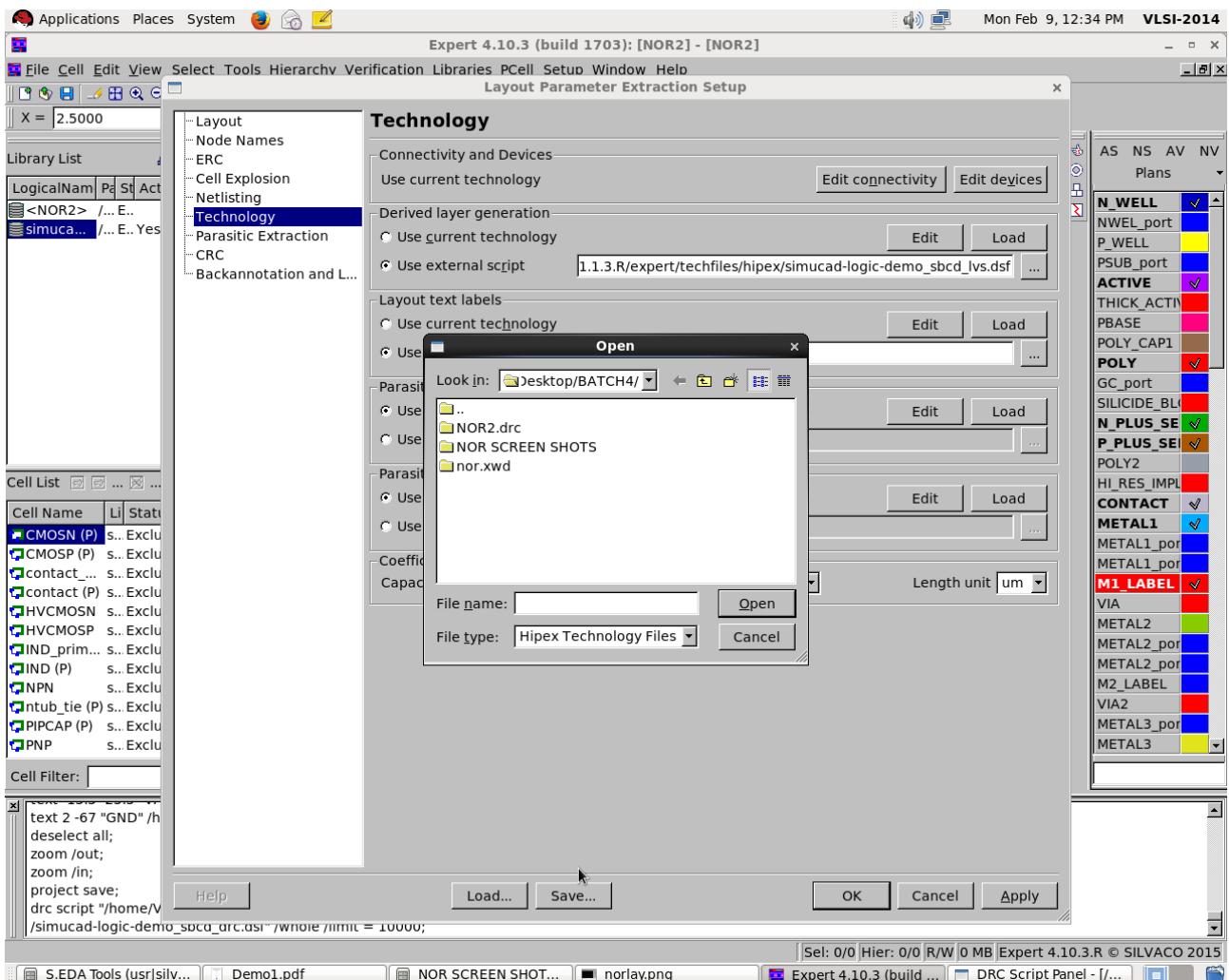
- Click on LPE Setup icon for layout parameter extractions.
- A new LPE setup window will be open.



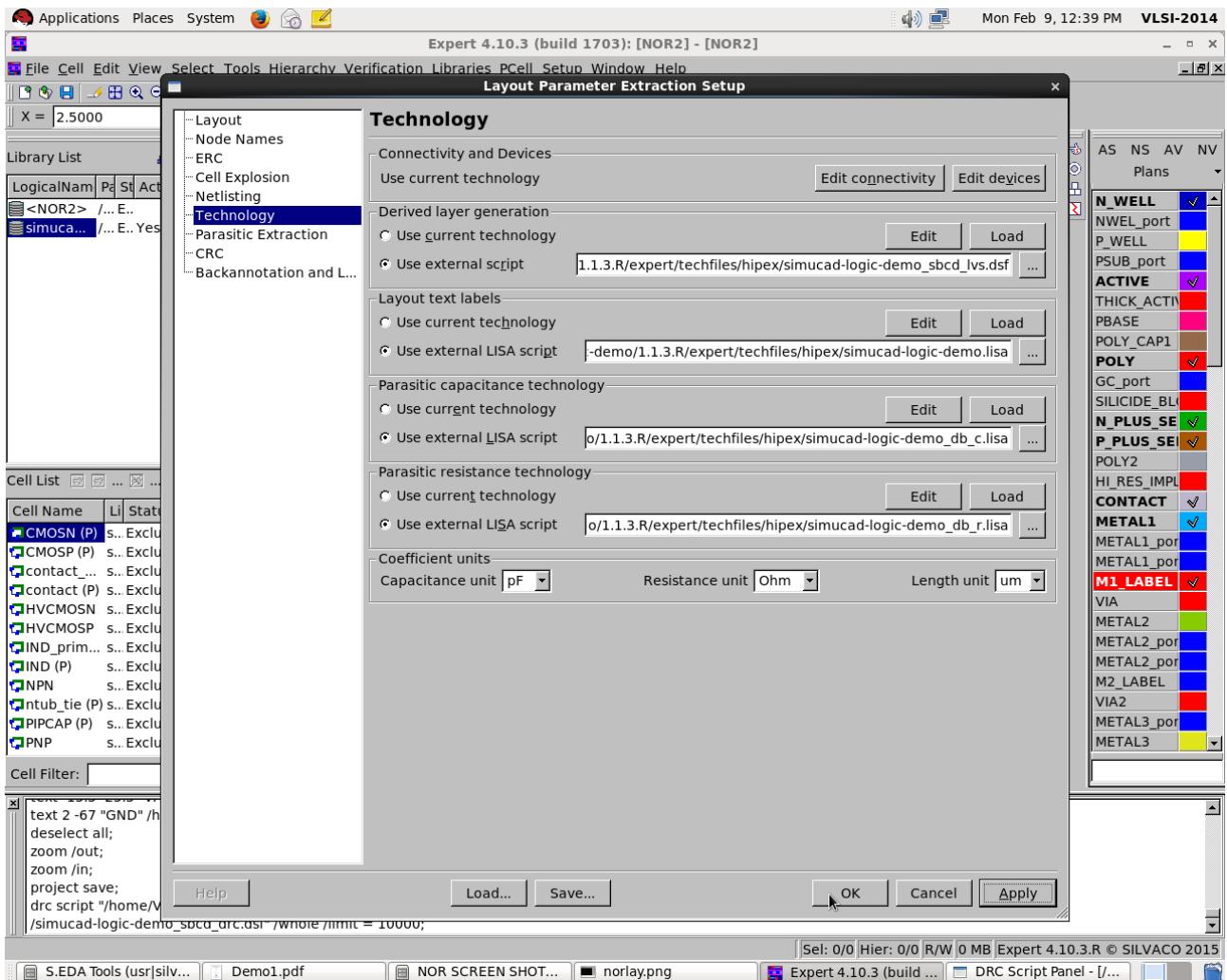
- Select Netlisting and provide the paths for different spice files.



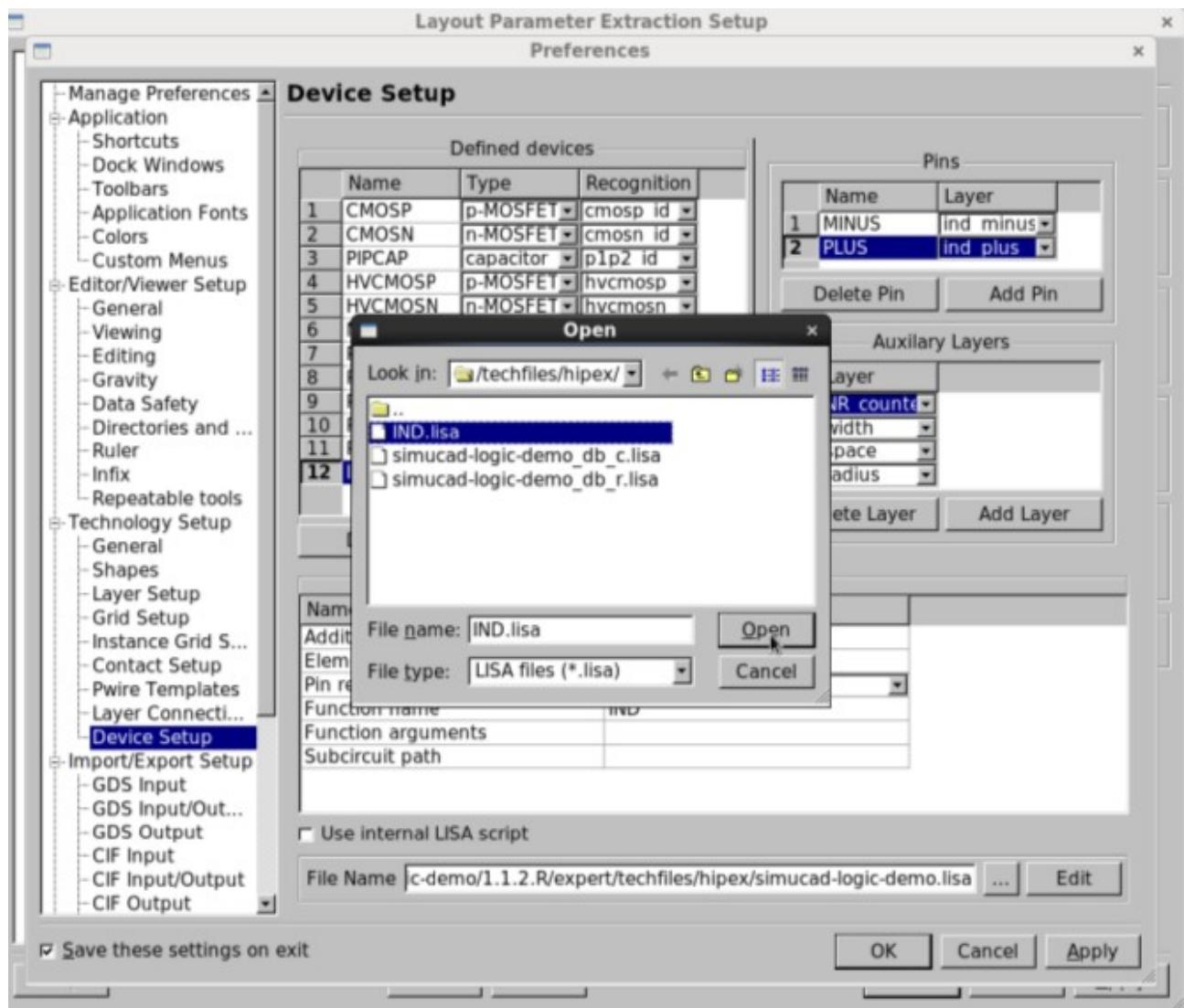
- Select technology and provide the files paths for different purposes.



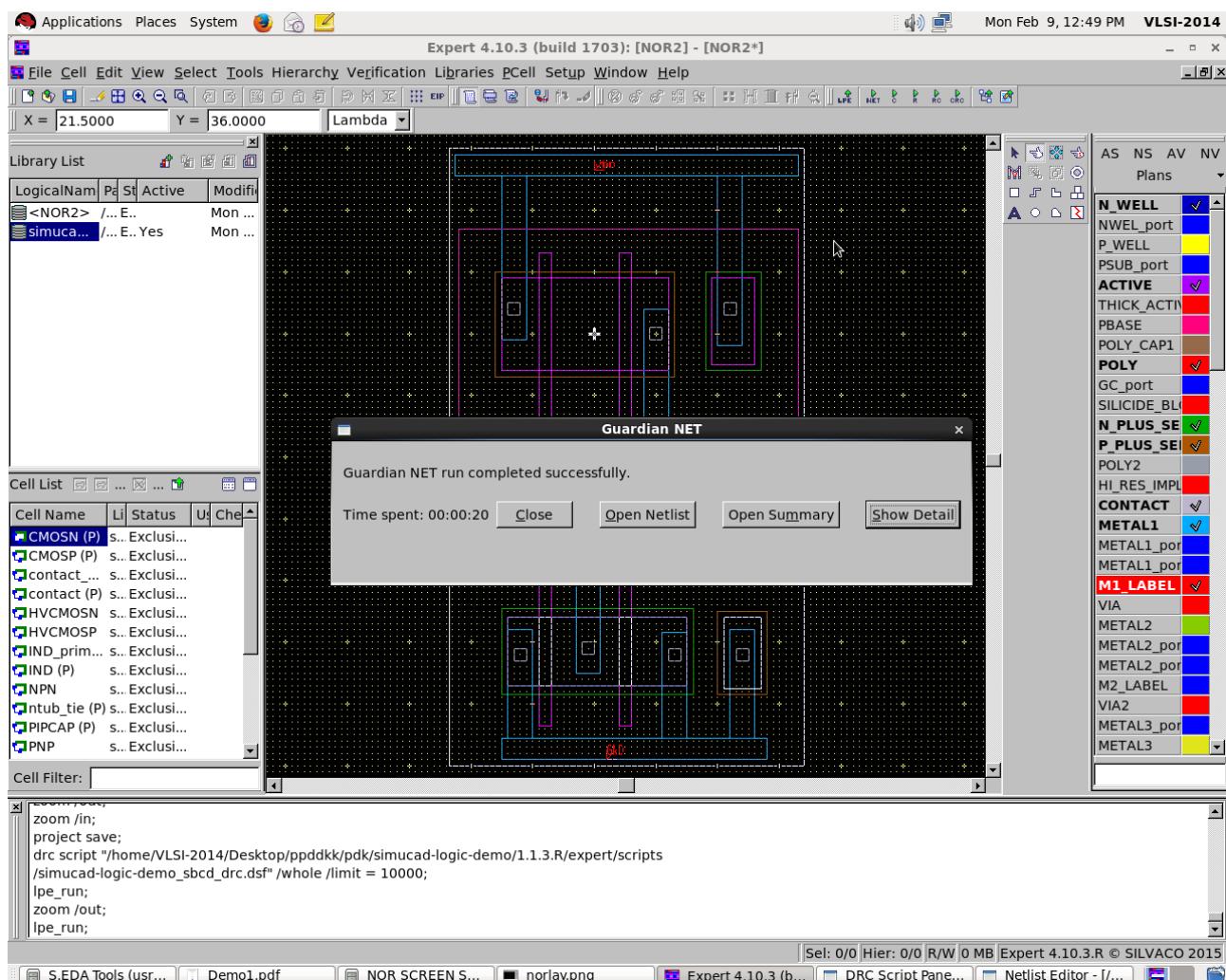
- Select file paths for parasitic capacitance and parasitic resistance technologies.



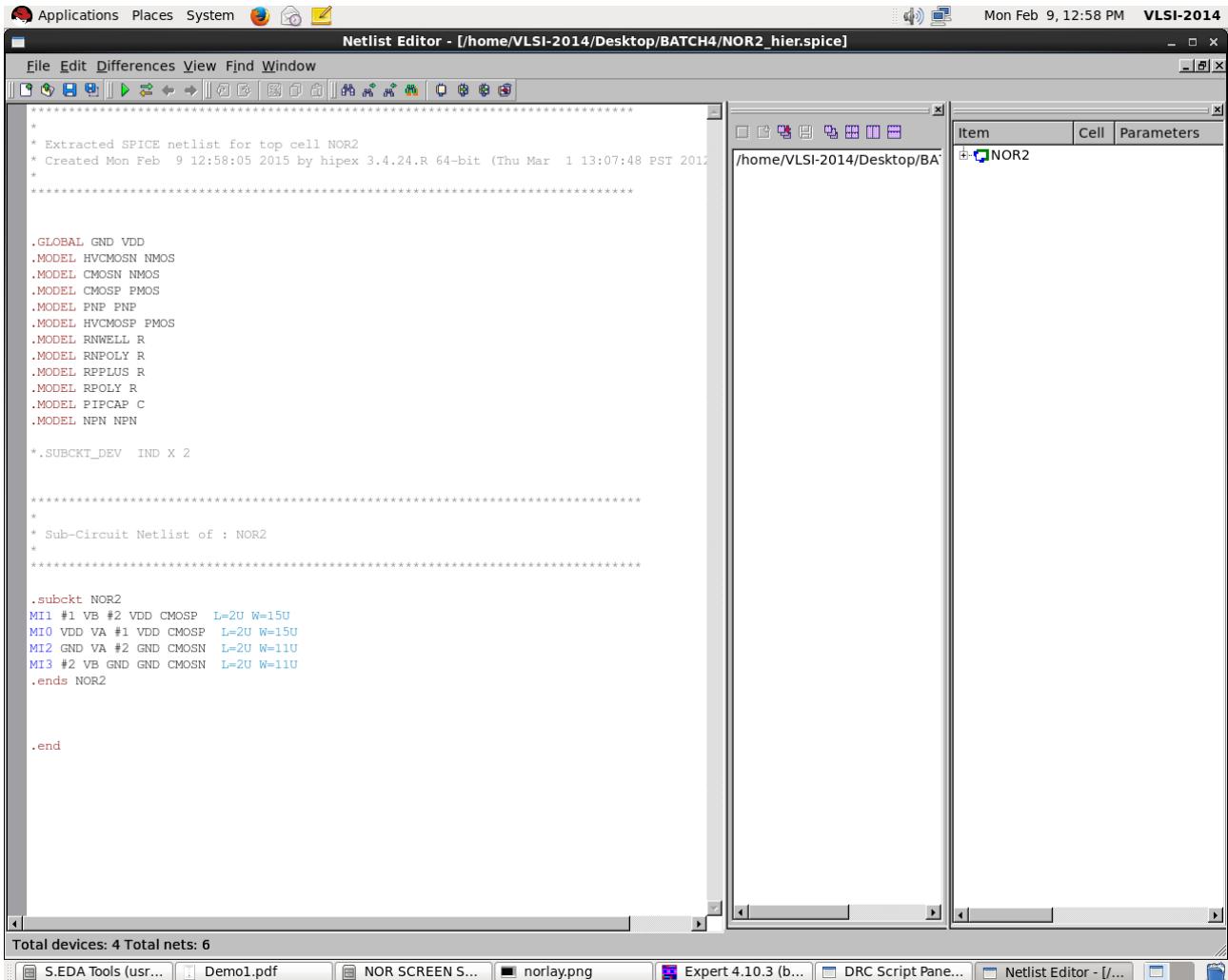
- Set the definition file for inductor through, Setup-Technology-Device Setup.



- Run netlist extractor for spice netlist.
- A successful message will be display.



- By clicking on open netlist in Guardian NET window, new netlist window will be open.



The screenshot shows the Netlist Editor interface with the following details:

- Title Bar:** Applications Places System Mon Feb 9, 12:58 PM VLSI-2014
- Menu Bar:** File Edit Differences View Find Window
- Toolbars:** Standard toolbar with icons for file operations, zoom, and search.
- Netlist Editor Area:**

```

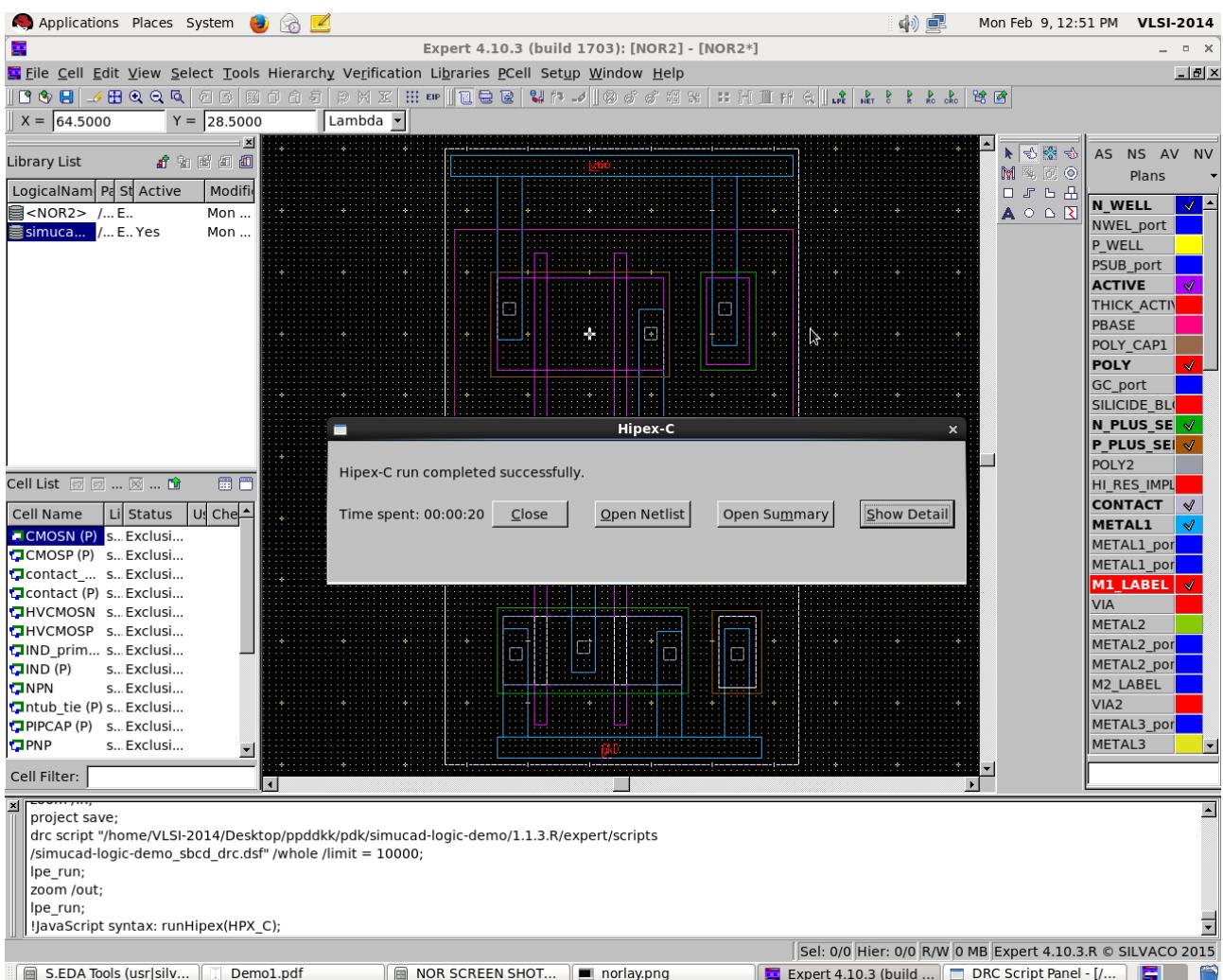
* Extracted SPICE netlist for top cell NOR2
* Created Mon Feb 9 12:58:05 2015 by hipex 3.4.24.R 64-bit (Thu Mar 1 13:07:48 PST 2012)
*
*****GLOBAL***** GND VDD
.MODEL HVCMOSN NMOS
.MODEL CMOSN NMOS
.MODEL CMOSP PMOS
.MODEL PNP PNP
.MODEL HVCMOSP PMOS
.MODEL RNWELL R
.MODEL RNPOLY R
.MODEL RPPLUS R
.MODEL RPOLY R
.MODEL PIPCAP C
.MODEL NPN NPN
*
*.SUBCKT_DEV IND X 2

*****
* Sub-Circuit Netlist of : NOR2
*
*****
.subckt NOR2
M1 #1 VB #2 VDD CMOSP L=2U W=15U
M10 VDD VA #1 VDD CMOSP L=2U W=15U
M12 GND VA #2 GND CMOSN L=2U W=11U
M13 #2 VB GND GND CMOSN L=2U W=11U
.ends NOR2

.end

```
- Right Panel:** A tree view of the project structure under "/home/VLSI-2014/Desktop/BATCH4". The "NOR2" node is selected.
- Bottom Status Bar:** Total devices: 4 Total nets: 6
- Bottom Taskbar:** Shows multiple open windows: S.EDA Tools (usr...), Demo1.pdf, NOR SCREEN S..., norlay.png, Expert 4.10.3 (b...), DRC Script Pane..., Netlist Editor - [/...], and a folder icon.

- Run Hipex-C tool for capacitance values extraction.
- A successful message of Hipex-C will be open.



- You can read the file by open the Hipex-C extracted file.

Applications Places System Mon Feb 9, 3:57 PM VLSI-2014

File Edit Differences View Find Window

Netlist Editor - [/home/VLSI-2014/Desktop/BATCH4/nor_r_hier.spice]

```
* Extracted SPICE netlist for top cell NOR2
* Created Mon Feb 9 15:56:40 2015 by hipex 3.4.24.R 64-bit (Thu Mar 1 13:07:48 PST 2012)
*
*****GLOBAL VDD GND
*.MODEL HVMOSN NMOS
*.MODEL CMOSN NMOS
*.MODEL CMOSP PMOS
*.MODEL PNP PNP
*.MODEL HVMOSP PMOS
*.MODEL RNWELL R
*.MODEL RNPOLY R
*.MODEL RPPLUS R
*.MODEL RPOLY R
*.MODEL PIPCAP C
*.MODEL NPN NPN
*.SUBCKT_DEV IND X 2

*****
* Sub-Circuit Netlist of : NOR2
*
**** Parasitic capacitors ***
Cp1 VB #2 559.659A
Cp2 VB GND 728.913F
Cp3 VDD GND 18.4225F
Cp4 VA GND 718.261F
Cp5 #2 GND 12.3923F

.ends NOR2

*.end
```

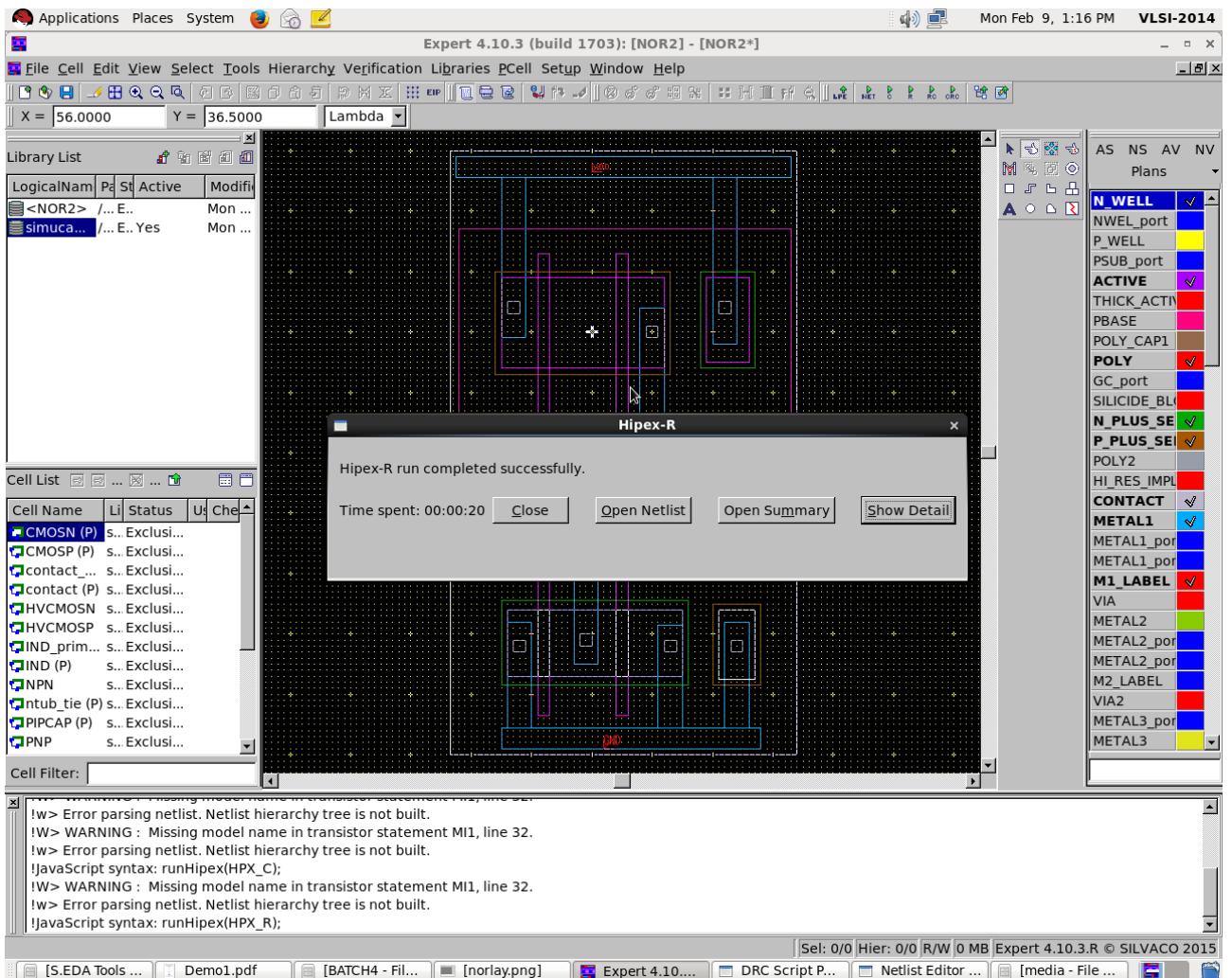
item Cell Parameters

+ NOR2

Ln 7, Col 1

[S.EDA Tools (usr|sil...) Expert 4.10.3 (build ... [DRC Script Panel - [...] [LIVE - File Browser] BATCH4 - File Browser Netlist Editor - [/hom...]

- Run Hipex-R tool for resistance values extraction.
- A successful message of Hipex-R will be display.



- Open the Hipex-R window for reading the resistance values

Applications Places System Mon Feb 9, 3:55 PM VLSI-2014

Netlist Editor - [/home/VLSI-2014/Desktop/BATCH4/NOR2_r.hier.spice]

File Edit Differences View Find Window

```

.GLOBAL VDD GND
*.MODEL HVMOSN NMOS
*.MODEL CMOSN NMOS
*.MODEL CMOSP PMOS
*.MODEL PNP PNP
*.MODEL HVMOSP PMOS
*.MODEL RNWELL R
*.MODEL RNPOLY R
*.MODEL RPPLUS R
*.MODEL RPOLY R
*.MODEL PIPCAP C
*.MODEL NPN NPN

*.SUBCKT_DEV IND X 2

*****
*
* Sub-Circuit Netlist of : NOR2
*
*****

.subckt NOR2
M11 #1 VB:6 #2:5 VDD CMOSP L=2U W=15U
M10 VDD VA:6 #1 VDD CMOSP L=2U W=15U
M12 GND VA:7 #2:4 GND CMOSN L=2U W=11U
M13 #2:4 VB:7 GND GND CMOSN L=2U W=11U

*** Parasitic resistors ***
Rp1 VB:5 VB:8 200.951461
* Layer connect_poly at (11, -33)
Rp2 VB:5 VB:9 208.081547
* Layer connect_poly at (11, -33)
Rp3 VB:8 VB:9 488.150000
* Layer connect_poly at (5, -30)
Rp4 VB:6 VB:8 599.950000
* Layer connect_poly at (5, 9.002)
Rp5 VB:7 VB:9 237.450000
* Layer connect_poly at (5, -45.998)
Rp6 VA:5 VA:8 174.672433
* Layer connect_poly at (-13, -27)
Rp7 VA:5 VA:9 191.812470
* Layer connect_poly at (-13, -27)
Rp8 VA:8 VA:9 525.700000
* Layer connect_poly at (-8, -24)
Rp9 VA:6 VA:8 449.950000
* Layer connect_poly at (-8, 9.002)

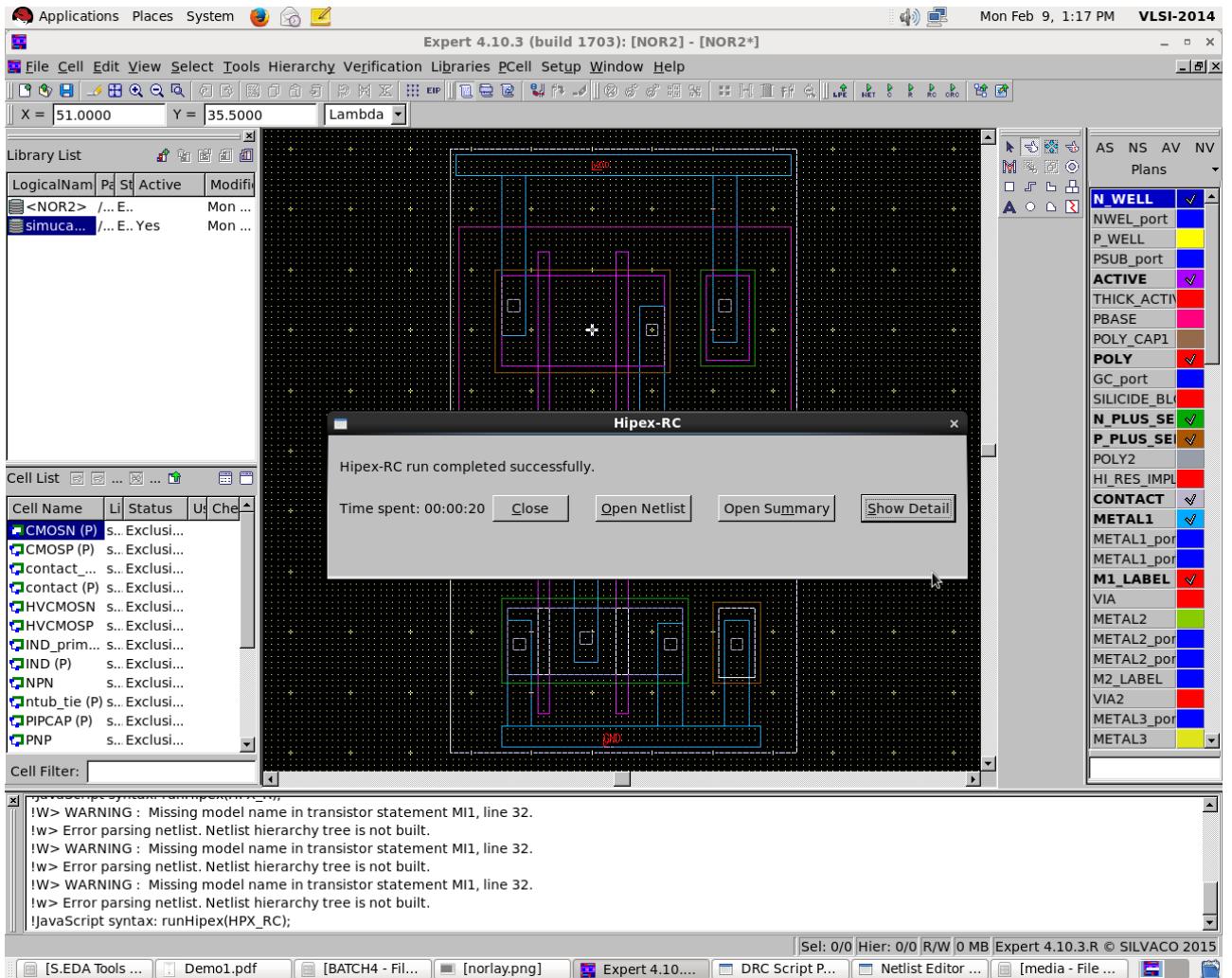
```

Item Cell Parameters

NOR2

[S.EDA Tools (usr|sil...)] [Expert 4.10.3 (build ...)] [DRC Script Panel - ...] [LIVE - File Browser] [BATCH4 - File Browser] [Netlist Editor - [/hom...]]

- Run Hipex-RC tool for extraction of combinations of resistance and capacitance values.
- A successful message will be display in new Hipex-RC window.



- Open Hipex-RC window for noting the values of resistance and capacitances.
- Use RC contain netlist for various metrics characterization.

Applications Places System Mon Feb 9, 3:58 PM VLSI-2014

Netlist Editor - [/home/VLSI-2014/Desktop/BATCH4/NOR2_rc_hier.spice]

File Edit Differences View Find Window

```
*****
.subckt NOR2
M1 #1 VB:6 #2:5 VDD CMOSP L=2U W=15U
M10 VDD VA:6 #1 VDD CMOSP L=2U W=15U
M12 GND VA:7 #2:4 GND CMOSN L=2U W=11U
M13 #2:4 VB:7 GND GND CMOSN L=2U W=11U

*** Parasitic resistors and capacitors **

Cp0 #2:13 GND 12.952F
Rp0 #2:11 #2:13 0.058333
* Layer connect_metal terminals at (8, -23) and (1, -23)
Rp1 #2:12 #2:13 0.029415
* Layer connect_metal terminals at (-1, -26) and (1, -23)
Rp2 #2:10 #2:11 0.029415
* Layer connect_metal terminals at (10, -20) and (8, -23)
Rp3 #2:5 #2:10 0.250000
* Layer connect_metal terminals at (10, 0) and (10, -20)
Rp4 #2:4 #2:12 0.312500
* Layer connect_metal terminals at (-1, -51) and (-1, -26)
Cp1 VA:5 GND 718.261F
Rp5 VA:7 VA:9 374.950000
* Layer connect_poly terminals at (-8, -45.998) and (-8, -31)
Rp6 VA:6 VA:8 449.950000
* Layer connect_poly terminals at (-8, 9.002) and (-8, -24)
Rp7 VA:8 VA:9 525.700000
* Layer connect_poly terminals at (-8, -24) and (-8, -31)
Rp8 VA:5 VA:9 191.812470
* Layer connect_poly terminals at (-13, -27) and (-8, -31)
Rp9 VA:5 VA:8 174.672433
* Layer connect_poly terminals at (-13, -27) and (-8, -24)
Cp2 VB:5 GND 729.472F
Rp10 VB:7 VB:9 237.450000
* Layer connect_poly terminals at (5, -45.998) and (5, -36.5)
Rp11 VB:6 VB:8 599.950000
* Layer connect_poly terminals at (5, 9.002) and (5, -30)
Rp12 VB:8 VB:9 488.150000
* Layer connect_poly terminals at (5, -30) and (5, -36.5)
Rp13 VB:5 VB:9 208.081547
* Layer connect_poly terminals at (11, -33) and (5, -36.5)
Rp14 VB:5 VB:8 200.951461
* Layer connect_poly terminals at (11, -33) and (5, -30)
Cp3 VDD GND 18.4225F

.ends NOR2
```

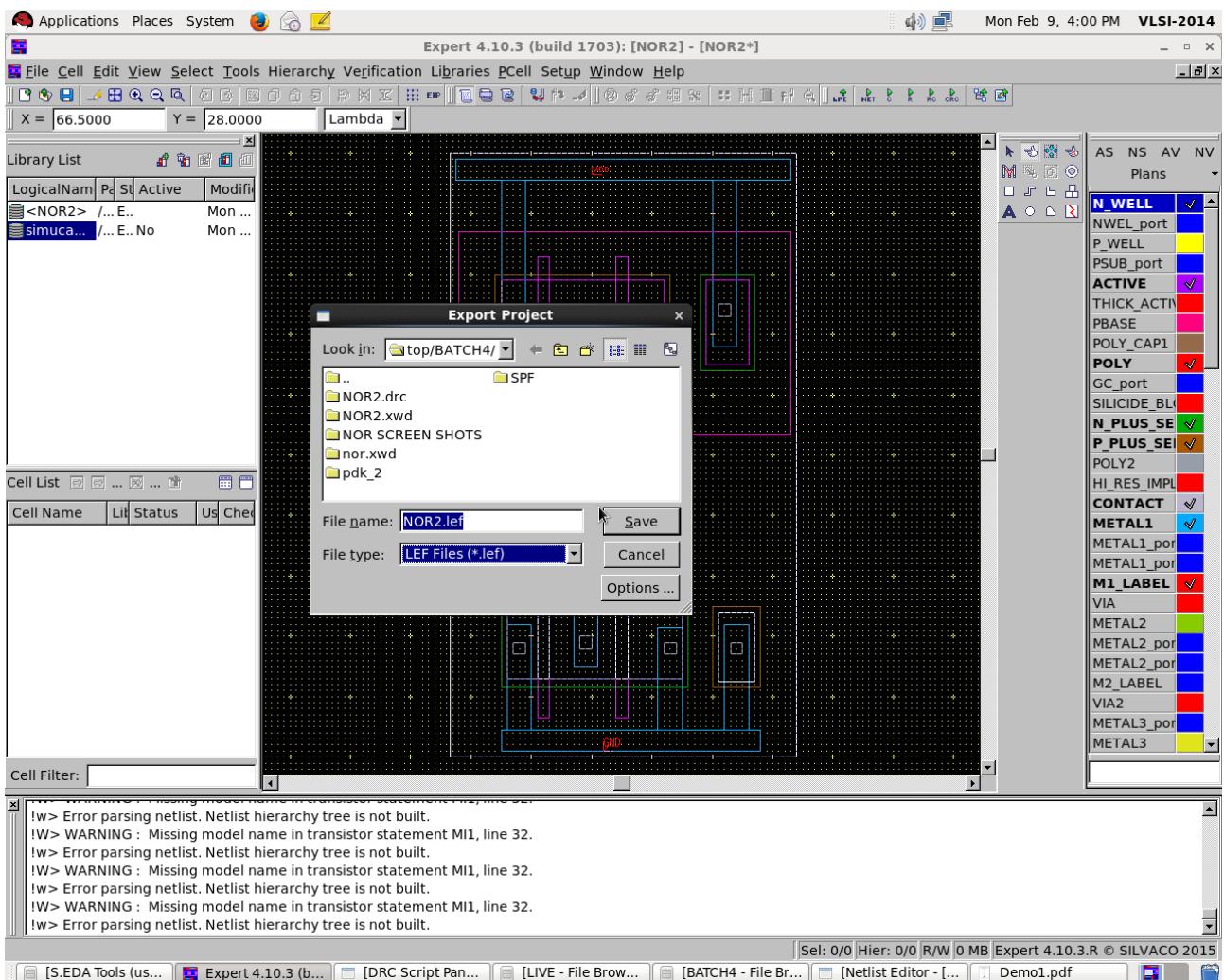
Item Cell Parameters

+ NOR2

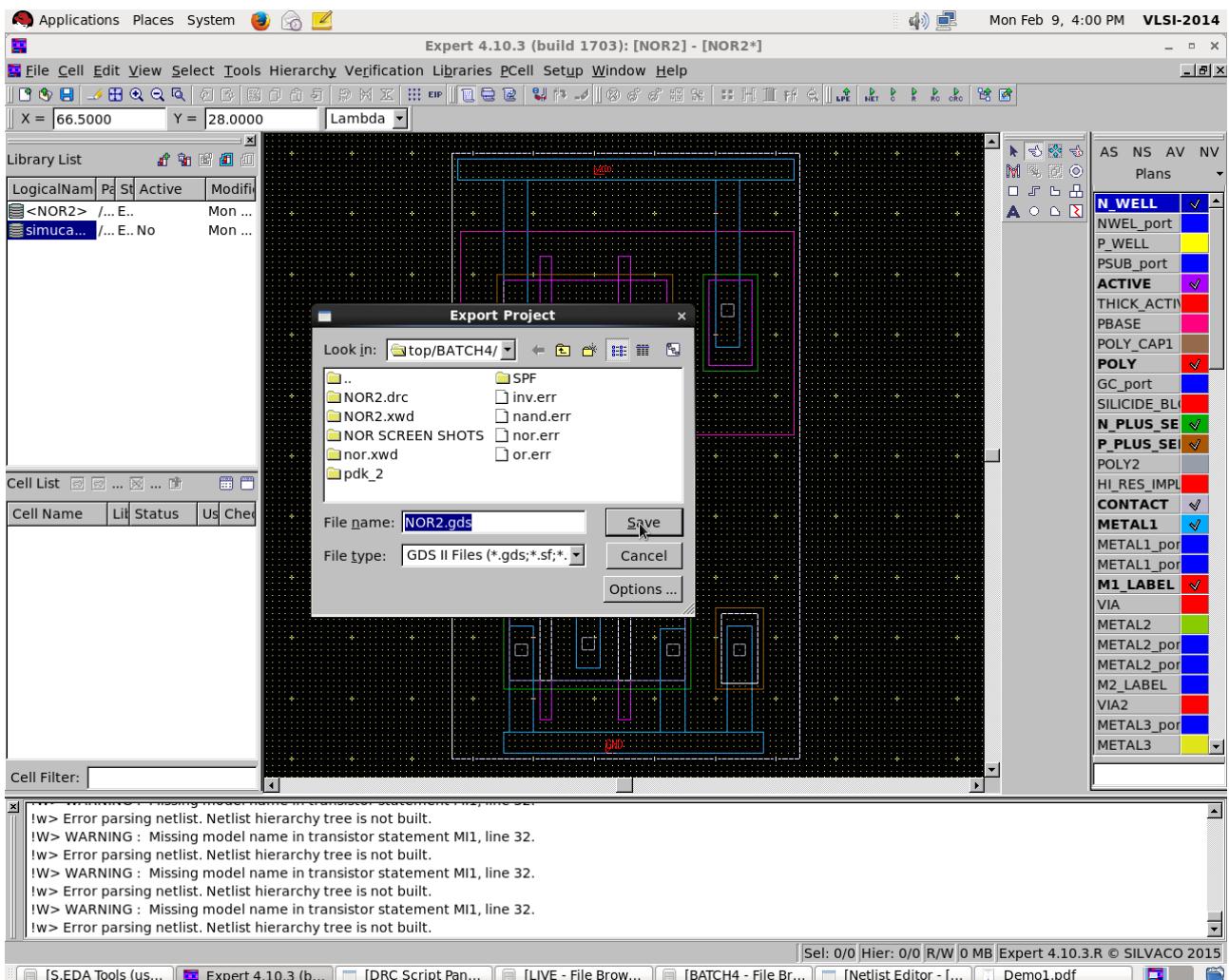
Ln 7, Col 1

[S.EDA Tools (usr|sil...], [Expert 4.10.3 (build ...], [DRC Script Panel - [...], [LIVE - File Browser], [BATCH4 - File Browser], [Netlist Editor - [/hom...]]

- Export the verified layout for different file formats.
- File-Export-Export Project.**
- Export for lef format.



- Export the layout for gdsII format.



- Export for def format.

