Assignment 5
Due: 11:59 pm, November 24th, 2015

Purpose: Understand memory access behavior and effects of memory coalescing
Target Machines: Your program must run on PACE using gcc 4.9
Assignment: Write a memory coalescing mechanism and a memory mapping scheme, generate memory trace files from your emulator (one per run), and feed the trace files into Dinero IV cache simulator. You may also integrate Dinero directly into your emulator if you prefer. Dinero IV does not handle data from the memory accesses or simulate access times, it will only simulate memory accesses using the trace file and return the overall hit rate. Submit one or more graphs of the cache hit ratio relative to 1.) cache line size and 2.) memory mapping scheme for each version of each application.

1. You are provided with two applications: Vecsum and Scan
2. Each applications have two versions: 8 threads/warp and 16 threads/warp
3. Implement a memory coalescing mechanism that can merge multiple requests from the same warp. Requests to the same cache line are coalesced. Must be aware of cache line size. Try to minimize the number of memory requests.
4. Produce a memory trace in the Dinero trace format: see item 9
5. Implement a memory mapping from address generated from the program to another mapping in the cache to increase the number of coalesced accesses. This is dependent on the application, so create a unique mapping for each application (create 2 memory mappings). An example mapping could be swapping bits 3-7 with bits 16-19 of the address, if threads in a warp were accessing consecutive addresses at bits 16-19.
6. You may wish to look at the performance profile thread on Piazza to optimize your code if it does not run fast (seconds).
7. Dinero IV: http://pages.cs.wisc.edu/~markhill/DineroIV/
8. Dinero IV user guide: http://www.ece.mtu.edu/faculty/rmkieckh/cla/4173/DINERO/d4-man.pdf
9. From the bottom of page 2 in d4-man.pdf:
   D The extended ‘‘din’’ format of Dinero IV. Three fields are examined per line: access type, address, and access size. The access type is numeric: 0 for read, 1 for write, 2 for instruction fetch, 3 for miscellaneous, 4 for copy-back, and 5 for invalidate. The address is hexadecimal, beginning with an optional ‘‘0x’’ or ‘‘0X’’. Size is the size of the access in bytes. Fields are separated by whitespace (space or tab), and everything following the first two fields of a line is ignored.
   Example:
   ./dineroIV -l1-dsize 32768 -l1-dbsize 16 -l1-dassoc 4 -l1-dwalloc n -l1-dccc -informat D < testinput
   Where testinput is of the following format:
   1 0x1000A200 4
   1 0x1000A204 4
   1 0x1000A208 4
10. Use only read and write access types in your trace file.

11. The cache specification is: 4 way associativity, 8 banks, 32KB in total size, cache line sizes from 16B to 128B in powers of 2.

Grading Guidelines

For your information here are the grading guidelines

- 50pts: Provide a written description, pseudocode, and/or code snippets of memory coalescing mechanism and memory address map
- 50pts: One or more graphs that succinctly illustrate how cache line and memory map scheme affects cache hit rate for the 2 applications and their variations. Fully explain any irregularities you encounter and trends that support or contradict your expectations.

Submission Guidelines:

All submissions should be electronic (both program and problems). Submissions must time stamped by midnight on the due date. Submissions will be via Tsquare.

Note: No late assignments will be graded. Remember, you are expected to make a passing grade on the assignments to pass the course!