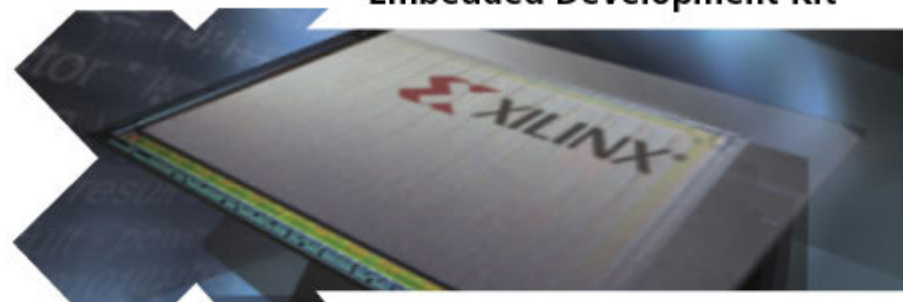




ML510 Dual MicroBlaze Processor Hardware Build

February 2009

Embedded Development Kit



PowerPC

Platform Studio™

MicroBlaze™

ISE



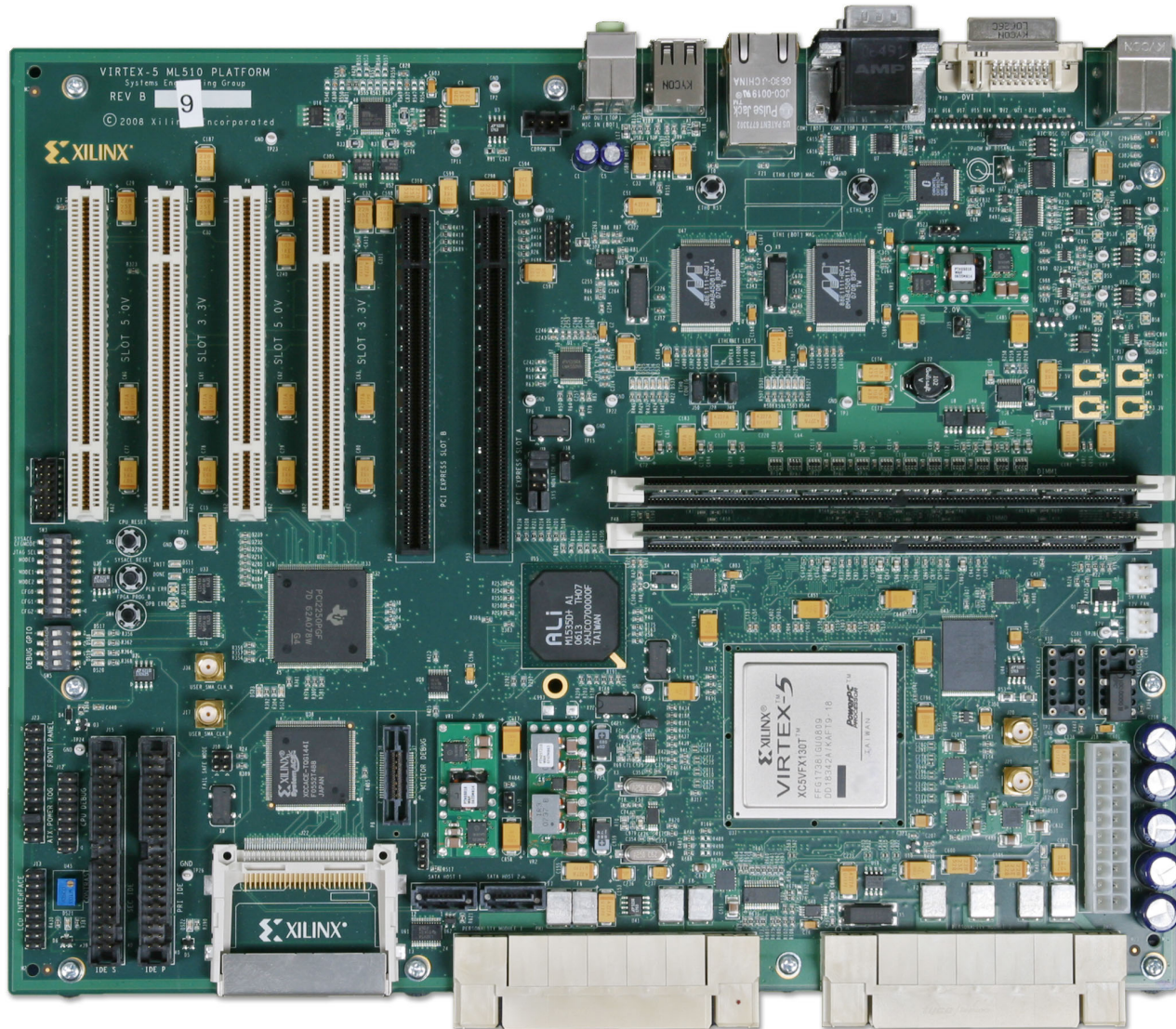
XILINX®

Overview

- Hardware Setup
- Software Requirements
- Download Bootloop Bitstream
- Download Application to MB_0
- Download Application to MB_1



Xilinx ML510 Board



Note: Presentation applies to the ML510

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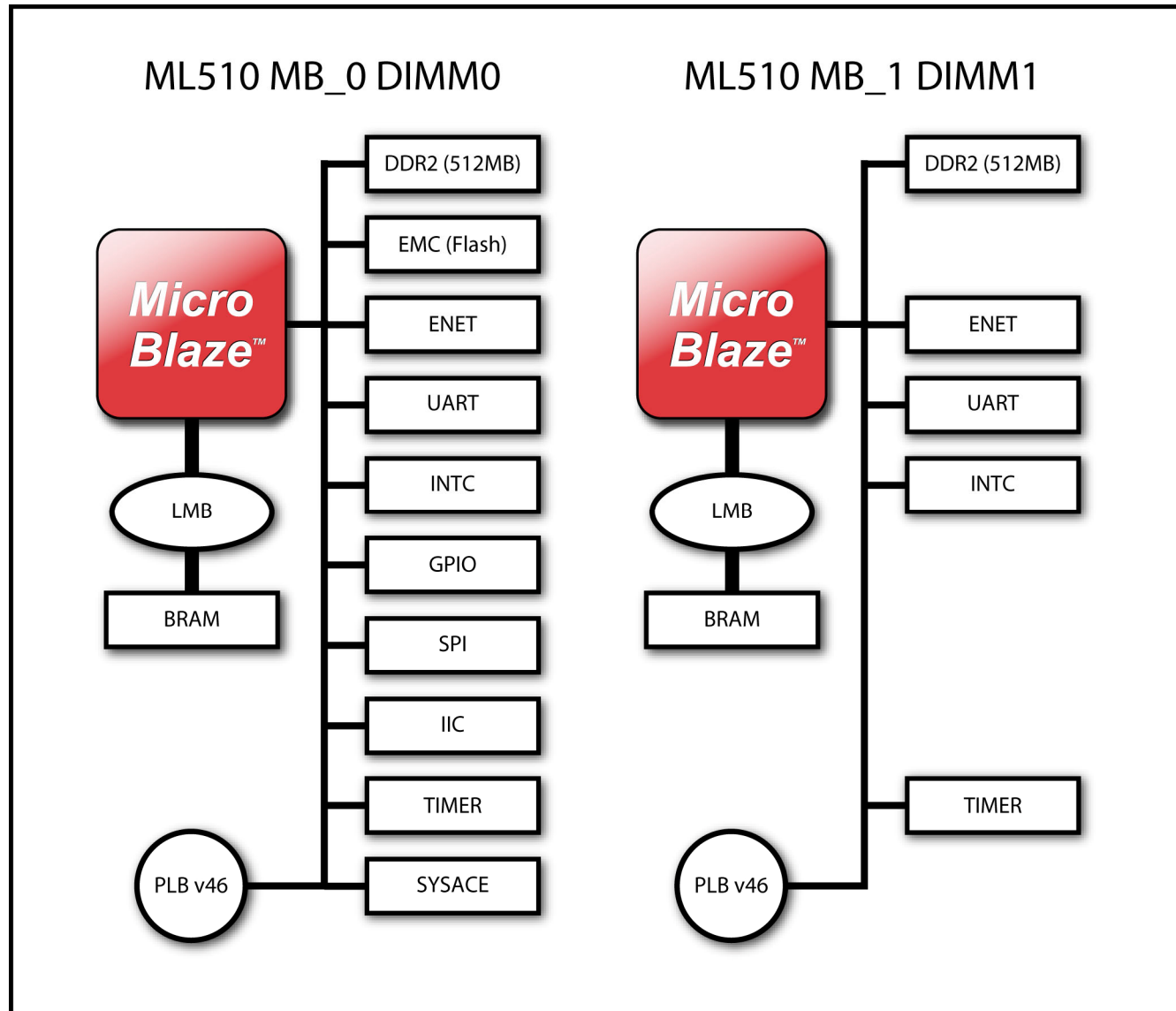
ML510 Dual MB Hardware

- MB_0:

- DDR2 Interface
- BRAM
- EMC (Flash)
- Networking
- UART
- Interrupt Controller
- GPIO
- SPI
- IIC
- Timer
- System ACE

- MB_1:

- DDR2 Interface
- BRAM
- Networking
- UART
- Interrupt Controller
- Timer



Additional Setup Details

- Refer to ml510_overview_setup.ppt for details on:
 - Software Requirements
 - ML510 Board Setup
 - **Equipment and Cables**
 - **Software**
 - **Network**
 - Terminal Programs
 - **This presentation requires the 9600-8-N-1 Baud terminal setup**

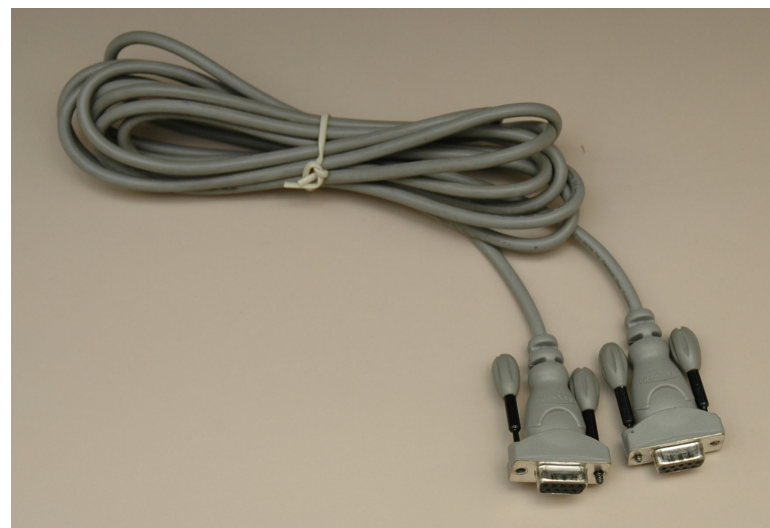


Hardware Setup

- Connect the Xilinx Platform Cable USB to the ML510 board



- Connect the RS232 null modem cable to the ML510 board
 - Connect to the COM1 and COM2 ports on the ML510 board



ISE Software Requirement

- Xilinx ISE 10.1i SP3 software



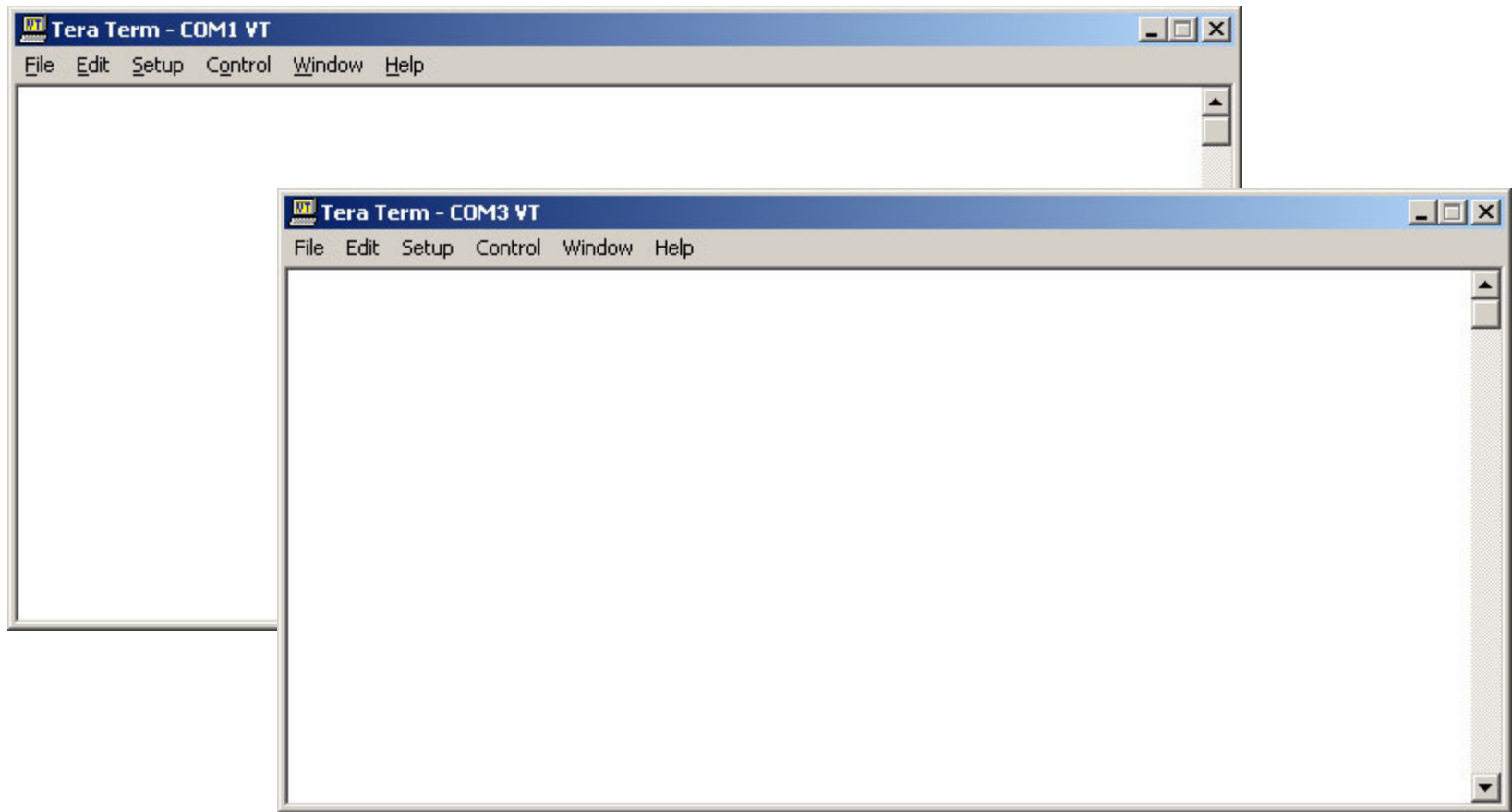
EDK Software Requirement

- Xilinx EDK 10.1i SP3 software



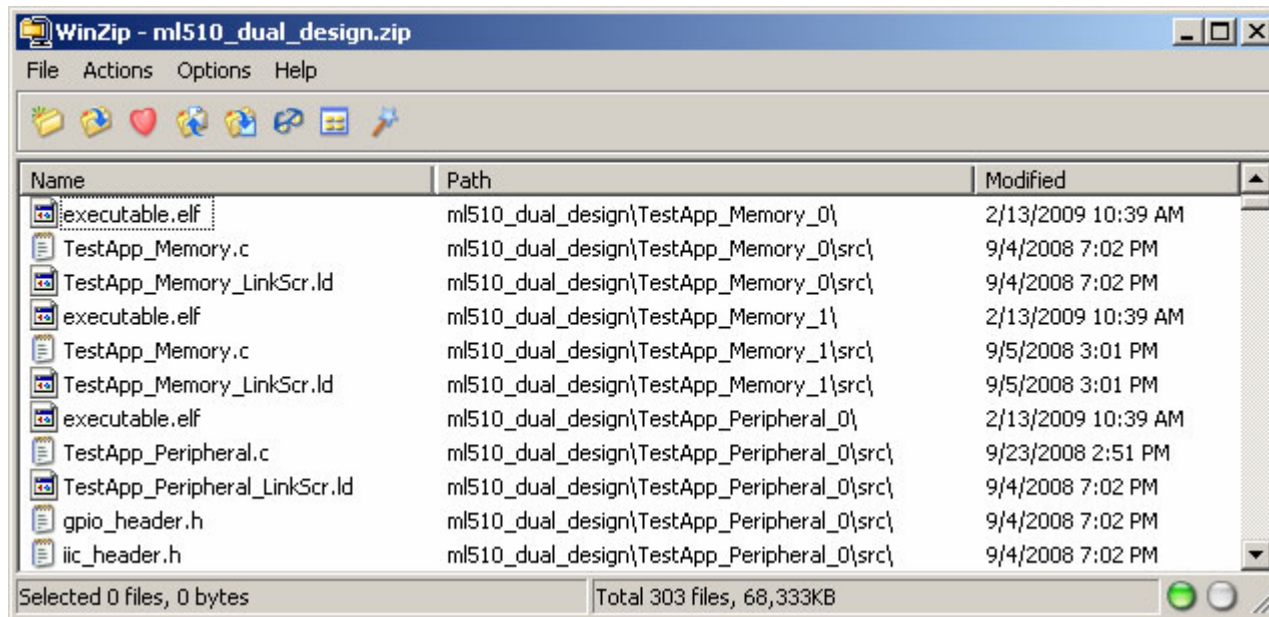
Software Setup

- Start a Terminal Program for each UART:



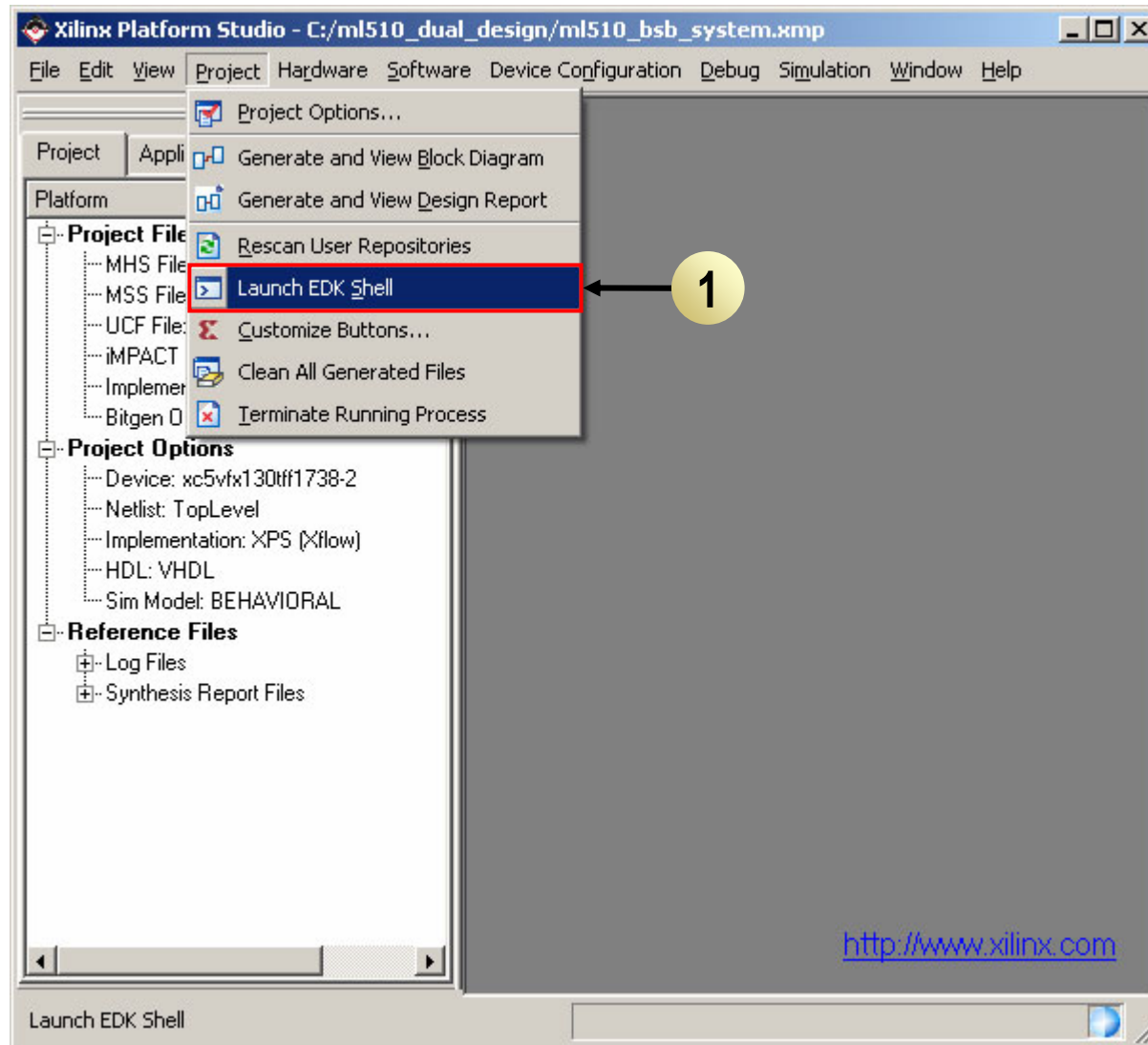
Extracting the Design

- Unzip the ml510_dual_design.zip file
 - This creates ISE and EDK project directories



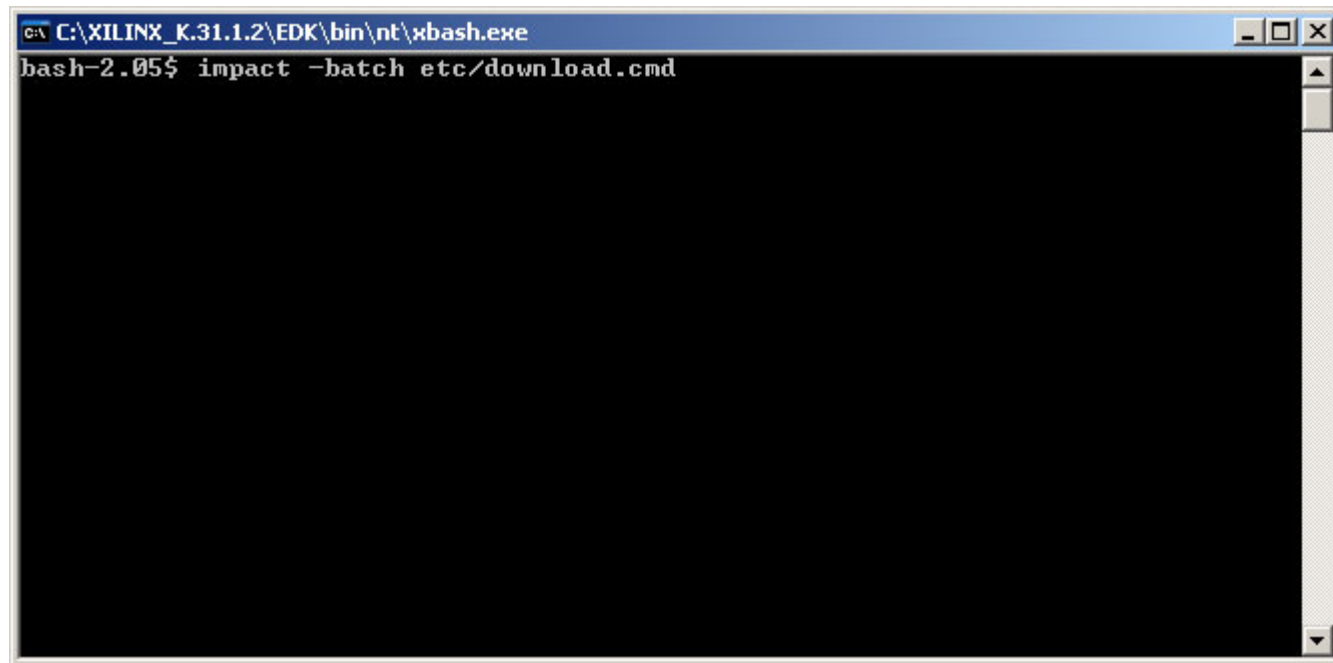
Run Xilinx Platform Studio

- Launch XPS project
<design path>\
ml510_bsb_system.xmp
 - Select **Project** →
**Launch EDK
Shell** (1)



Download Bitstream

- Download the bitstream:
impact -batch etc/download.cmd

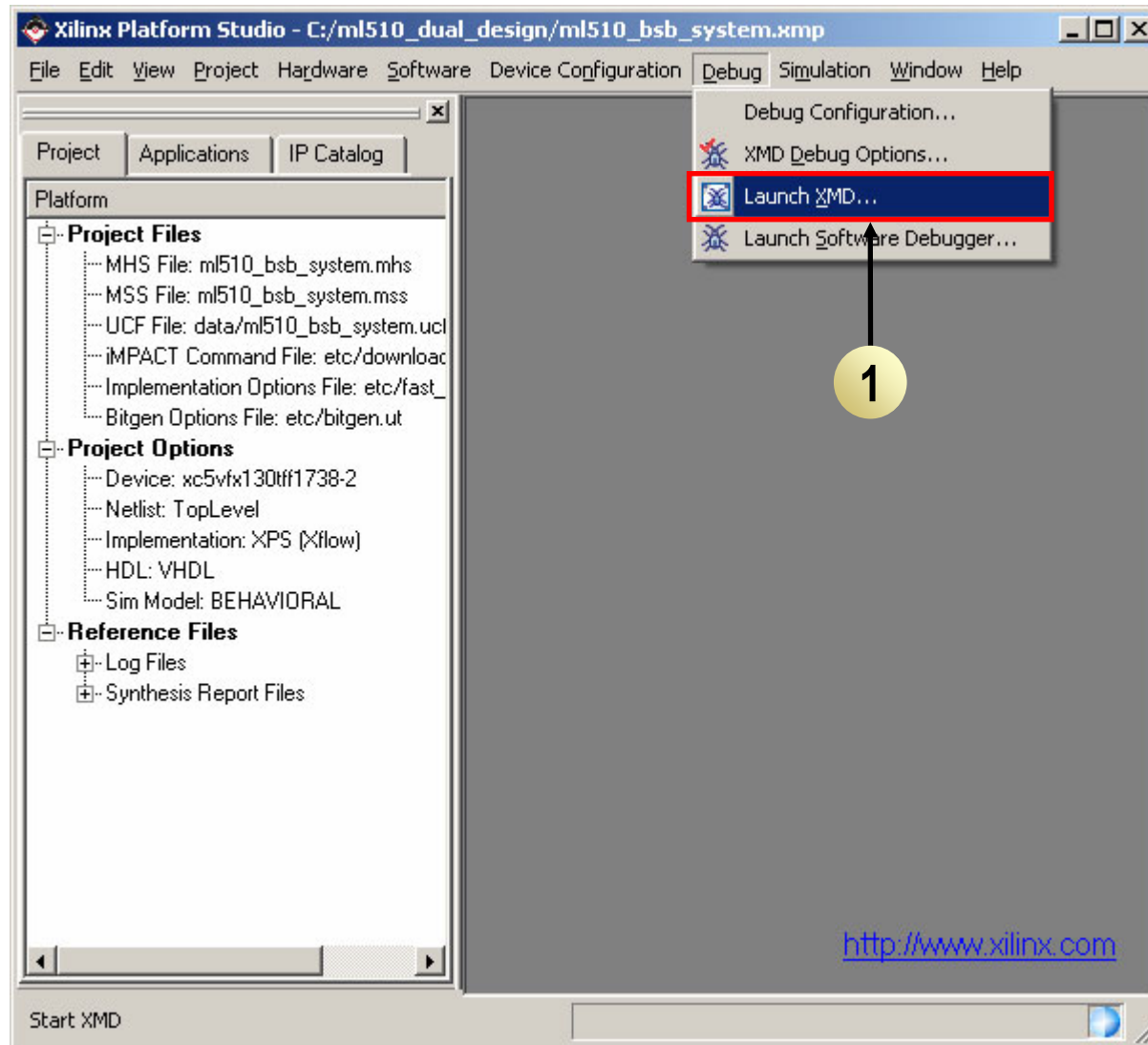
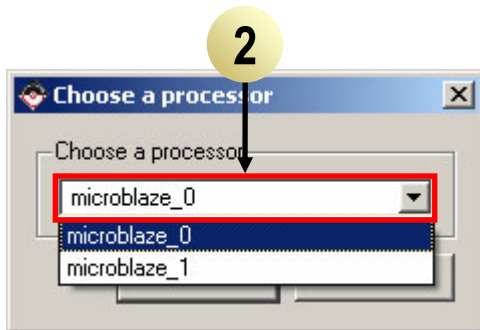


A screenshot of a Windows command prompt window. The title bar at the top reads "C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe". The command prompt shows the text "bash-2.05\$ impact -batch etc/download.cmd". The rest of the window is black, indicating that the command has been executed and the output is not visible.



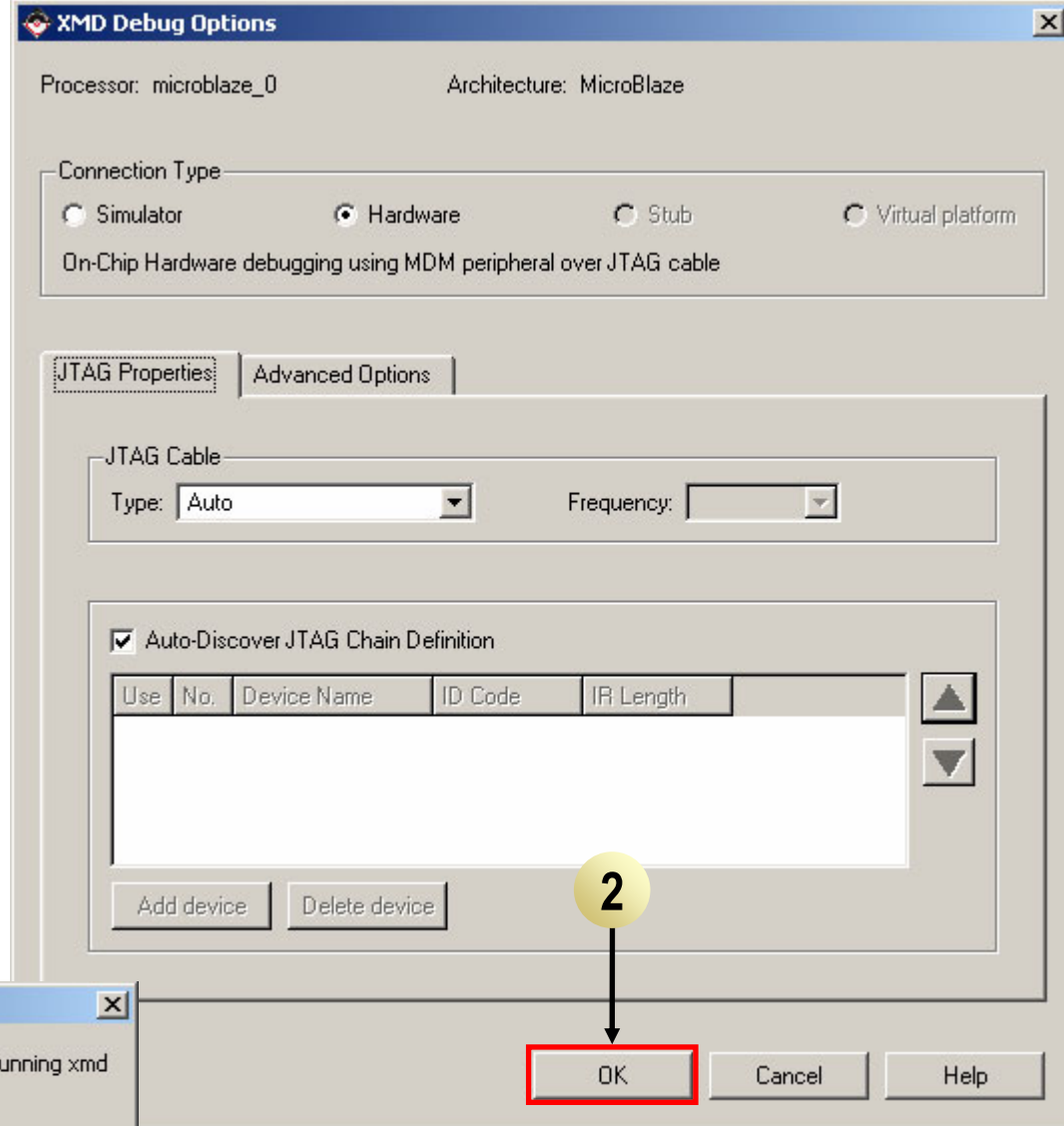
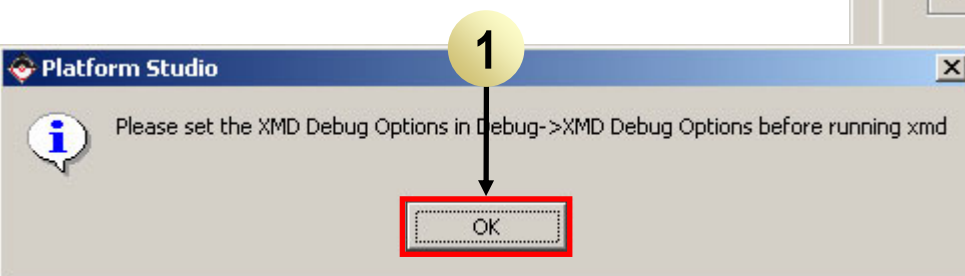
Loading Bootloop into BRAM

- A memory read can be executed to test if bootloop was successfully loaded
 - Select **Debug** → **Launch XMD** (1)
 - Select **microblaze_0** (2)



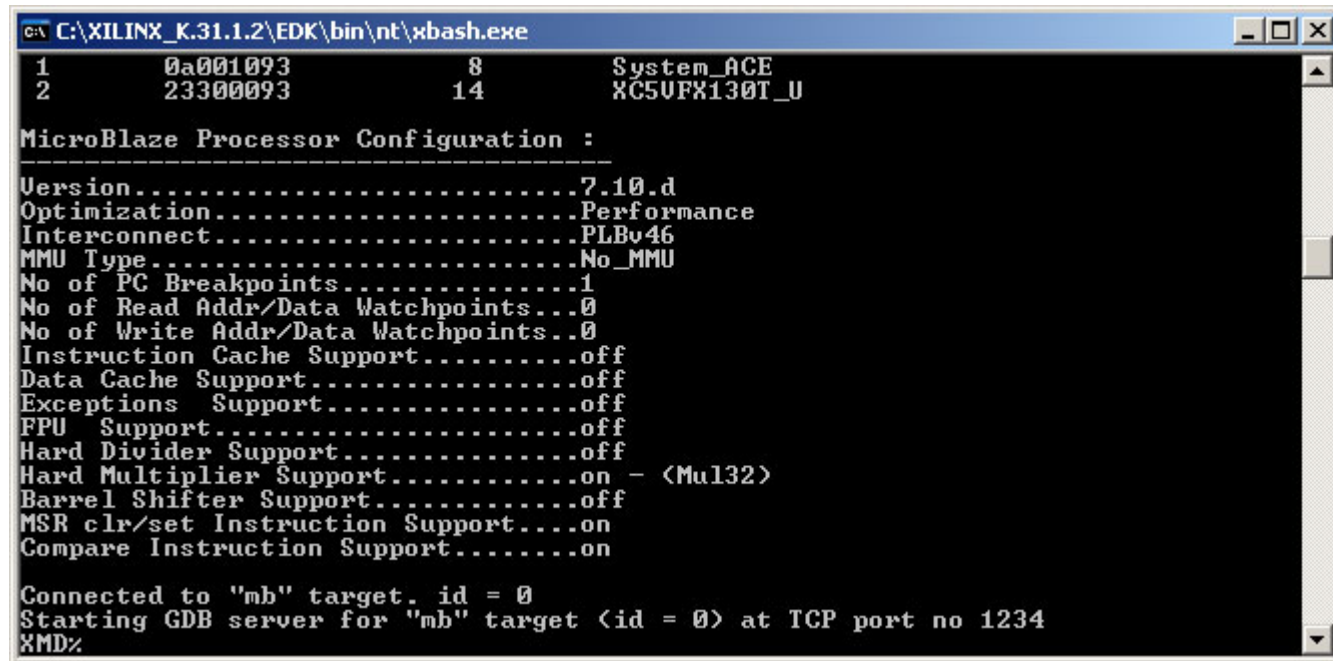
XMD Setup

- The first time XMD runs on a project, the options must be set
 - Click **OK** (1)
 - Click **OK** (2)



Loading Bootloop into BRAM

- XMD opens and connects to the processor, using the default options



```
C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
1      0a001093      8      System_ACE
2      23300093     14      XC5VFX130T_U

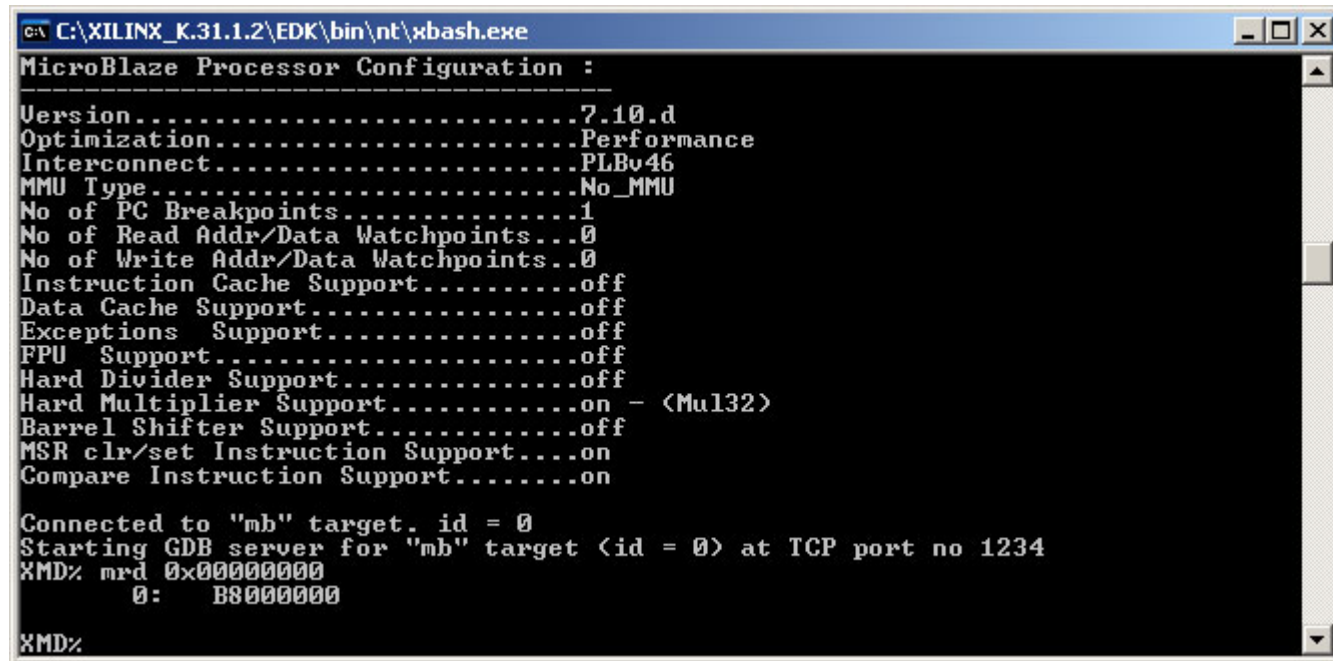
MicroBlaze Processor Configuration :
-----
Version.....7.10.d
Optimization.....Performance
Interconnect.....PLBv46
MMU Type.....No_MMU
No of PC Breakpoints.....1
No of Read Addr/Data Watchpoints...0
No of Write Addr/Data Watchpoints..0
Instruction Cache Support.....off
Data Cache Support.....off
Exceptions Support.....off
FPU Support.....off
Hard Divider Support.....off
Hard Multiplier Support.....on - (Mul32)
Barrel Shifter Support.....off
MSR clr/set Instruction Support....on
Compare Instruction Support.....on

Connected to "mb" target. id = 0
Starting GDB server for "mb" target (id = 0) at TCP port no 1234
XMD%
```



Loading Bootloop into BRAM

- To execute a memory read, type **mrd 0x00000000**
- This will read the memory address at the reset vector; the value should be **0xB8000000** as shown below



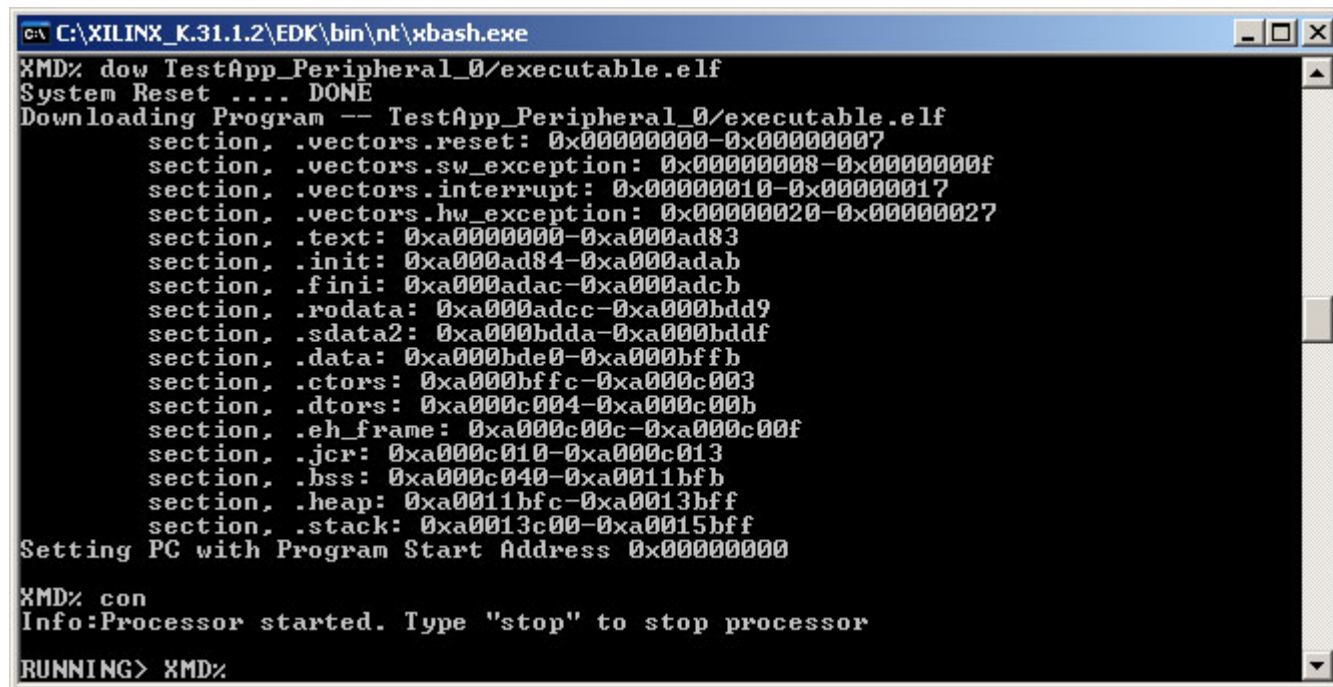
```
C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
MicroBlaze Processor Configuration :
-----
Version.....7.10.d
Optimization.....Performance
Interconnect.....PLBv46
MMU Type.....No_MMU
No of PC Breakpoints.....1
No of Read Addr/Data Watchpoints...0
No of Write Addr/Data Watchpoints..0
Instruction Cache Support.....off
Data Cache Support.....off
Exceptions Support.....off
FPU Support.....off
Hard Divider Support.....off
Hard Multiplier Support.....on - <Mul32>
Barrel Shifter Support.....off
MSR clr/set Instruction Support.....on
Compare Instruction Support.....on

Connected to "mb" target. id = 0
Starting GDB server for "mb" target <id = 0> at TCP port no 1234
XMD% mrd 0x00000000
      0:  B8000000
XMD%
```



TestApp_Peripheral

- Download and run the TestApp_Peripheral elf file:
dow TestApp_Peripheral_0/executable.elf
con

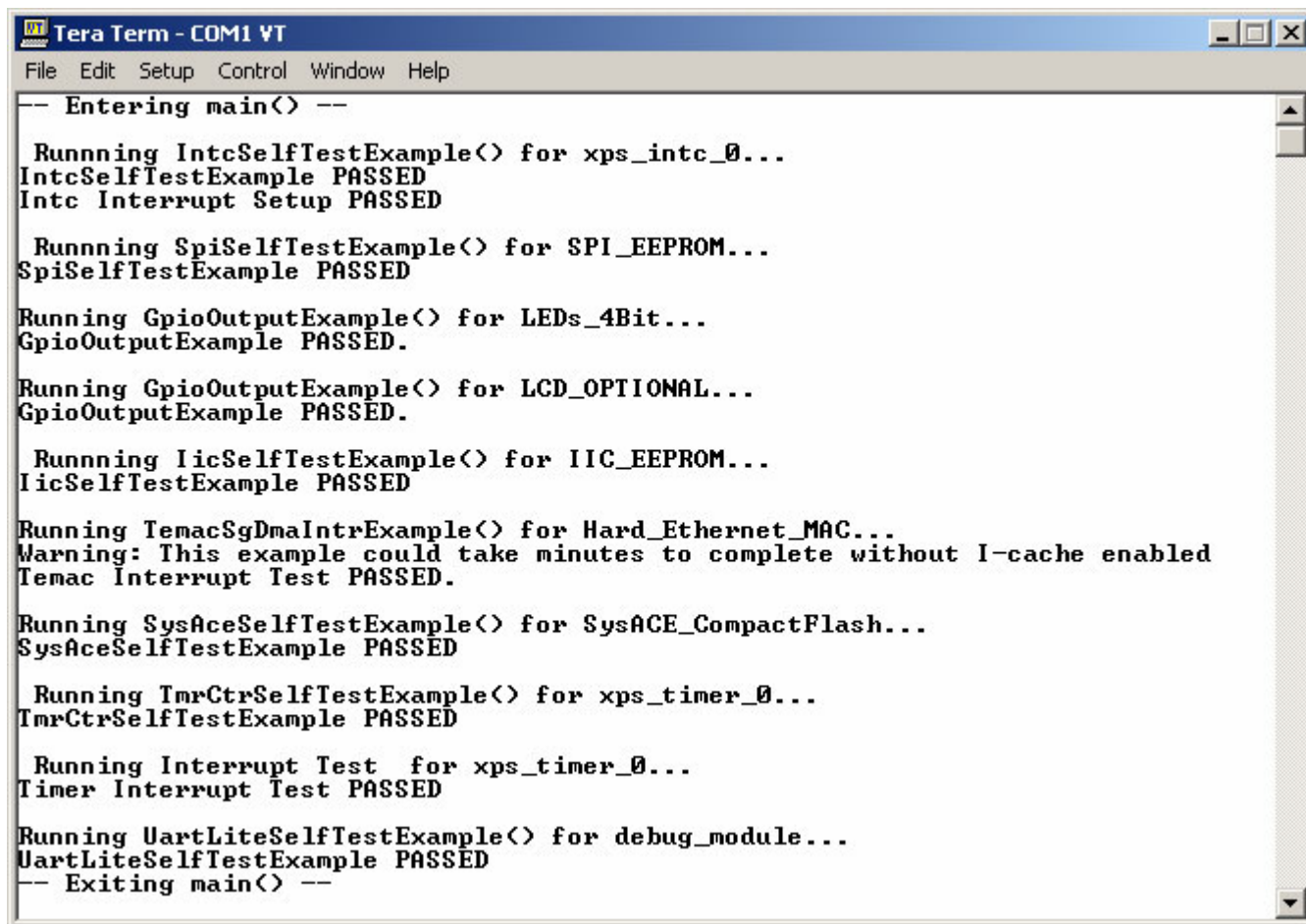


```
C:\XILINX_K31.1.2\EDK\bin\nt\xbash.exe
XMD% dow TestApp_Peripheral_0/executable.elf
System Reset .... DONE
Downloading Program -- TestApp_Peripheral_0/executable.elf
section, .vectors.reset: 0x00000000-0x00000007
section, .vectors.sw_exception: 0x00000008-0x0000000f
section, .vectors.interrupt: 0x00000010-0x00000017
section, .vectors.hw_exception: 0x00000020-0x00000027
section, .text: 0xa0000000-0xa000ad83
section, .init: 0xa000ad84-0xa000adab
section, .fini: 0xa000adac-0xa000adcb
section, .rodata: 0xa000adcc-0xa000bdd9
section, .sdata2: 0xa000bdda-0xa000bddf
section, .data: 0xa000bde0-0xa000bffb
section, .ctors: 0xa000bffc-0xa000c003
section, .dtors: 0xa000c004-0xa000c00b
section, .eh_frame: 0xa000c00c-0xa000c00f
section, .jcr: 0xa000c010-0xa000c013
section, .bss: 0xa000c040-0xa0011bfb
section, .heap: 0xa0011bfc-0xa0013bff
section, .stack: 0xa0013c00-0xa0015bff
Setting PC with Program Start Address 0x00000000
XMD% con
Info:Processor started. Type "stop" to stop processor
RUNNING> XMD%
```



Download the Bitstream

- View the output of a successful bitstream download in the terminal window



```
Tera Term - COM1 VT
File Edit Setup Control Window Help

-- Entering main() --

Running IntcSelfTestExample() for xps_intc_0...
IntcSelfTestExample PASSED
Intc Interrupt Setup PASSED

Running SpiSelfTestExample() for SPI_EEPROM...
SpiSelfTestExample PASSED

Running GpioOutputExample() for LEDs_4Bit...
GpioOutputExample PASSED.

Running GpioOutputExample() for LCD_OPTIONAL...
GpioOutputExample PASSED.

Running IicSelfTestExample() for IIC_EEPROM...
IicSelfTestExample PASSED

Running TemacSgDmaIntrExample() for Hard_Ethernet_MAC...
Warning: This example could take minutes to complete without I-cache enabled
Temac Interrupt Test PASSED.

Running SysAceSelfTestExample() for SysACE_CompactFlash...
SysAceSelfTestExample PASSED

Running TmrCtrSelfTestExample() for xps_timer_0...
TmrCtrSelfTestExample PASSED

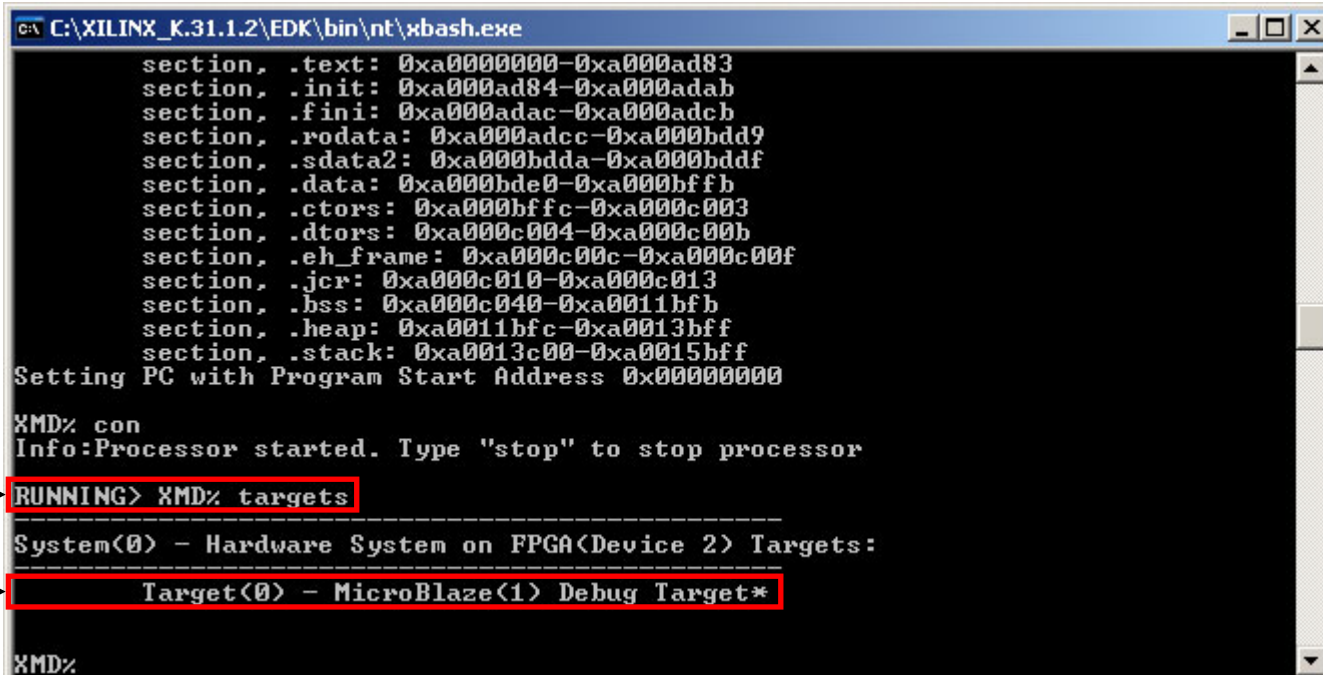
Running Interrupt Test for xps_timer_0...
Timer Interrupt Test PASSED

Running UartLiteSelfTestExample() for debug_module...
UartLiteSelfTestExample PASSED
-- Exiting main() --
```



Create 2nd Target in XMD

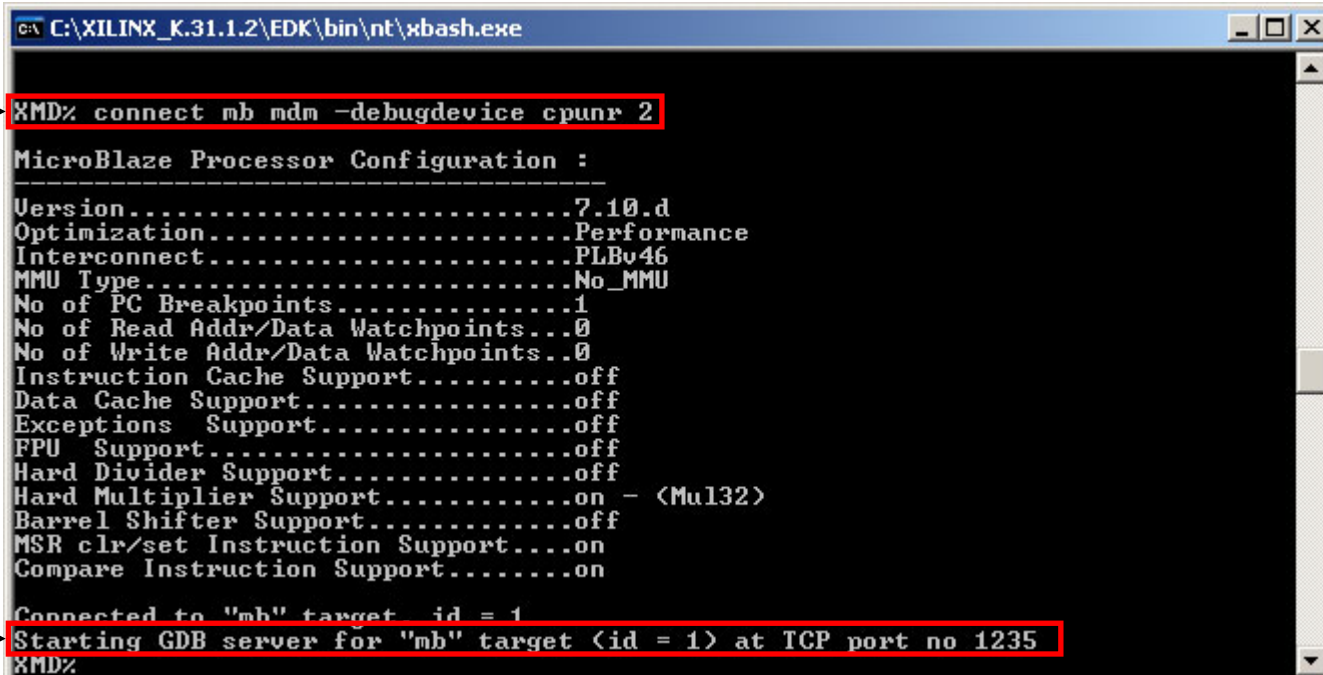
- Type **targets** (1) to view the current target, 0 (2)



```
C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
section, .text: 0xa0000000-0xa000ad83
section, .init: 0xa000ad84-0xa000adab
section, .fini: 0xa000adac-0xa000adcb
section, .rodata: 0xa000adcc-0xa000bdd9
section, .sdata2: 0xa000bdda-0xa000bddf
section, .data: 0xa000bde0-0xa000bfff
section, .ctors: 0xa000bffc-0xa000c003
section, .dtors: 0xa000c004-0xa000c00b
section, .eh_frame: 0xa000c00c-0xa000c00f
section, .jcr: 0xa000c010-0xa000c013
section, .bss: 0xa000c040-0xa00011bfb
section, .heap: 0xa00011bfc-0xa00013bff
section, .stack: 0xa00013c00-0xa00015bff
Setting PC with Program Start Address 0x00000000
XMD% con
Info:Processor started. Type "stop" to stop processor
1 -> RUNNING> XMD% targets
-----
System<0> - Hardware System on FPGA<Device 2> Targets:
2 -> Target<0> - MicroBlaze<1> Debug Target*
XMD%
```

Create 2nd Target in XMD

- Type **connect mb mdm -debugdevice cpunr 2** (1) to connect to the second cpu
- XMD connects to the 2nd processor
 - Note that this attaches through port 1235 (2)



The screenshot shows a command prompt window titled "C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe". The command `XMD% connect mb mdm -debugdevice cpunr 2` is entered and highlighted with a red box, with a yellow circle containing the number "1" pointing to it. Below the command, the "MicroBlaze Processor Configuration" is displayed, listing various hardware features and their status. At the bottom of the window, the message "Starting GDB server for 'mb' target (id = 1) at TCP port no 1235" is highlighted with a red box, with a yellow circle containing the number "2" pointing to it.

```
C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
XMD% connect mb mdm -debugdevice cpunr 2
MicroBlaze Processor Configuration :
-----
Version.....7.10.d
Optimization.....Performance
Interconnect.....PLBv46
MMU Type.....No_MMU
No of PC Breakpoints.....1
No of Read Addr/Data Watchpoints...0
No of Write Addr/Data Watchpoints..0
Instruction Cache Support.....off
Data Cache Support.....off
Exceptions Support.....off
FPU Support.....off
Hard Divider Support.....off
Hard Multiplier Support.....on - (Mul32)
Barrel Shifter Support.....off
MSR clr/set Instruction Support....on
Compare Instruction Support.....on

Connected to "mb" target id = 1
Starting GDB server for "mb" target (id = 1) at TCP port no 1235
XMD%
```



Verify Bootloop in BRAM

- Type **targets** again (1); target 1 is now selected (2)

```
C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
PowerPC440 Processor Configuration
-----
Version.....0x7ff21912
User ID.....0x00f00002
No of PC Breakpoints.....4
No of Addr/Data Watchpoints.....2
User Defined Address Map to access Special PowerPC Features using XMD:
  I-Cache <Data>.....0x70000000 - 0x70007fff
  I-Cache <TAG>.....0x70008000 - 0x7000ffff
  D-Cache <Data>.....0x78000000 - 0x78007fff
  D-Cache <TAG>.....0x78008000 - 0x7800ffff
  DCR.....0x78020000 - 0x78020fff
  TLB.....0x70020000 - 0x70023fff

Connected to "ppc" target. id = 1
Starting GDB server for "ppc" target (id = 1) at TCP port no 1235
XMD% targets

System(0) - Hardware System on FPGA(Device 2) Targets:
-----
  Target(0) - PowerPC440(1) Hardware Debug Target
  Target(1) - PowerPC440(2) Hardware Debug Target*

XMD%
```

Verify Bootloop in BRAM

- To execute a memory read, type **mrd 0x00000000**
- This will read the memory address at the reset vector; the value should be **0xB8000000** as shown below

```
C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
No of Read Addr/Data Watchpoints...0
No of Write Addr/Data Watchpoints..0
Instruction Cache Support.....off
Data Cache Support.....off
Exceptions Support.....off
FPU Support.....off
Hard Divider Support.....off
Hard Multiplier Support.....on - <Mul32>
Barrel Shifter Support.....off
MSR clr/set Instruction Support.....on
Compare Instruction Support.....on

Connected to "mb" target. id = 1
Starting GDB server for "mb" target <id = 1> at TCP port no 1235
XMD% targets
-----
System<0> - Hardware System on FPGA<Device 2> Targets:
-----
      Target<0> - MicroBlaze<1> Debug Target
      Target<1> - MicroBlaze<2> Debug Target*

XMD% mrd 0x00000000
      0:  B8000000
XMD%
```



Download ELF File

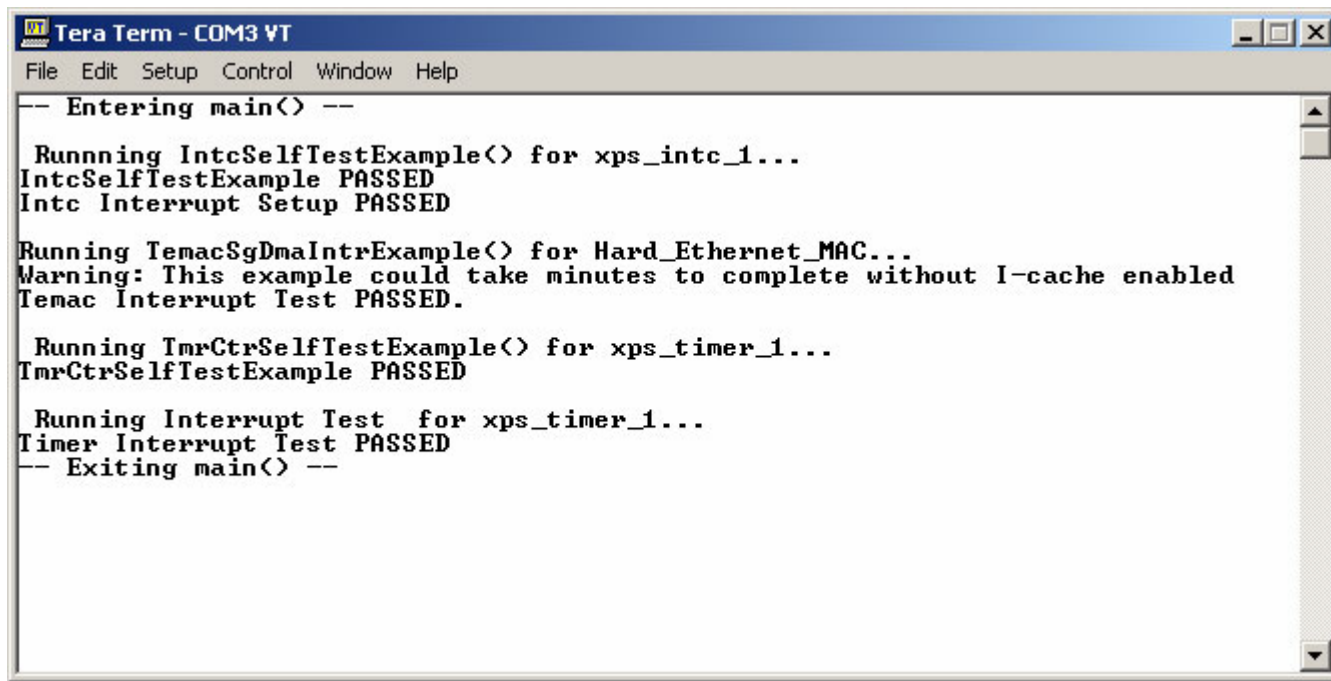
- Download the 2nd TestApp Peripheral ELF file from XMD
dow TestApp_Peripheral_1/executable.elf
con

```
C:\XILINX_K.31.1.2\EDK\bin\nt\xbash.exe
XMD% dow TestApp_Peripheral_1/executable.elf
System Reset .... DONE
Downloading Program -- TestApp_Peripheral_1/executable.elf
section, .vectors.reset: 0x00000000-0x00000007
section, .vectors.sw_exception: 0x00000008-0x0000000f
section, .vectors.interrupt: 0x00000010-0x00000017
section, .vectors.hw_exception: 0x00000020-0x00000027
section, .text: 0xa0000000-0xa000700f
section, .init: 0xa0007010-0xa0007033
section, .fini: 0xa0007034-0xa000704f
section, .rodata: 0xa0007050-0xa0007cfd
section, .sdata2: 0xa0007cfe-0xa0007cff
section, .data: 0xa0007d00-0xa0007e97
section, .ctors: 0xa0007e98-0xa0007e9f
section, .dtors: 0xa0007ea0-0xa0007ea7
section, .eh_frame: 0xa0007ea8-0xa0007eab
section, .jcr: 0xa0007eac-0xa0007eaf
section, .bss: 0xa0007ec0-0xa000d933
section, .heap: 0xa000d934-0xa000f937
section, .stack: 0xa000f938-0xa0011937
Setting PC with Program Start Address 0x00000000
XMD% con
Info:Processor started. Type "stop" to stop processor
RUNNING> XMD%
```



Download the Bitstream

- View the output of a successful bitstream download in the terminal window



```
Tera Term - COM3 VT
File Edit Setup Control Window Help

-- Entering main() --

Running IntcSelfTestExample() for xps_intc_1...
IntcSelfTestExample PASSED
Intc Interrupt Setup PASSED

Running TemacSgDmaIntrExample() for Hard_Ethernet_MAC...
Warning: This example could take minutes to complete without I-cache enabled
Temac Interrupt Test PASSED.

Running TmrCtrSelfTestExample() for xps_timer_1...
TmrCtrSelfTestExample PASSED

Running Interrupt Test for xps_timer_1...
Timer Interrupt Test PASSED
-- Exiting main() --
```



Documentation

- Virtex-5
 - Silicon Devices
http://www.xilinx.com/products/silicon_solutions
 - Virtex-5 Multi-Platform FPGA
http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5
 - Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms
http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
 - Virtex-5 FPGA DC and Switching Characteristics Data Sheet
http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf



Documentation

- Virtex-5
 - Virtex-5 FPGA User Guide
http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
 - Virtex-5 FPGA Configuration User Guide
http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
 - Virtex-5 System Monitor User Guide
http://www.xilinx.com/support/documentation/user_guides/ug192.pdf
 - Virtex-5 Packaging and Pinout Specification
http://www.xilinx.com/support/documentation/user_guides/ug195.pdf



Documentation

- Virtex-5 RocketIO
 - RocketIO GTP Transceivers
http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTP.htm
 - RocketIO GTX Transceivers
http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTX.htm
 - RocketIO GTP Transceiver User Guide – UG196
http://www.xilinx.com/support/documentation/user_guides/ug196.pdf
 - RocketIO GTX Transceiver User Guide – UG198
http://www.xilinx.com/support/documentation/user_guides/ug198.pdf



Documentation

- Design Resources

- ISE Development Tools and IP

- <http://www.xilinx.com/ise>

- Integrated Software Environment (ISE) Foundation Resources

- http://www.xilinx.com/ise/logic_design_prod/foundation.htm

- ISE Manuals

- http://www.xilinx.com/support/software_manuals.htm

- ISE Development System Reference Guide

- <http://toolbox.xilinx.com/docsan/xilinx10/books/docs/dev/dev.pdf>

- ISE Development System Libraries Guide

- http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5_hdl/virtex5_hdl.pdf



Documentation

- Additional Design Resources
 - Customer Support
<http://www.xilinx.com/support>
 - Xilinx Design Services:
<http://www.xilinx.com/xds>
 - Titanium Dedicated Engineering:
<http://www.xilinx.com/titanium>
 - Education Services:
<http://www.xilinx.com/education>
 - Xilinx On Board (Board and kit locator):
<http://www.xilinx.com/xob>



Documentation

- Platform Studio
 - Embedded Development Kit (EDK) Resources
<http://www.xilinx.com/edk>
 - Embedded System Tools Reference Manual
http://www.xilinx.com/support/documentation/sw_manuals/edk10_est_rm.pdf
 - EDK Concepts, Tools, and Techniques
http://www.xilinx.com/support/documentation/sw_manuals/edk_ctt.pdf



Documentation

- PowerPC 440
 - PowerPC 440 Processor
<http://www.xilinx.com/powerpc>
 - Embedded Processor Block in Virtex-5 FPGAs Reference Guide – UG200
http://www.xilinx.com/support/documentation/user_guides/ug200.pdf
 - PPC440 Virtex-5 Wrapper – DS621
http://www.xilinx.com/support/documentation/ip_documentation/ppc440_virtex5.pdf
 - DDR2 Memory Controller for PowerPC 440 Processors – DS567
http://www.xilinx.com/support/documentation/data_sheets/ds567.pdf



Documentation

- MicroBlaze
 - MicroBlaze Processor
<http://www.xilinx.com/microblaze>
 - MicroBlaze Processor Reference Guide – UG081
http://www.xilinx.com/support/documentation/sw_manuals/mb_ref_guide.pdf



Documentation

- Memory Solutions

- Demos on Demand – Memory Interface Solutions with Xilinx FPGAs

http://www.demosondemand.com/clients/xilinx/001/page_new2/index.asp#35

- Xilinx Memory Corner

http://www.xilinx.com/products/design_resources/mem_corner

- Additional Memory Resources

<http://www.xilinx.com/support/software/memory/protected/index.htm>

- Xilinx Memory Interface Generator (MIG) 2.2 User Guide

http://www.xilinx.com/support/documentation/ip_documentation/ug086.pdf

- Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator

http://www.xilinx.com/support/documentation/white_papers/wp260.pdf



Documentation

- ChipScope Pro
 - ChipScope Pro 10.1i Serial IO Toolkit User Manual
http://www.xilinx.com/ise/verification/chipscope_pro_siotk_10_1_ug213.pdf
 - ChipScope Pro 10.1i ChipScope Pro Software and Cores User Guide
http://www.xilinx.com/ise/verification/chipscope_pro_sw_cores_10_1_ug029.pdf



Documentation

- Ethernet
 - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet
http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_ds550.pdf
 - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide
http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_gsg340.pdf
 - Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide
http://www.xilinx.com/support/documentation/user_guides/ug194.pdf
 - LightWeight IP (lwIP) Application Examples – XAPP1026
http://www.xilinx.com/support/documentation/application_notes/xapp1026.pdf



Documentation

- PLB v4.6 IP
 - Processor Local Bus (PLB) v4.6 Data Sheet – DS531
http://www.xilinx.com/support/documentation/ip_documentation/plb_v46.pdf
 - Multi-Port Memory Controller (MPMC) – DS643
http://www.xilinx.com/support/documentation/ip_documentation/mpmc.pdf
 - XPS Multi-Channel External Memory Controller (XPS MCH EMC) – DS575
http://www.xilinx.com/support/documentation/ip_documentation/xps_mch_emc.pdf
 - XPS LocalLink TEMAC – DS537
http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_temac.pdf
 - XPS LocalLink FIFO – DS568
http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_fifo.pdf



Documentation

- PLB v4.6 IP
 - XPS IIC Bus Interface – DS606
http://www.xilinx.com/support/documentation/ip_documentation/xps_iic.pdf
 - XPS SYSACE (System ACE) Interface Controller – DS583
http://www.xilinx.com/support/documentation/ip_documentation/xps_sysace.pdf
 - XPS Timer/Counter – DS573
http://www.xilinx.com/support/documentation/ip_documentation/xps_timer.pdf
 - XPS Interrupt Controller – DS572
http://www.xilinx.com/support/documentation/ip_documentation/xps_intc.pdf
 - Using and Creating Interrupt-Based Systems Application Note
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