MiloSAR Documentation

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Chapter 1

Introduction

Chapter 2

FPGA

2.1 Registers

2.1.1 Configuration

Table 2.1: General configuration register.

			В	3							В	32			
31	31 30 29 28 27 20 25 2								22	21	20	19	18	17	16
		Res	serve	d [31	:24]					Res	serve	d [23:	:16]		

			В	31							В	0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			•		De	cima	tion	Facto	or [15	:0]	•				

2.1.2 Channel X Status

Table 2.2: Channel X status register.

			В	3							В	32			
31	31 30 29 28 27 26 25 24								22	21	20	19	18	17	16
					Cha	annel	ХР	ointe	r [31	:16]		•			

			В	1							В	80			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Channel X Pointer [15:0]														

Table 2.3: Synthesizer reference signal phase increment register.

			В	3							В	2			
31	31 30 29 28 27 26 25 2								22	21	20	19	18	17	16
					Pł	nase]	Incre	ment	[31:1	[6]					

			В	1							В	0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					Р	hase	Incre	ment	[15:	0]					

Table 2.4: GPIO register.

			В	3							В	2			
31	31 30 29 28 27 26 25 2								22	21	20	19	18	17	16
			•		(Clock	Divi	isor [31:16]					

			В	31							В	0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Cle	ock I	Diviso	or [15	:9]		E			G	PIO	N [7:0	0]		

2.1.3 Synthesizer Reference Signal

2.1.4 GPIO

2.1.5 Cancellation

Table 2.5: Cancellation signal phase increment register.

			В	3							В	32			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
					Pł	nase l	Incre	ment	[31:1	[6]		•			

			В	31							В	80			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					Р	hase	Incre	ement	[15:	0]					