MiloSAR Documentation

Version 0.1

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2.1 μWire Interface

The LMX2492EVM is packaged with a USBtoMANY converter, enabling users to program the evaluation module through its μWire connector using TI's CodeLoader. This process is however tedious, especially when programming two synthesizers with different waveforms. The LMX2492 datasheet provides the timing requirements and clocking structure for programming the synthesizer through its μWire connector pins. GPIO pins on the Red Pitaya were used to program both synthesizers efficiently. Figure 2.1 illustrates the connection between the Red Pitaya and two LMX2492 evaluation boards.

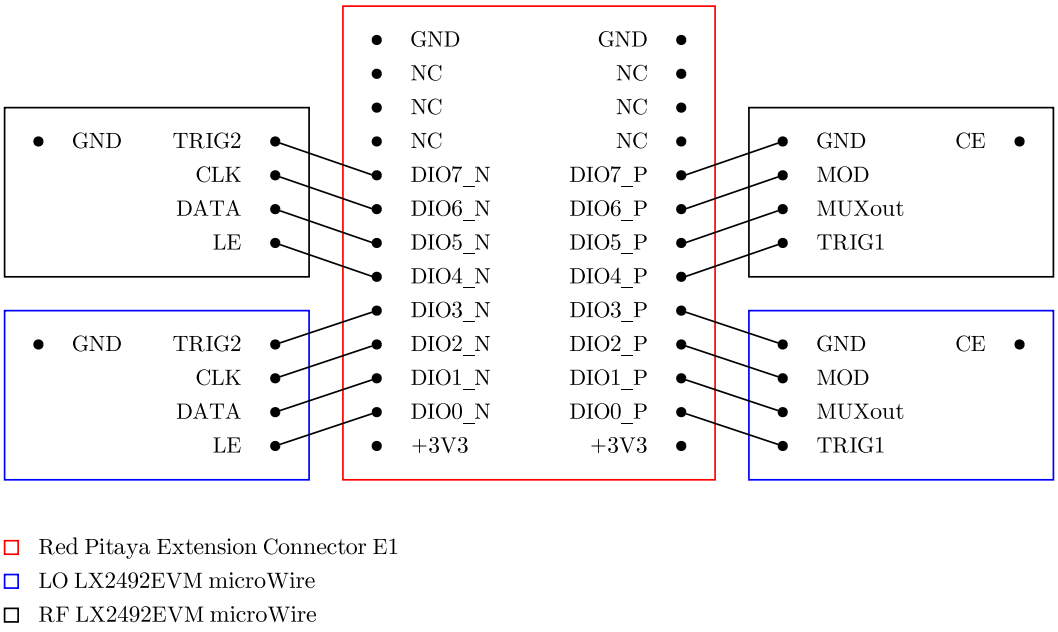

Figure 2.1: Wiring diagram for connection between Red Pitaya and the LMX2492.

Chapter 3

FPGA

3.1 Registers

3.1.1 Configuration

The configuration register is currently only used to set the decimation factor for reducing sampling rate. Sixteen bits are reserved for later use.

Table 3.1: General configuration register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved [31:24]								Reserved [23:16]							

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Decimation Factor [15:0]															

3.1.2 Channel X Status

Both recording channels within the FPGA require a status register to provide the CPU with the location of the RAM writer's current pointer location.

Table 3.2: Channel X status register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Channel X Pointer [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel X Pointer [15:0]															

3.1.3 Synthesizer Reference Signal

Provides the FPGA with the DDS phase increment used to generate the 50 MHz phase reference signal.

Table 3.3: Synthesizer reference signal phase increment register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Phase Increment [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Phase Increment [15:0]															

3.1.4 GPIO

Table 3.4: GPIO register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Clock Divisor [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Clock Divisor [15:9]							E	GPION [7:0]							

3.1.5 Cancellation

Table 3.5: Cancellation signal phase increment register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Phase Increment [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Phase Increment [15:0]															