MiloSAR Documentation

Version 0.1

Darryn Jordan

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2.1 μWire Interface

The LMX2492EVM is packaged with a USBtoMANY converter, enabling users to program the evaluation module through its μWire connector using TI's CodeLoader. This process is however tedious, especially when programming two synthesizers with different waveforms. The LMX2492 datasheet provides the timing requirements and clocking structure for programming the synthesizer through its μWire connector pins. GPIO pins on the Red Pitaya were used to program both synthesizers efficiently. Figure 2.1 illustrates the connection between the Red Pitaya and two LMX2492 evaluation boards.

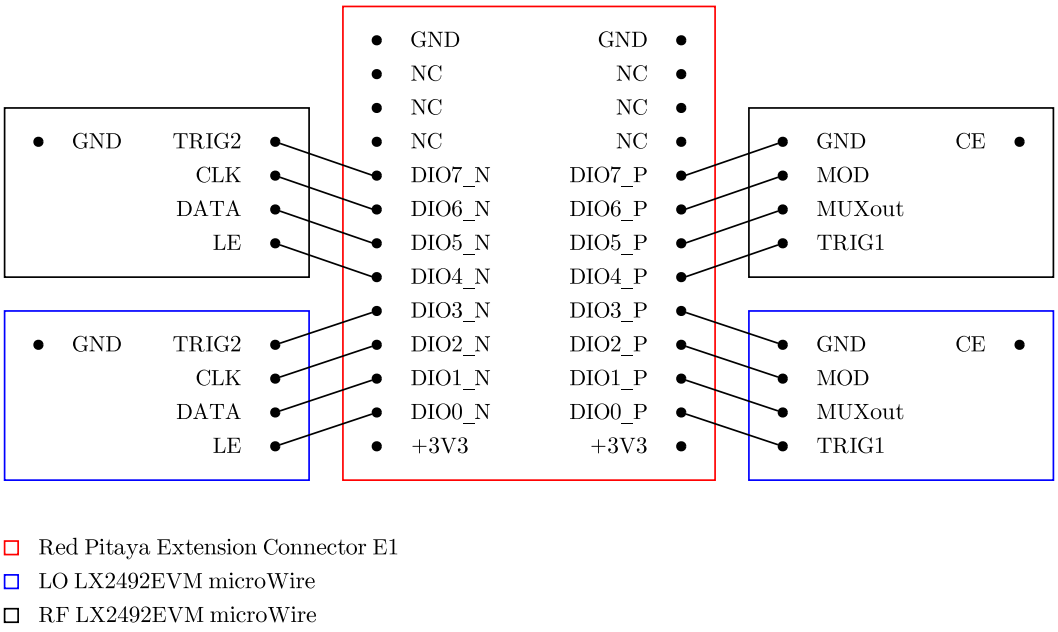

Figure 2.1: Wiring diagram for connection between Red Pitaya and the LMX2492.

Chapter 3

FPGA

3.1 Registers

3.1.1 Configuration

The configuration register is currently only used to set the decimation factor for reducing sampling rate. Sixteen bits are reserved for later use.

Table 3.1: General configuration register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved [31:24]								Reserved [23:16]							

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Decimation Factor [15:0]															

3.1.2 Channel X Status

Both recording channels within the FPGA require a status register to provide the CPU with the location of the RAM writer's current pointer location.

Table 3.2: Channel X status register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Channel X Pointer [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel X Pointer [15:0]															

3.1.3 Synthesizer Reference Signal

Provides the FPGA with the DDS phase increment used to generate the 50 MHz phase reference signal.

Table 3.3: Synthesizer reference signal phase increment register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Phase Increment [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Phase Increment [15:0]															

3.1.4 GPIO

The GPIO register is currently haphazard and contains the clock divisor value, which is used to set the PRF. Furthermore, an enable flag, bit 8, is used to enable the receive chain. It is suggested that both of these settings be moved the the configuration register once the decimation factor is fixed.

Table 3.4: GPIO register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Clock Divisor [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Clock Divisor [15:9]							E	GPION [7:0]							

3.1.5 Cancellation

Table 3.5: Cancellation signal phase increment register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Phase Increment [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Phase Increment [15:0]															

3.2 Digital Receiver Design

Design of the digital receiver begins with the selection of a suitable analogue bandpass filter. The SBP-10.7+ bandpass filter (BPF), procured from Mini-Circuits, features a 3 dB bandwidth of 3.8 MHz and lower-side cut-off frequency, $f_{3\,\mathrm{dB}}$, of 8.5 dB as illustrated in Figure 3.1. The SBP-10.7+ serves a dual role in suppressing feed-through and implementing sensitivity frequency-control.

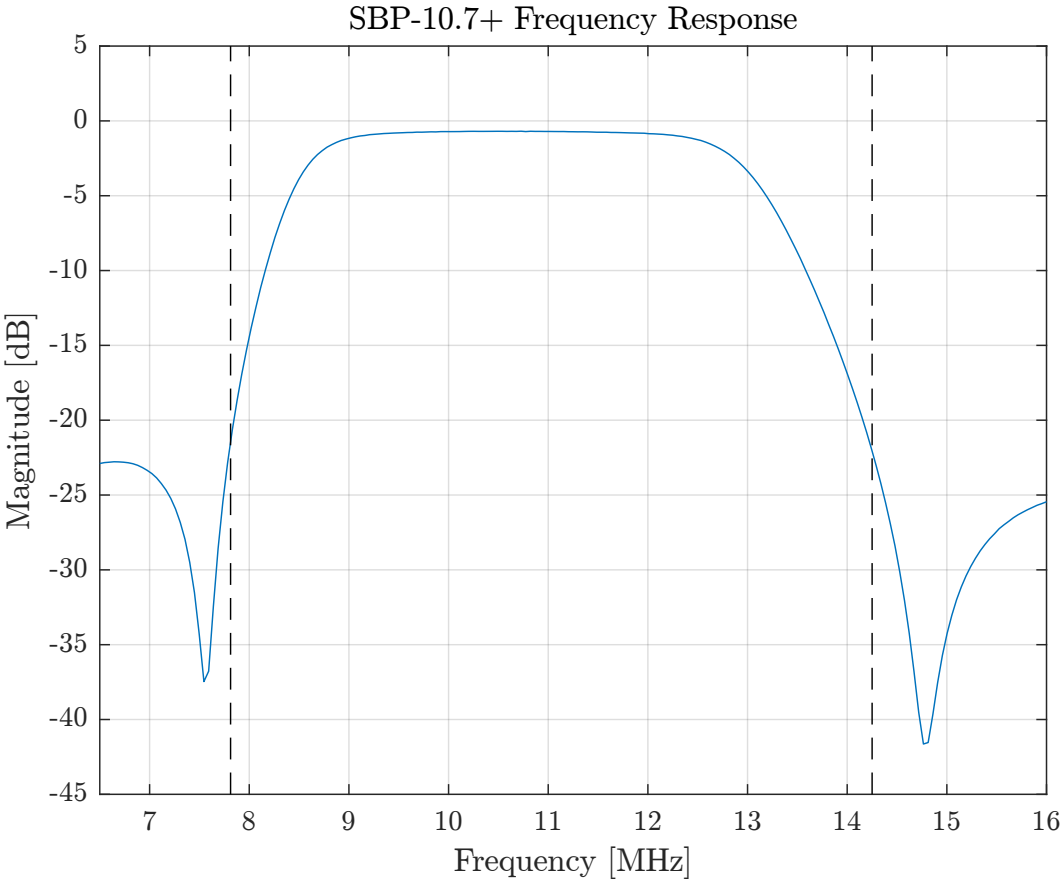

Figure 3.1: Frequency response of the SBP-10.7+ BPF with dashed lines indicating the Nyquist band of interest .

Following the SBP-10.7+, the beat spectrum is oversampled at a rate of 125 MHz using the Red Pitaya. This results in a spreading of quantization noise over the full sampled bandwidth (62.5 MHz). With appropriate filtering, quantization noise is greatly reduced. An additional benefit of oversampling is the ability to perform decimation through averaging in order to increase the effective number of bits (ENOB). Equation 3.1 reveals that an additional 1.5 bits are gained through decimation by a factor of 8.

$$n = \log_4(DF) \tag{3.1}$$

The SBP-10.7+ BPF is ideally positioned to make use of the second Nyquist zone

when using a decimation factor (DF) of 8. All signals of interest must therefore be contained within the $f_s/2$ to f_s band, or 7.8125 MHz to 15.625 MHz respectively, illustrated by the dashed lines in Figure 3.1. Components out of the Nyquist band of interest are therefore attenuated by more than 20 dB.

Having oversampled the beat spectrum at IF, the first step in the digital receive chain is pass the signal through the bandpass FIR decimation filter illustrated in Figure 3.2.

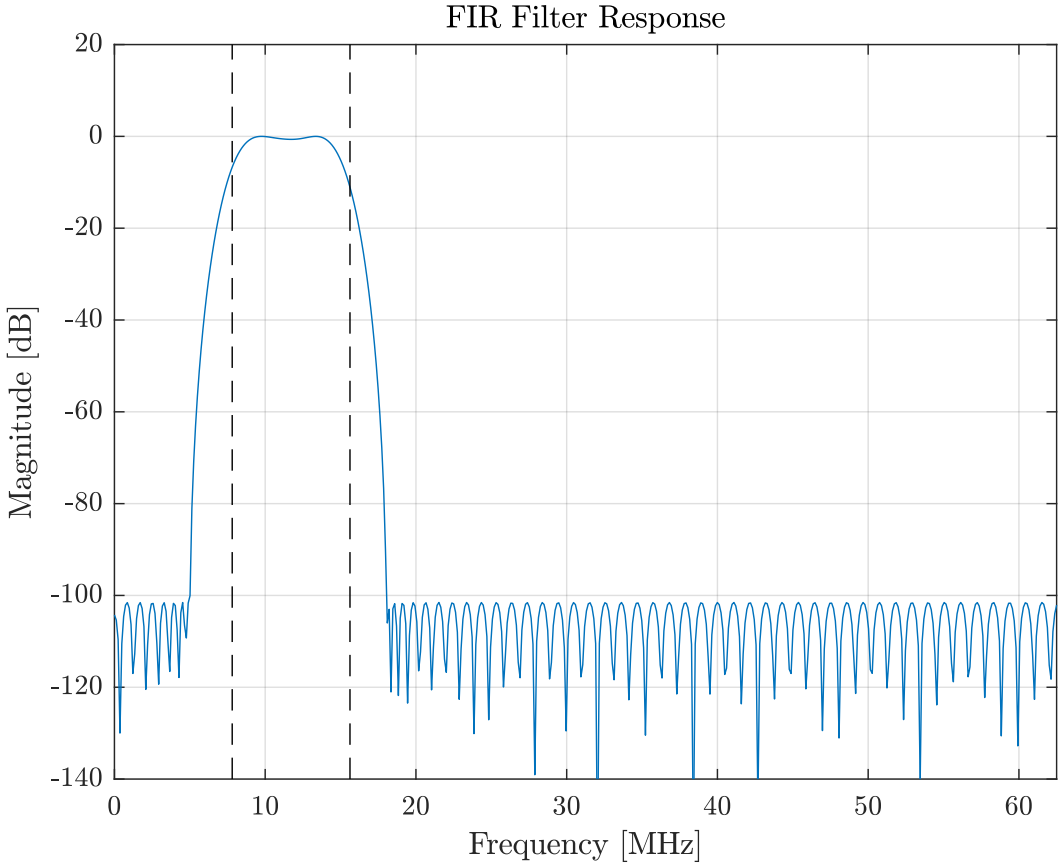

Figure 3.2: Frequency response of the FIR filter within the Red Pitaya.

Over 100 dB of suppression is provided by this 115-tap FIR filter. In addition to this, the filter is responsible for implementing decimation through averaging. It is important to note that the SBP-10.7+ analogue filter provides

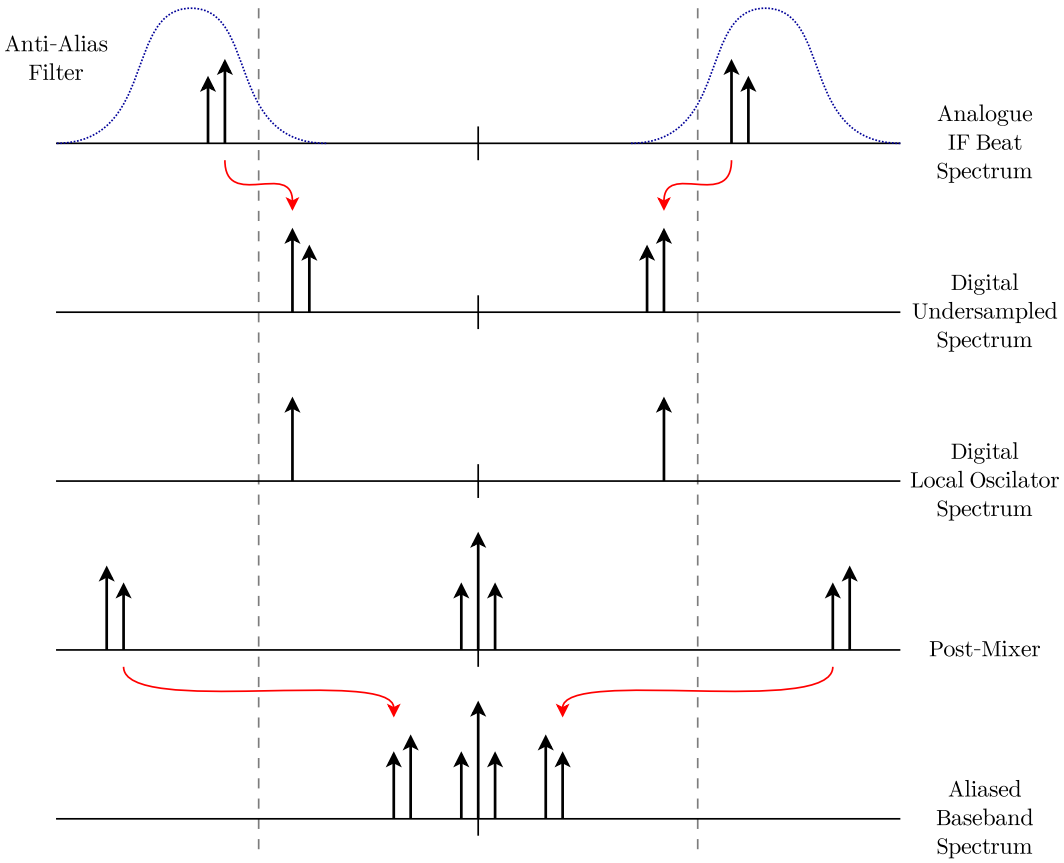

Figure 3.3: Down-conversion with aliasing owing to low sample rate.

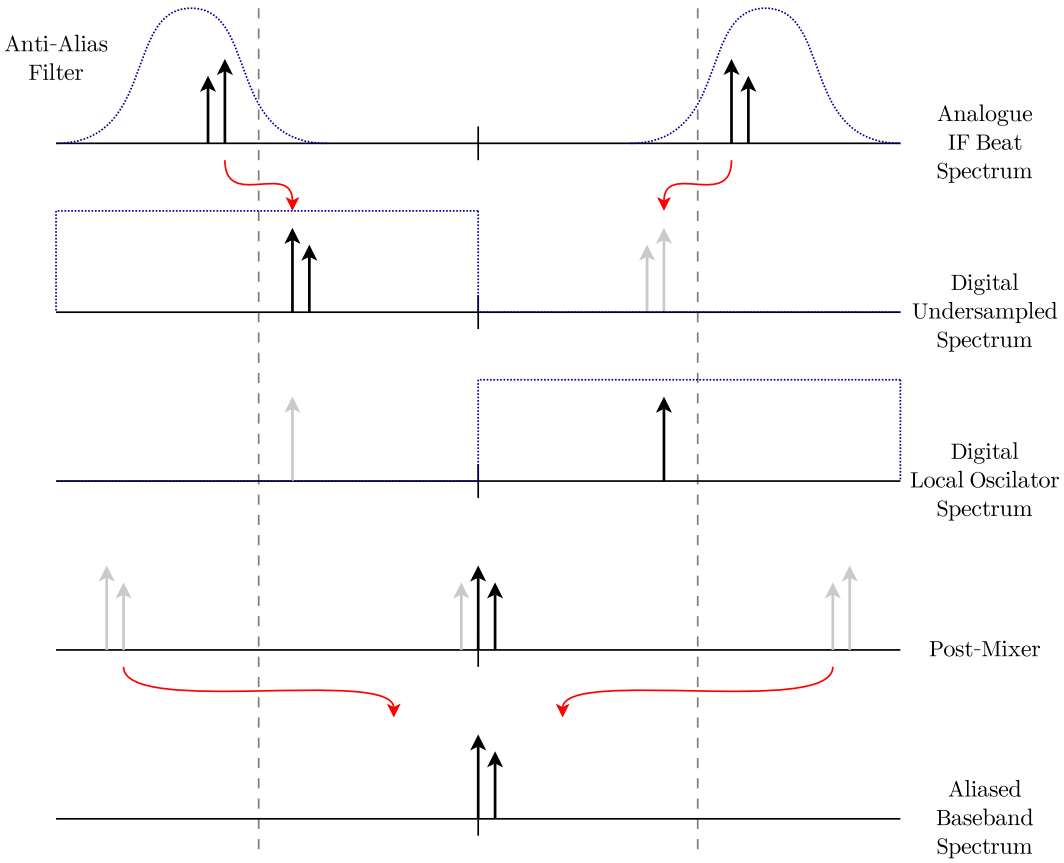

Figure 3.4: Down-conversion without aliasing.