MiloSAR Documentation

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Chapter 1

Introduction

Chapter 2

FPGA

2.1 Registers

2.1.1 Configuration

Table 2.1: General configuration register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved [31:24]								Reserved [23:16]							

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Decimation Factor [15:0]															

2.1.2 Channel X Status

Table 2.2: Channel X status register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Channel X Pointer [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel X Pointer [15:0]															

Table 2.3: Synthesizer reference signal phase increment register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Phase Increment [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Phase Increment [15:0]															

Table 2.4: GPIO register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Clock Divisor [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Clock Divisor [15:9]							E	GPION [7:0]							

2.1.3 Synthesizer Reference Signal

2.1.4 GPIO

2.1.5 Cancellation

Table 2.5: Cancellation signal phase increment register.

B3								B2							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Phase Increment [31:16]															

B1								B0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Phase Increment [15:0]															