Rana Taher 900221430

Mon, Oct 21, 1:00pm:

- discussed the project details with Yasmina.

Thursday, Oct 24, 3:30pm:

- discussed further details about the project with Yasmina.

Thursday, Oct 24, 6:00pm:

- Implemented the shifter module needed by the ALU.

Sun, Oct 27, 2:00 pm - 9:30:

- Added the ALU and Immgen modules (with Yasmina)
- Created the Branch control unit (with Yasmina)
- Modified the ALUcu and Control Unit (with Yasmina)
- Created the write and pc control (with Yasmina)
- Modifying the data memory to make it byte addressable (with Yasmina)
- Modifying the RISC-V module to support the new additions (with Yasmina)
- Tested the shifter, Control unit, and Data memory modules

Mon, Oct 28, 3:30pm - 10:30pm:

- Tested the whole program using multiple test cases that support all the instructions (with Yasmina)
- Fixed issues with the pc values and shifter values
- Fixing the control unit branch issue (with Yasmina)
- Wrote the Report.