THE AMERICAN UNIVERSITY IN CAIRO

الجامعة الأمريكية بالقاهرة

CSCE 3301

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Single Cycle implementation -

Project Report

Brief description of project

This project is an implementation of the single cycle RISC-V processor using verilog that will be supporting the instructions of the RV32I extension.

Structure

- RISC_Top.v
    - RISC_V.v: Has instances of all the modules needed to complete the full datapath.
        - RCA.v: Three instances for the pc calculations.
        - Registe_load_rst.v: used to store the current value of the pc.
        - BranchCu.v: used to determine whether the branch instruction will be executed or not.
        - InstMem.v: Stores the instructions of the program
        - ControlUnit.v: simulates the control unit of the datapath.
        - RegFile.v: simulates the register file by storing the contents of each register.
        - rv32_ImmGen.v: generates the needed immediates by all the instructions.
        - ALUcu.v: generates the needed ALUSel needed by the ALU to figure out which instruction to compute.
        - prv32_ALU.v: simulates how the ALU computes each instruction needed by it and generates all the flags needed
            - n_bit_shifter.v: This computes the output of the shifting instructions.
        - DataMem.v: simulates the data memory and stores the content of the data memory.
    - Four_Digit_Seven_Segment_Driver.v: used to display the pc on the seven segment display.

Problems and solutions

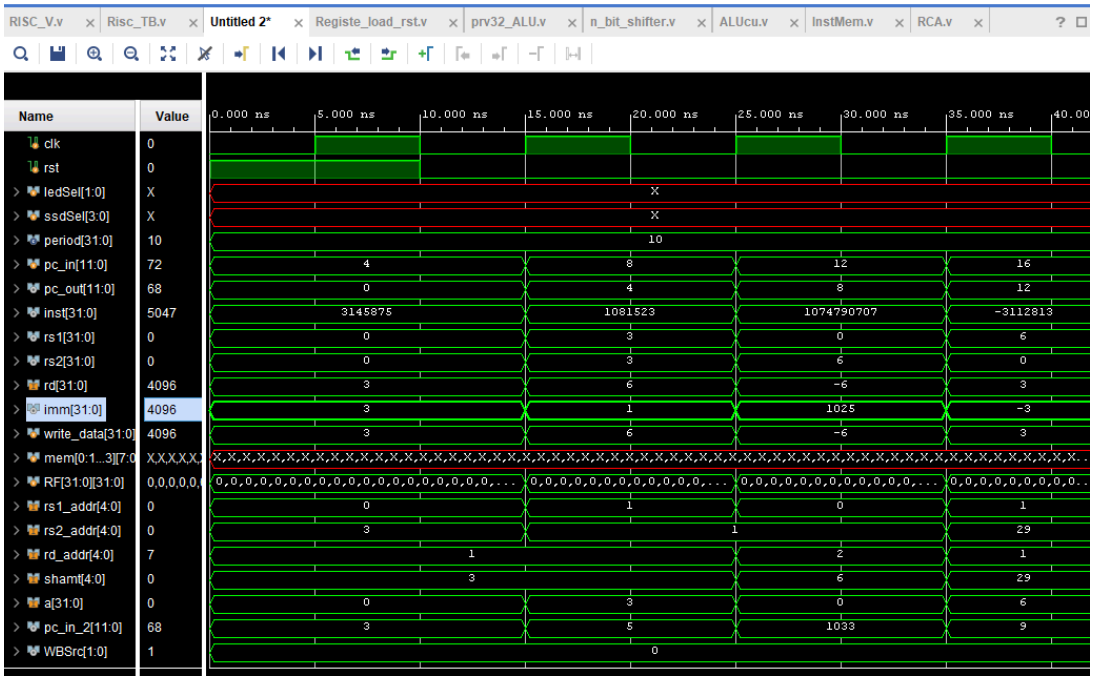
At the beginning of the testing process a number of issues were encountered.

They were as follows:
i1: pc not working correctly
s1: fixed the default values for the registers from 8 to 12 bits (PC size to accommodate 4KB memory)
i2: sra not working correctly; not sign-extending
s2: declared the input to be shifted as signed input
i3: I-type shifting not working as expected; shamt being read incorrectly
s3: Added a multiplexor to set shamt as rs2 for R-type and instr[24:30] for I-type
i4: auipc not working correctly; pc value is too small (12 bits) to use the output of target adder as auipc resulty
s4: added separate adder and wire for auipc result

Waveforms Snippets and Test Case Descriptions

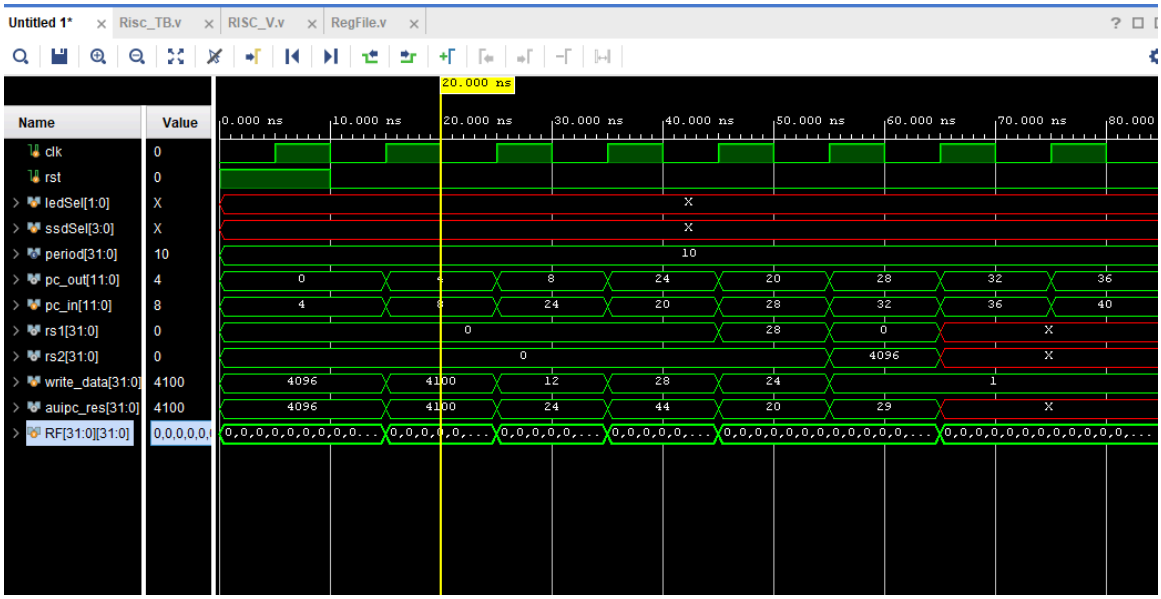
Test 1

Purposes: tests all R and I instructions except for load and jalr



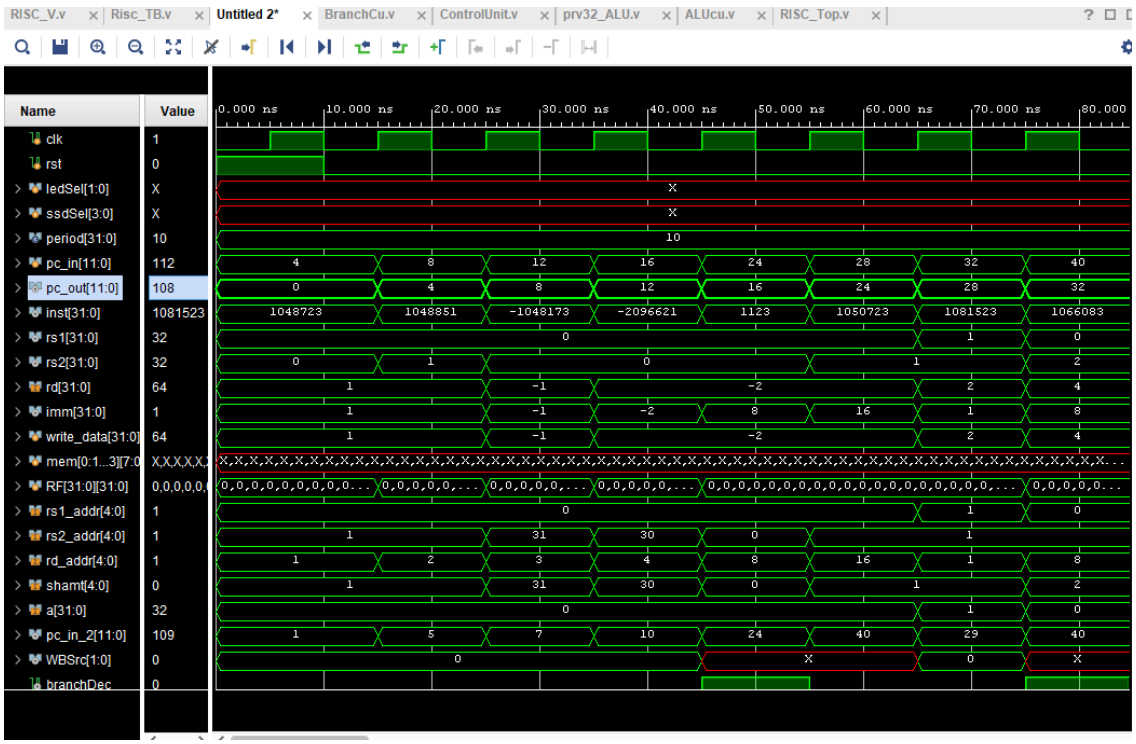
Test 2

Purposes: tests all S and load instructions



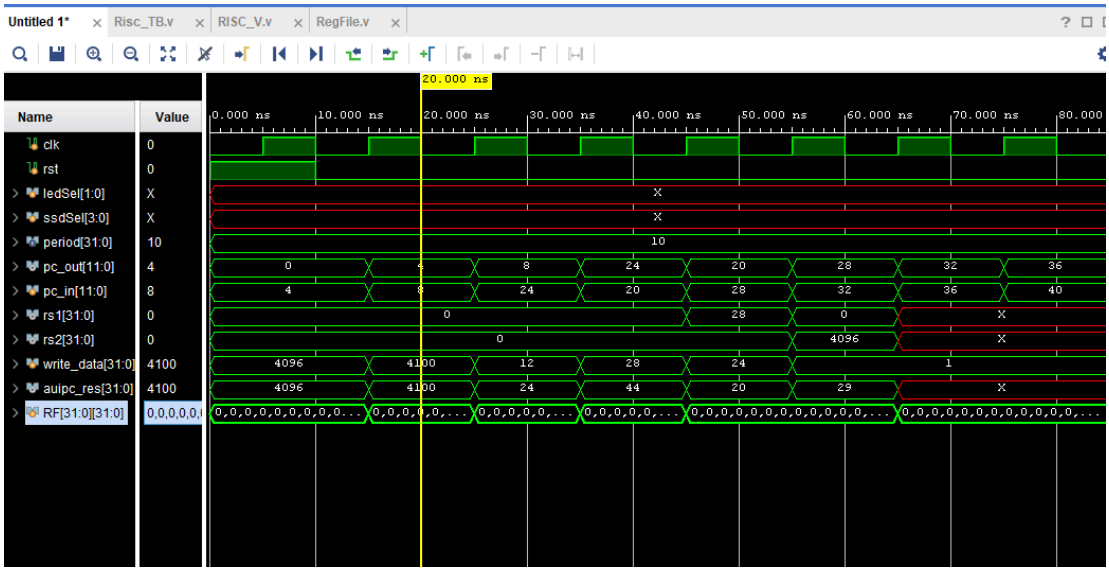
Test 3

Purpose: tests all branch instructions



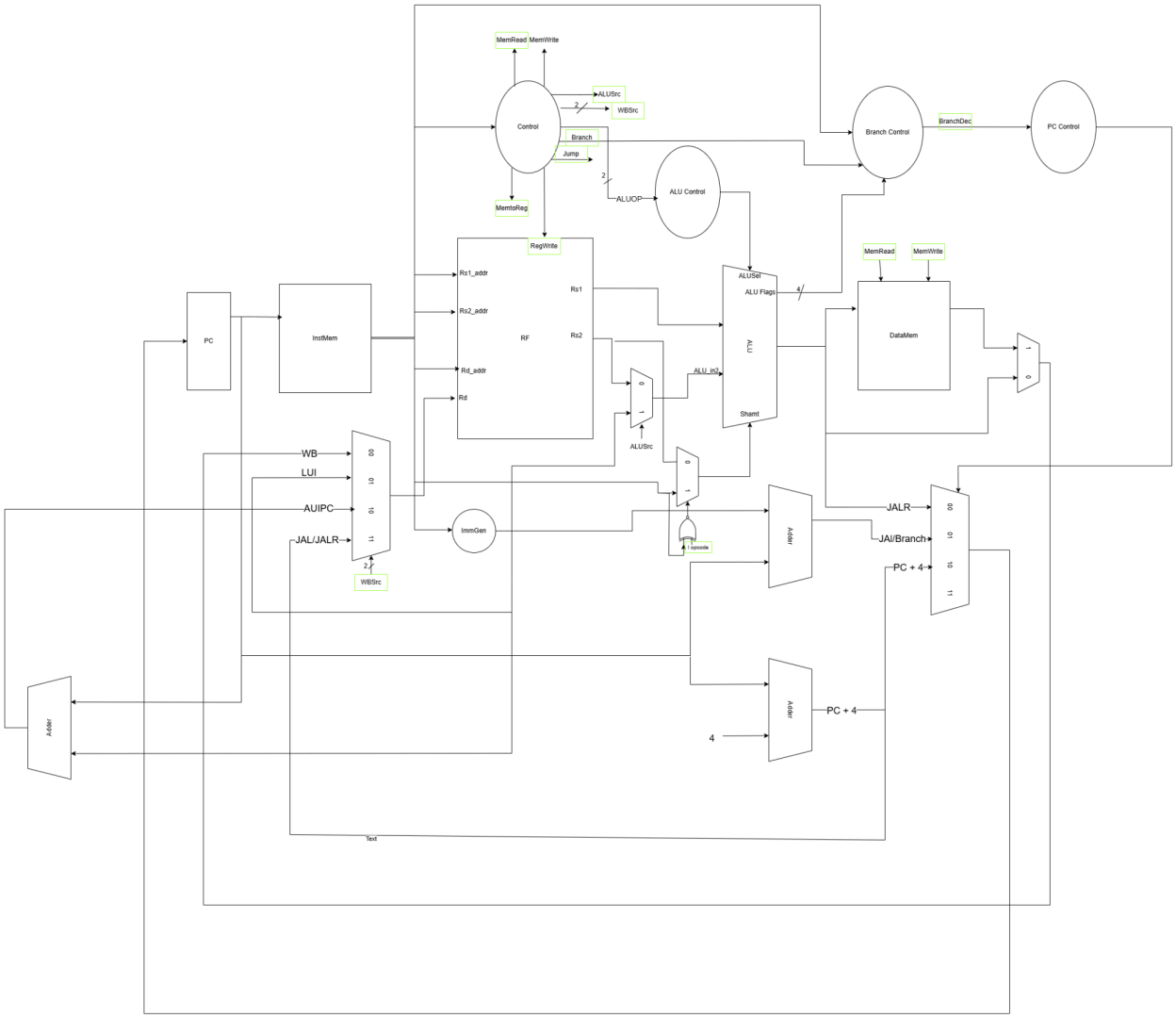
Test 4

Purpose: tests lui, auipc, jal, jalr



Final datapath

Note that clock, reset and instruction bits are not displayed on the datapath



References

Computer Architecture Slides, Dr Cherif Salama, Fall2024.