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Earlier (in the labs): created the base for the Single Cycle CPU

Mon, Oct 21, 1:00pm-2:00pm:

- discussed initial project details (with Rana)

Thurs, Oct 24, 3:30-5:00pm:

- discussed more details about the project (with Rana)
- Figured out extra components needed per every instruction format

Sun, Oct 27, 1:00pm-7:00pm:

- Started the datapath design
- Added the provided ALU and ImmGen (with Rana)
- Added the Branch CU that handles branching logic (with Rana)
- Modified the shifter module to fix issus (with Rana)
- Modified the CU (with Rana)
- Modified the ALUCu
- Modified the dataMem to support different load/store instructions, made the memory byte addressable and fixed the PC (with Rana)
- Added write back logic (with Rana)
- Added PC logic (with Rana)
- Integrated all the new additions to the RiscV (top) module (with Rana)

Mon, Oct 28, 3:30pm-12:00am:

- Wrote tests to support the different instruction formats
- Tested all the instructions (with Rana)
- Fixed minor issues (AUIPC not working correctly)
- Fixed control unit issue (with Rana)
- Finished the datapath
- Wrote the report (with Rana; mostly her)
- Wrote the readme