Department of Computer Science & Engineering
University of Rajshahi

Design of VLSI Circuits and Systems Lab

Lab Manual

CSE4152

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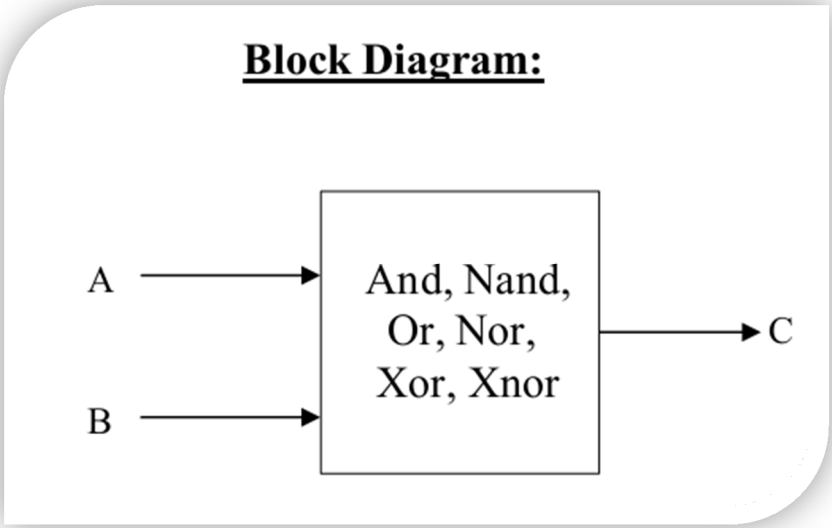
Rajshahi 6205, Bangladesh

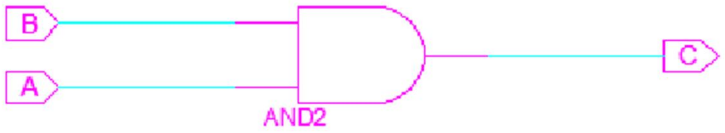
Assignment-1

Title: Design and simulate all the logic gates using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of all the logic gates gate level modeling style in VHDL using a Test bench.



RTL SCHEMATIC:



Simulation Waveforms

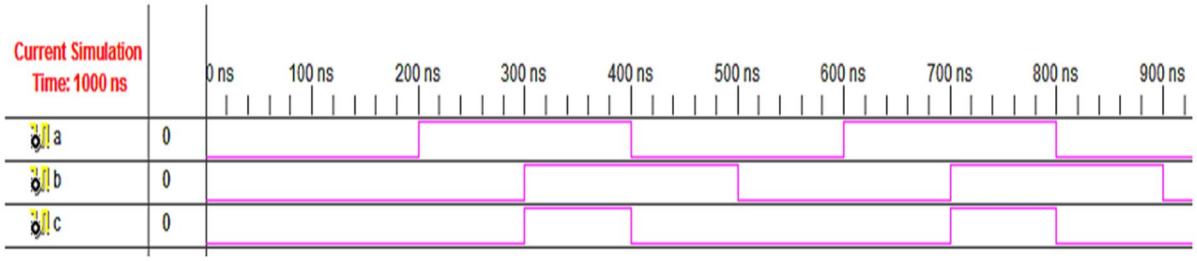


Figure-1: Schematic Diagram and Timing Diagram of AND gate.

Report Writing: For report writing instructions, just follow the following instructions:

- Name of the Program
- Program Areas

- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 50%.

Assignment-2

Title: Design and simulate 1-bit half adder using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of 1-bit half adder written in Gate level modeling style in VHDL using a Test bench.

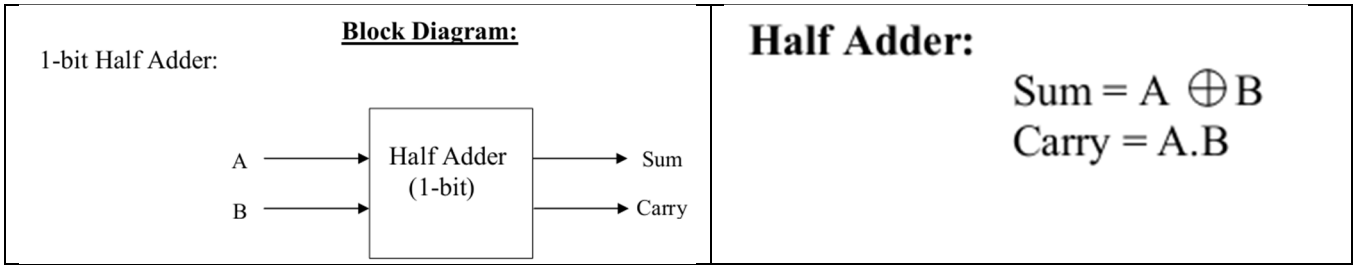


Figure-2: Schematic Diagram of 1-bit Half adder.

Report Writing: For report writing instructions, just follow the following instructions:

- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

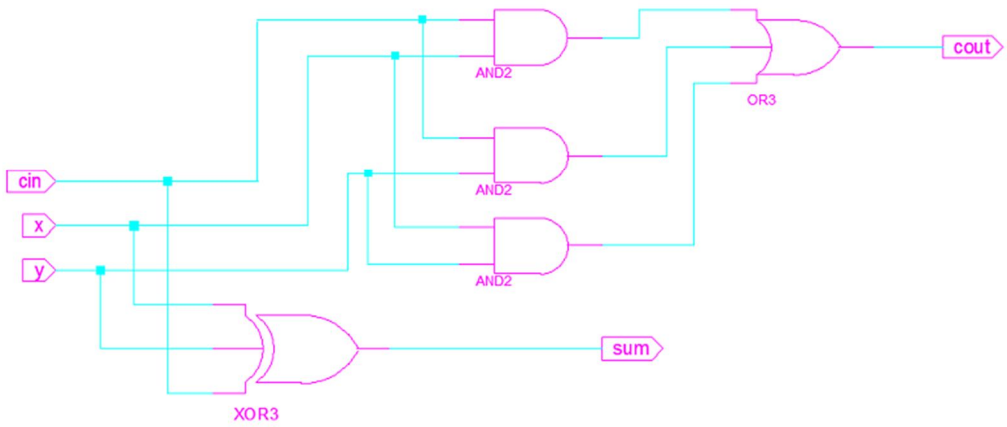
Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 70%.

Assignment-3

Title: Design and simulate Full adder using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of Full adder written in Gate level modeling style in VHDL using a Test bench.

RTL Schematic:



Simulation waveforms:

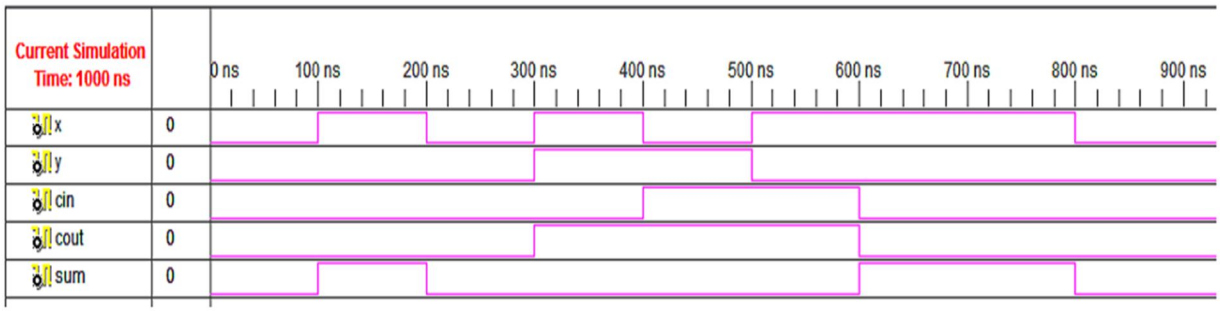


Figure-3: Schematic Diagram of Full adder.

Report Writing: For report writing instructions, just follow the following instructions:

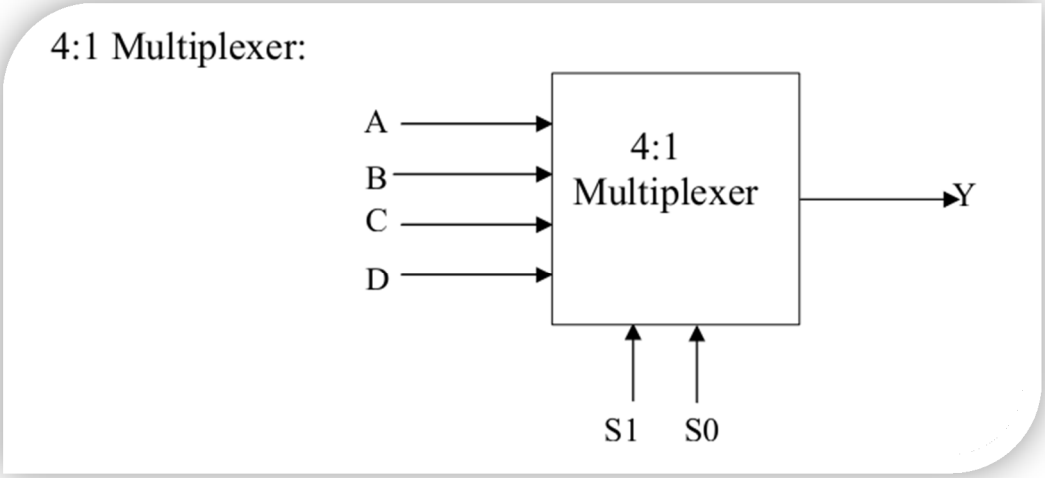
- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 100%.

Assignment-4

Title: Design and simulate 4:1 Multiplexer using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of 4:1 Multiplexer written in Gate level modeling style in VHDL using a Test bench.



4:1 Multiplexer:

$$Y = A.S1'.S0' + B.S1'.S0 + C.S1.S0' + D.S1.S0$$

Figure-4: Schematic Diagram of 4:1 Multiplexer.

Report Writing: For report writing instructions, just follow the following instructions:

- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 100%.

Assignment-5

Title: Design and simulate 1:4 Demultiplexer using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of 1:4 Demultiplexer written in Gate level modeling style in VHDL using a Test bench.

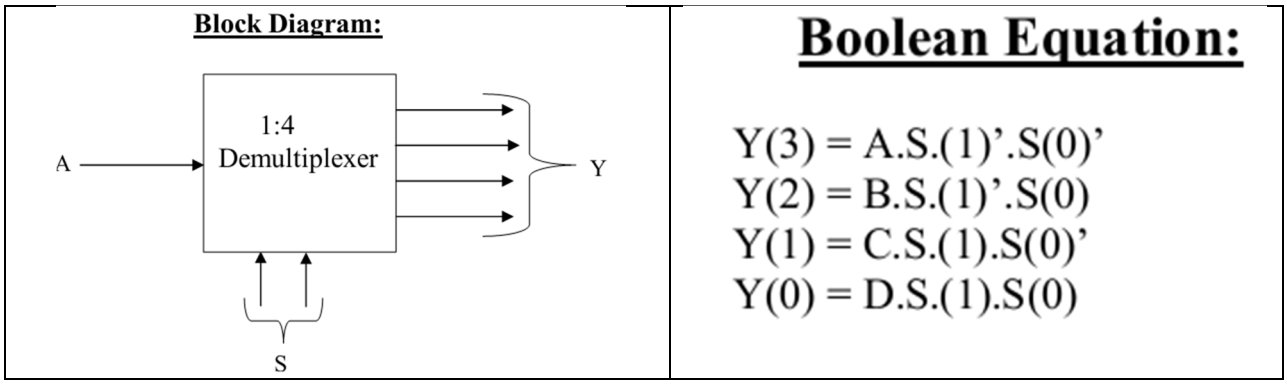


Figure-5: Schematic Diagram of 1:4 Demultiplexer.

Report Writing: For report writing instructions, just follow the following instructions:

- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 100%.

Assignment-6

Title: Design and simulate 3-to-8 line Decoder using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of 3-to-8 line Decoder written in Gate level modeling style in VHDL using a Test bench.

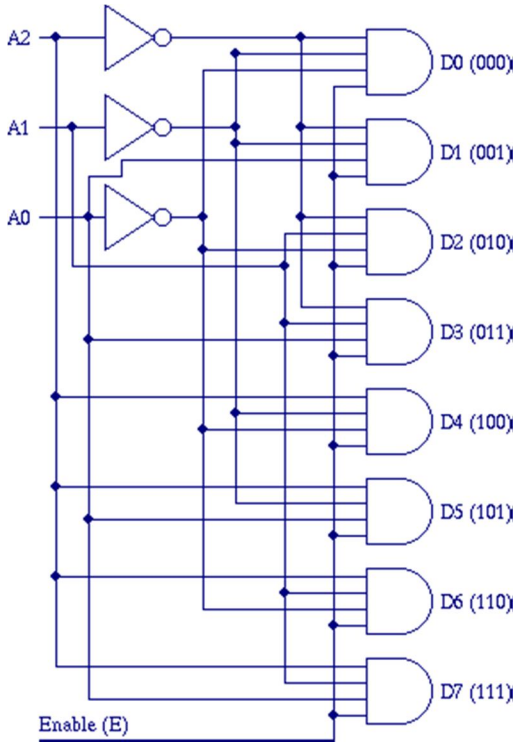


Figure-6: Schematic Diagram of 3-to-8 line Decoder.

Report Writing: For report writing instructions, just follow the following instructions:

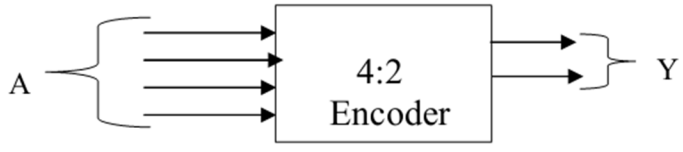
- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 100%.

Assignment-7

Title: Design and simulate 4-to-2 line Encoder using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of 4-to-2 line Encoder written in Gate level modeling style in VHDL using a Test bench.



Boolean Equation:

$$Y(1) = A(1) + A(0)$$
$$Y(0) = A(2) + A(0)$$

Figure-7: Schematic Diagram of 4-to-2 line Encoder.

Report Writing: For report writing instructions, just follow the following instructions:

- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 100%.

Assignment-8

Title: Design and simulate J-K Flip-Flop using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of J-K Flip-Flop written in Gate level modeling style in VHDL using a Test bench.

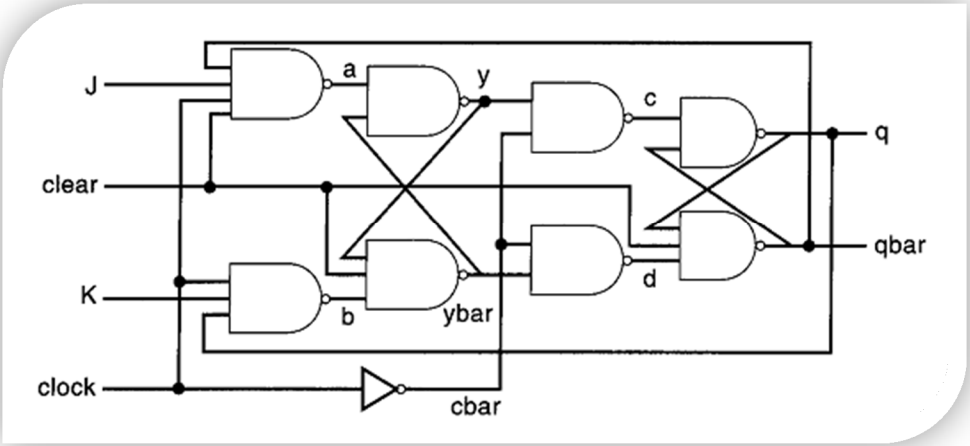


Figure-8: Schematic Diagram of J-K Flip-Flop.

Report Writing: For report writing instructions, just follow the following instructions:

- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 100%.

Assignment-9

Title: Design and simulate 4-bit Carry Look-ahead adder using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of 4-bit Carry Look-ahead adder written in Gate level modeling style in VHDL using a Test bench.

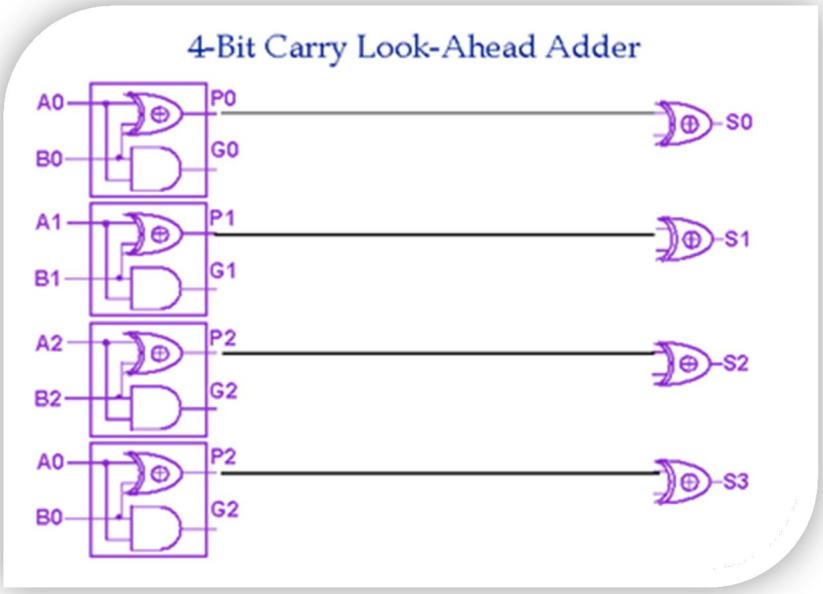


Figure-9: Schematic Diagram of 4-bit Carry Look-ahead adder.

Report Writing: For report writing instructions, just follow the following instructions:

- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 100%.

Assignment-10

Title: Design and simulate 4-bit BCD adder using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of 4-bit BCD adder written in Gate level modeling style in VHDL using a Test bench.

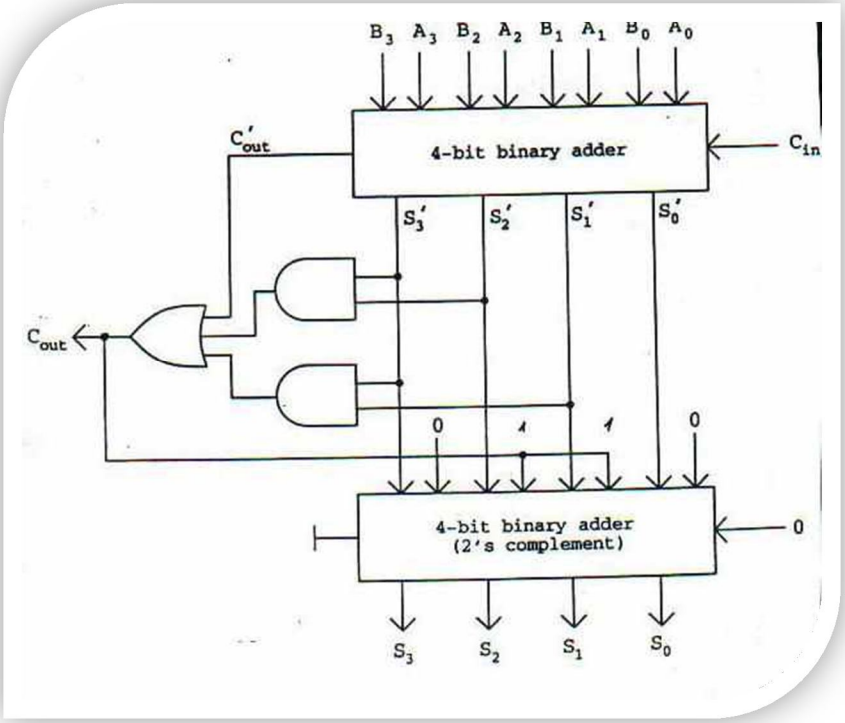


Figure-10: Schematic Diagram of 4-bit BCD adder.

Report Writing: For report writing instructions, just follow the following instructions:

- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 100%.

Assignment-11

Title: Design and simulate 4-bit Binary adder/subtractor using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of 4-bit Binary adder/subtractor written in Gate level modeling style in VHDL using a Test bench.

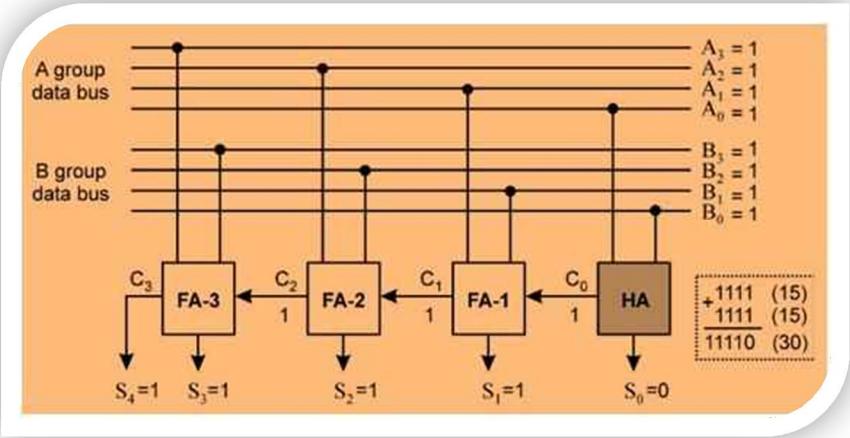


Figure-11: Schematic Diagram of 4-bit Binary adder/subtractor.

Report Writing: For report writing instructions, just follow the following instructions:

- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 100%.

Assignment-12

Title: Design and simulate 4-bit Synchronous Counter using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of 4-bit Synchronous Counter written in Gate level modeling style in VHDL using a Test bench.

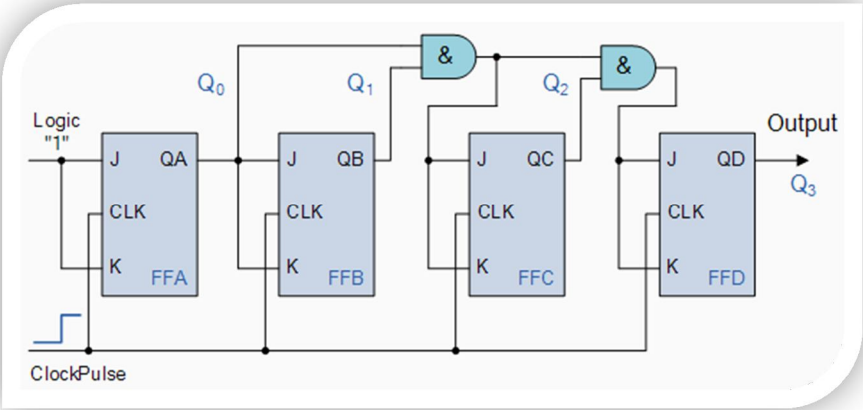


Figure-12: Schematic Diagram of 4-bit Synchronous Counter.

Report Writing: For report writing instructions, just follow the following instructions:

- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 100%.

Assignment-13

Title: Design and simulate 3-bit Asynchronous Counter using the gate level modeling style of VHDL.

Outline: Perform Zero Delay Simulation of 3-bit Asynchronous Counter written in Gate level modeling style in VHDL using a Test bench.

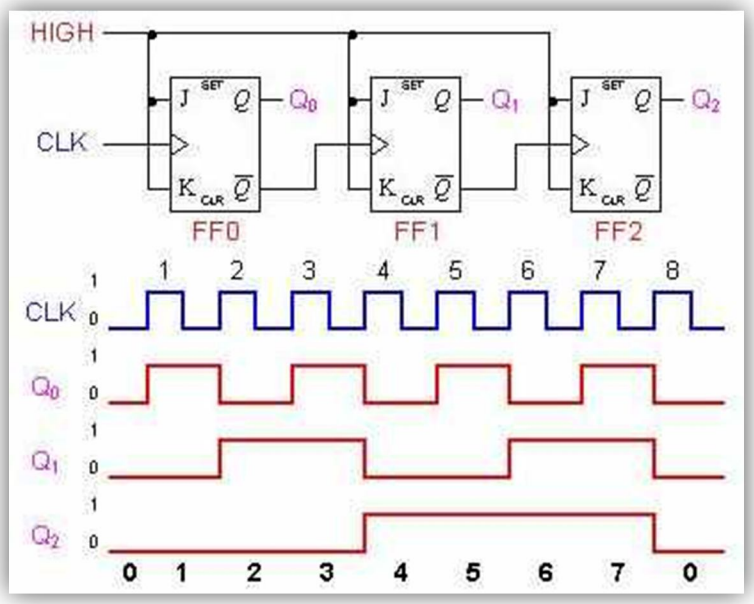


Figure-13: Schematic Diagram of 3-bit Asynchronous Counter.

Report Writing: For report writing instructions, just follow the following instructions:

- Name of the Program
- Program Areas
- Objectives
- Design Circuits
- Truth Table

Mode of Evaluation: Presentation, Implementation & Testing, and Viva.
Percentage of Weight: 100%.