CSE260 Lab Report-3

Experiment: Parity Generator and Checker

Group-1:

21301351_Md Tasrif Khan,
21301350_Fardeen Mohammad Monayem,
22101428_Sibgatullah Tasnim,
22101710_Md. Anwar Hossain

1) Name of the Experiment: Parity Generator and Checker.

2) Objective:

- To design and implement an Even Parity Generator and Even Parity Checker using XOR gates (IC-7486).

3) Required Components and Equipments: AT-700 Portable Analogue / Digital Laboratory, 7400-3, IC-7486, Trainer Board, Bread Board.

4) Experimental Setup: To start with, IC-7486 is taken which is of XOR gate. Using a wire, the IC's pin 14 was connected to "+5V" position whereas pin 7 was connected to "GND" position. Then, a parity generator circuit was prepared. Four inputs D_0, D_1, D_2 and D_3 were taken. D_0 and D_1 were connected to pin no. 1 and pin no. 2 respectively. Similarly, the inputs C and D were connected to pin no. 4 and 5. As a result, two outputs of XOR gates at pin no. 3 and pin no. 6 were prepared. After that, a wire was taken from pin no. 3 and pin no. 6 and were connected to pin no. 13 and pin no. 12 respectively. Finally, pin no. 11 was connected to the main output pin with a

Then we match the outputs with ~~out~~ the resultant truth table. Therefore, an Even Parity Generator was prepared. Similarly, an Even Parity Checker was also prepared. But in this case, an extra input P was taken. Just like before, the inputs D_0, D_1, D_2 and D_3 were taken. However, the input of P was taken from pin no.9. The circuit arrangement of the first four inputs was the same as before. According to the previous arrangement, pin no.11 was the main output. But ~~now~~ then we had to connect pin no.11 and pin no.10 using a wire which was not done before. Therefore, taking inputs from pin no.9 and 10 ~~we got~~ the final resultant output was got from pin no.8 and it was connected to the main output pin with a wire. After that, we matched the results with our resultant truth table.

5) Results in Tabulated Form:

P	D_3	D_2	D_1	D_0
0	1	0	1	0
1	1	1	1	0
1	1	1	1	1
1	0	0	0	0

Figure-1: Even Parity Generator

P	D_3	D_2	D_1	D_0	Result
0	1	0	1	0	0
1	1	1	1	0	0
1	1	1	1	1	1
1	0	0	0	0	1

Figure-2: Even Parity Checker

6) Discussions (Explanation of results): From the resultant truth table of Even Parity Generator and Even Parity Checker a little difference was seen in case of results. The difference was that if the inputs of D_3, D_2, D_1 and D_0 are taken as 1, 1, 1 and 0 then in case of Even Parity Generator, the output was 1 and in case of Even Parity Checker the output was 0.