CSE260 Lab Report-4

Experiment: Design and Implementation of 4-bit Parallel Binary Adder

Group-1:

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1) Name of the Experiment: Design and Implementation of 4-bit Parallel Binary Adder

2) Objective:

- Creating a Half Adder, Full Adder and 4-bit Parallel Adder.

3) Required Components and Equipment: Bread Board, Trainer Board, Wire, IC-7486 (XOR gate), IC-7408 (AND gate), IC-7432 (OR gate) and IC-7483.

4) Experimental Setup: At first a Half Adder was prepared. The Half Adder was prepared using one IC-7486 (XOR gate) and one IC-7408 (AND gate). According to the truth table of Half Adder, it was seen that the carry part of the two inputs follow the truth table of AND gate and the sum part follows the truth table of XOR gate. Now, for IC-7486 pin no.1 and pin no.2 were taken as inputs. Then, ~~we match~~

~~the~~ outputs were matched with the truth table of sum part after connecting a wire to the output pin from pin no. 3. Similarly the carry part was created using a wire from pin no. 3 of IC-7408 and matched the outputs. As a result, A half-adder was prepared.

After that, a full adder was prepared. In this case IC-7486 (XOR gate), IC-7408 (AND gate) and IC-7432 (OR gate) were used. The first part of the Full Adder was done using a Half Adder. But in this case 3 inputs were taken. Now, from the XOR gate prepared before which was got from the output pin no. 3 of IC-7486 (XOR gate) a wire was taken from output pin no. 3 to output pin no. 4. After that a new input was taken and connected to the pin no. 5 of IC-7486 (XOR gate). As a result, the we a main output was taken

from pin no.6 to the output pin using a wire. So, we got the sum part of full Adder. Then again, another wire was taken from IC-7486 (XOR gate) and connected to the pin no.5 of IC-7408 (AND gate). A wire was also taken from pin no.3 of IC-7486 (XOR gate) and connected to pin no.4 of IC-7408 (AND gate). Now, from pin no.6 of IC-7408 (AND gate) another wire is taken and connected to pin no.1 of IC-7432 (OR gate). Similarly, we take yet another wire from pin no.3 of IC-7408 (AND gate) and connect it to pin no.2 of IC-7432 (OR gate). As a result, the output of carry was got from pin no.3 of IC-7432 (OR gate).

Now, after preparing a Half Adder and A Full Adder, a 4-bit parallel adder was prepared. In this case a new IC was used. The name of the IC is IC-7483. For this IC, pin no.5 was taken as "+5V" and pin no.12 was taken as "GND" or Ground. For preparing the 4-bit parallel binary Adder 8 inputs were taken which are A_4, A_3, A_2, A_1, B_4, B_3, B_2 and B_1 respectively. A_4 was taken from pin no.1 taking input from the input pin and connecting it to pin no.1 of IC-7483 using a wire. Similarly, A_3 was taken from pin no.3, A_2 from pin no.8, A_1 from pin no.10, B_4 from pin no.16, B_3 from pin no.4, B_2 from pin no.7 and B_1 from pin no.11. After that, connections were made for the 4

sums and 1 carry. The sums were taken as $\Sigma_4, \Sigma_3, \Sigma_2, \Sigma_1$ and carry was taken as C_4. Σ_4 was taken from pin no. 15, Σ_3 from pin no. 2, Σ_2 from pin no. 6, Σ_1 from pin no. 9 and C_4 from pin no. 14. After that the sums and carry were connected to the main output pins serially. Thus, ~~out~~ the 4-bit Parallel Binary Adder was prepared. So, ~~out~~ Half Adder, Full Adder and 4-bit Parallel Binary Adder was prepared.

5) Results (Truth Table) and Discussions:

X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Figure-1: Truth Table of Half Adder Circuit

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Figure-2: Truth Table of Full Adder

For the truth table of Half Adder, the output of S of Figure-1 represents XOR gate and C of Figure-1 represents AND gate. For the Full Adder, the sum part $S = X \oplus Y \oplus Z$ and for the

carry part $C = XY + Z(X \oplus Y)$. We can also make the 4-bit Parallel Adder into an Adder or Subtractor. For doing so, B1 needs to be taken from pin no. 11 of IC-7483 and connected as input in IC-7486 (XOR gate). Similarly, B_2, B_3 and B_4 also needs to be connected with C_0 which is common in all steps. For making it an adder C_0 can be taken as 0 and for subtractor C_0 can be taken as 1.