CSE260 Lab Report-2

Experiment: Universal gates and Applications of Boolean Algebra

Group-1:

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Name of the Experiment:

Universal gates and applications of boolean algebra.

Objective:

(i) To investigate the rules of boolean algebra.

(ii) To gain experience working with practical circuits.

(iii) To simply a complex function using boolean algebra.

Required components & Equipments:

Trainer board, bread board, IC-7400 & IC-7402 logic gates, AT-700 portable analog / digital laboratory, a 7400×1 and wires.

Experimental setup:

1. To begin with, a trainer board, bread board, IC-7400 and IC-7402 which represents NAND as well as NOR gate ~~which~~ were used for the experiment. Now, at first the AND gate was implemented using the

NAND gate. And for conducting this experiment pin no 1 & 2 were used for input. After that pin no 3 was used for connection to take inputs on pin no 4 & 5. Now, a wire was taken from pin no 6 and connected to the output and using the bulb light connection it was verified that the resultant gate was that of AND gate which was implemented using NAND gate. However, pin no 7 and 14 were used according to GND position and +5V position using the wires.

2. Similarly, an experiment was conducted using NOR gate to represent AND gate. Here, also pin no 7 was used at GND and 14 at +5V. But the only difference here occurs in input and output positions. At first, pin no 2 was used as A and a wire was connected to pin no 3 from pin no 2. And $\overline{A}$ was got from pin no 1. After that, pin no 5 was used to connect with B and again a

wire was taken from pin no 5 and connected with pin no 6. Then $\bar{B}$ was connected with pin no 4. And lastly, pin no 1 was used at pin no 11 and pin no 4 at pin no 12 as inputs. Therefore, pin no 13 was the main output.

3. For the final experiment ~~but~~ which is building circuits ~~using~~ using NAND gates, results to XOR gate. And for the setup like before the 7 no pin and 14 no pin were used for GND and +5V charge respectively. Now, as it is a circuit by NAND gate, the process of using pin no 1 & 2 as input and pin no 3 as y_1. Here, A was considered as input from pin no 1 and B as input from pin no ~~2~~ 2 accordingly. ~~After that~~, an assumption was taken by using y_1 in pin no 3. Moreover, A and y_1 were taken as input in pin no 4, 5

and got y_2 from pin no 6. Again, B & y_1 was taken as inputs in pin no 9 & 10 and got corresponding output from 8. Then, for easy calculation the previous outputs y_2 and y_3 were considered as input in pin no 12 & 13 which gave us the resultant output from pin no 11. Finally, the outputs matched with the truth table of XOR gate.

[4] Results:

(*) Simplification:

Here,

$$\overline{AB} = \overline{A} + \overline{B} = y_1$$

$$y_2 = \overline{A y_1} = \overline{A \cdot (\overline{A} + \overline{B})} = \overline{A} + (\overline{\overline{A}} \cdot \overline{\overline{B}}) = \overline{A} + AB$$
$$= \overline{A} + B$$

$$y_3 = \overline{B \cdot y_1} = \overline{B \cdot (\overline{A} + \overline{B})} = \overline{B} + (\overline{\overline{A}} \cdot \overline{\overline{B}}) = \overline{B} + AB$$
$$= \overline{B} + A$$

[De morgan's law]

$$y_4 = \overline{y_2 \cdot y_3} = \overline{y_2} + \overline{y_3} = (\overline{\overline{A} + B}) + (\overline{\overline{B} + A})$$

$$= (\overline{\overline{A}} \cdot \overline{B}) + (\overline{\overline{B}} \cdot \overline{A})$$

$$= A\overline{B} + B\overline{A} = A\overline{B} + \overline{A}B = A \oplus B$$

$= XOR$ gate

Truth Table:

A	B	$\overline{A}$	$\overline{B}$	$A\overline{B}$	$\overline{A}B$	$A\overline{B} + \overline{A}B$
0	0	1	1	0	0	0
1	0	0	1	1	0	1
0	1	1	0	0	1	1
1	1	0	0	0	0	0