

FIT3143 Tutorial Week 11

Lecturers: ABM Russel (MU Australia) and Vishnu Monn (MU Malaysia)

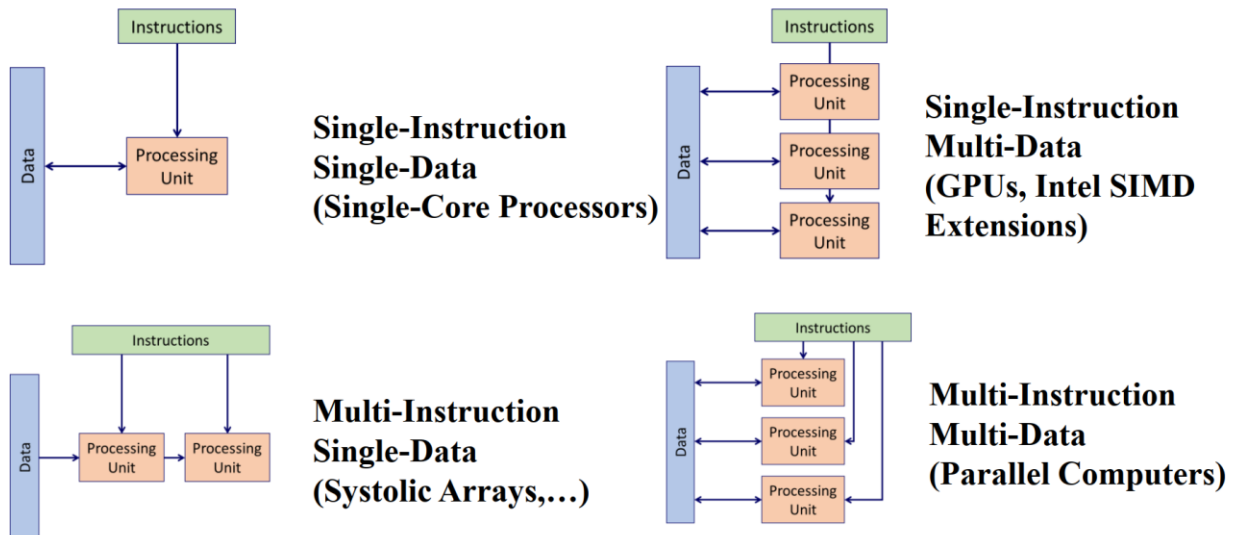
SIMD

OBJECTIVES

- Understand the concepts of the SIMD architecture and features

TOPICS

- 1) Using illustrations, describe Flynn's Taxonomy.

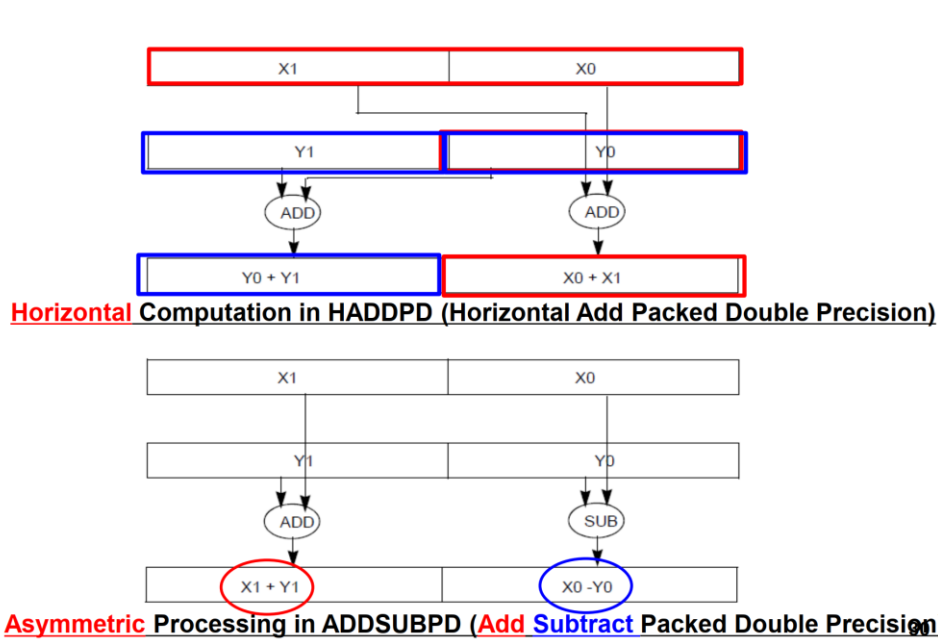


Further reading: <https://www.geeksforgeeks.org/computer-architecture-flynns-taxonomy/>

- 2) Compare SSE3 and SSE2. In detail, describe the new features of SSE3 and how it differs with SSE2. You can include illustrations to describe these features.

The most notable change in SSE3 is its capability to work horizontally in a register, as opposed to the more or less strictly vertical operation of all previous SSE instructions.

SSE3 also added instructions to perform different operations on the SIMD data, e.g. subtraction for the 1st pair of data and addition for the 2nd pair (asymmetric processing).



- 3) List key improvements of AVX over SSE4.

Widened data path from 128 bits to 256 bits and 3-operand instructions (up from 2).

- 4) Using a table, compare the features of MMX, SSE, SSE2, SSE3, SSE4 and AVX.

1997	1999	2000	2003	2007	2011
MMX	SSE	SSE2	SSE3	SSE4	AVX
<ul style="list-style-type: none"> - 8 64 bit registers - MM0 → MM7 - Shares register with X87 FPU - Only performs integer-based vector operations - Cannot perform integer and FPU 	<ul style="list-style-type: none"> - 8 128 bit registers, expandable to 16 registers for 64 bit architectures - XMM0 → XMM15 - Performs floating point based vector operations. 	<ul style="list-style-type: none"> - Enabled both integer and floating based operations to be performed using the XMM registers 	<ul style="list-style-type: none"> - Horizontal operations - Asymmetric processing 	<ul style="list-style-type: none"> - Additional instructions for vector operations 	<ul style="list-style-type: none"> - 16 256 bit registers - YMM0 → YMM15 - New instructions for vector operations.

operations simultaneously	- Integer based operations carried out using MMX				
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