

Lec 1 Introduction to M152A

Weitong Zhang

Overview

- Introduction
- Syllabus Overview
- **Install Xilinx ISE**

About this course

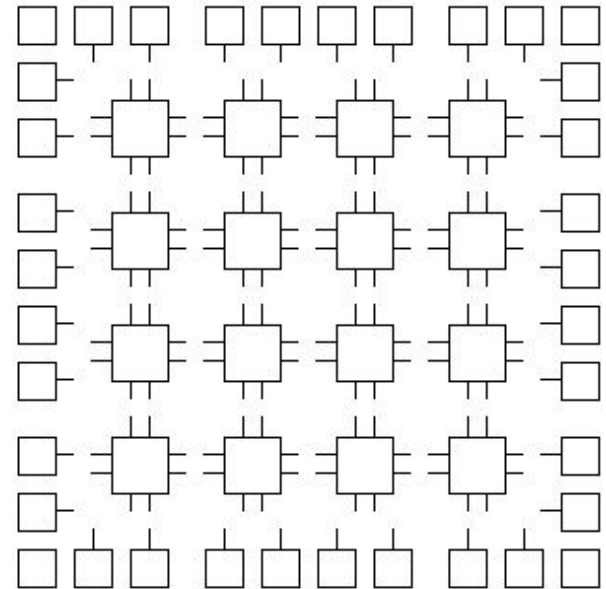
- Professor: Majid Sarrafzadeh (majid@cs.ucla.edu)
- Me:
 - Weitong Zhang, 2nd year Ph.D. student in CS
 - My research interest: Machine Learning (Theory), Reinforcement Learning
 - <https://web.cs.ucla.edu/~weightzero>, weightzero@ucla.edu
 - Office hour by appointment, but typically we can handle individual questions in class by breakout rooms.

Introduction

- Design implementation on Field Programmable Gate-Arrays (FPGAs)
- Knowledge basis: CS51A or ECE M16 (Digital circuits)
- Method: Programming using Verilog Hardware Design Language
- 4 Projects (2 Weeks each)
 - P1: Combinational Circuit basic (Float point number converter)
 - P2: Sequential Circuit basic (Clock divider)
 - P3: Finite State Machine (Vending Machine)
 - P4: FSM (Parking Meter)

Introduction - FPGA

- Programmable circuit.
- Integrated circuit designed to be configured by a customer or a designer after manufacturing.
- Technique (you don't need to know it in detail.):
 - Programmable Register / Gates
 - Use USB - UART port from PC to programm
- Why FPGA?
 - Comparing to circuit?
 - Comparing to CPU?
- How to program FPGA?
 - Verilog HDL (Hardware Design Language)
- Will cover this part in future.



FPGA applications

- Aerospace and Defense
- Consumer Electronics
- Digital displays, digital camera
- Data Centers
- High Performance Computing
- Machine Learning and Neural Network training

Syllabus and Schedule

Key takeaways

- Lecture: attendance required, quiz on CCLE
 - Q/A part: work as office hour / discussion session
- Projects
 - Work individually, only discuss high level ideas or very minor bugs in code
 - No deadline extension
 - Submission: follow the instructions in syllabus
- My office hours if you want an appointment: weightzero@ucla.edu

Questions & break

Xilinx ISE installation

Xilinx ISE Installation

Follow my notes

(<https://web.cs.ucla.edu/~weightzero/teaching/CSM152A-21S#how-to-start-with-xilinx-ise-design-suite>) or the files on CCLE

If you