Circuitos Lógicos e Organização de Computadores

Capítulo 3 – Tecnologia de Implementação

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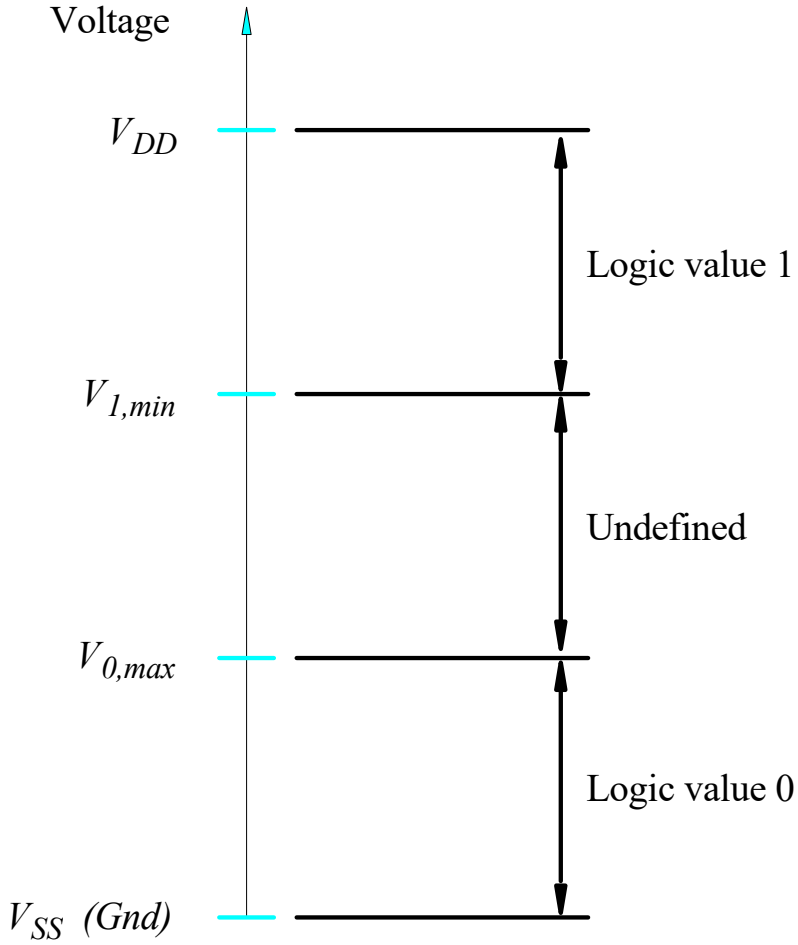
Tensão relativas aos níveis lógicos – Tecnologia MOS



Níveis Lógicos

0 – low – baixo
1 – high – alto
} Lógica Positiva

0 – high – alto
1 – low – baixo
} Lógica Negativa

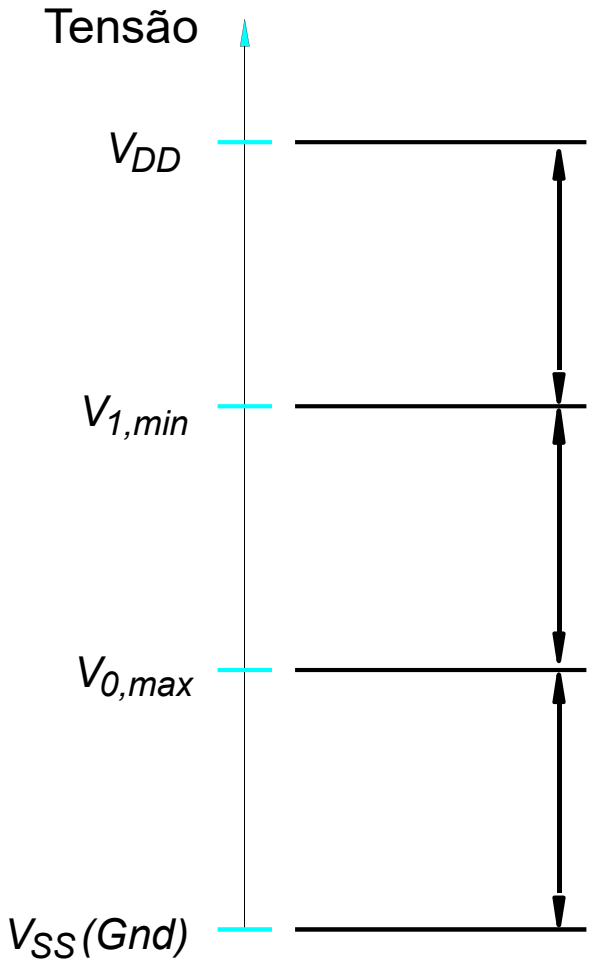
Valores Típicos:

V_{DD} = 5 V ou 3.3 V e V_{SS} = 0 V

V1,min = 60% V_{DD}

V0,max = 40% V_{DD}

Tensão relativas aos níveis lógicos



Valor lógico 1

Valor lógico indefinido

Valor lógico 0

Níveis Lógicos

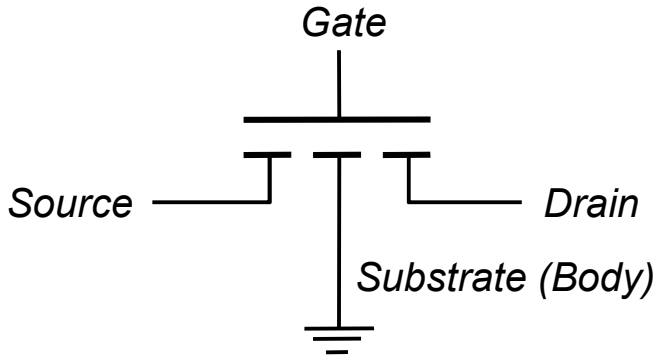
Valores para V_{DD} = 3.3 V e V_{SS} = 0 V

V1,min = 2,0 V

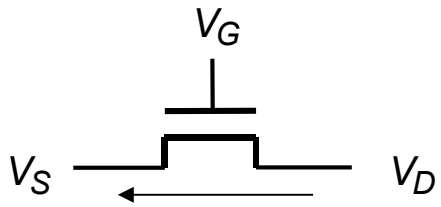
V0,max = 0,8 V

Transistor NMOS como uma chave

(a) Uma chave controlada por uma entrada x



(b) Transistor NMOS



(c) Símbolo simplificado de um transistor NMOS

MOS – Metal Oxide Semiconductor

NMOS – MOS tipo N (canal N – Substrato P)

Gate - Porta

Source – Fonte

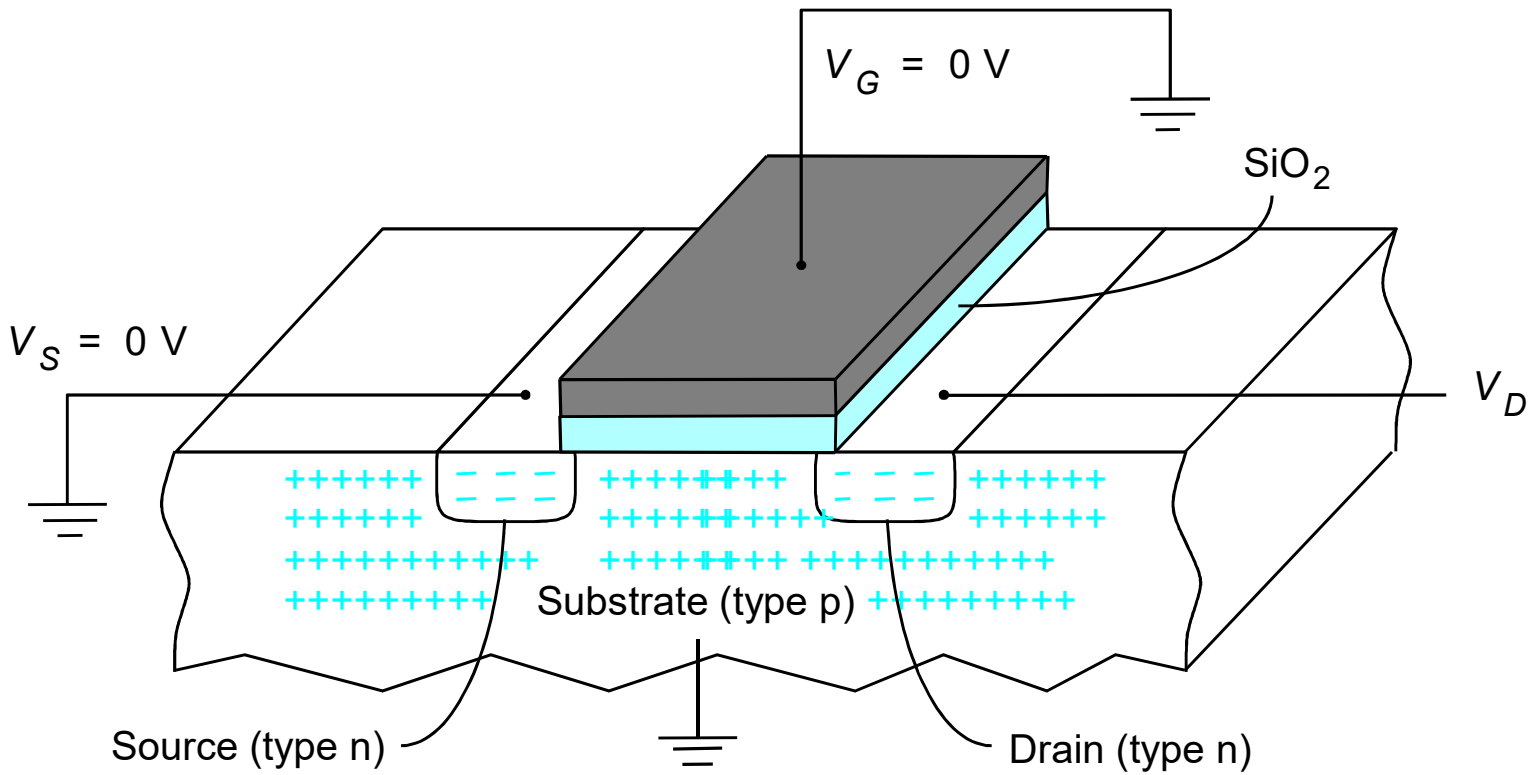
Drain - Dreno

Susbstrate (body) – substrato

Se V_G é baixo, não há formação de canal entre fonte e dreno → transistor não conduz → transistor aberto (turned off)

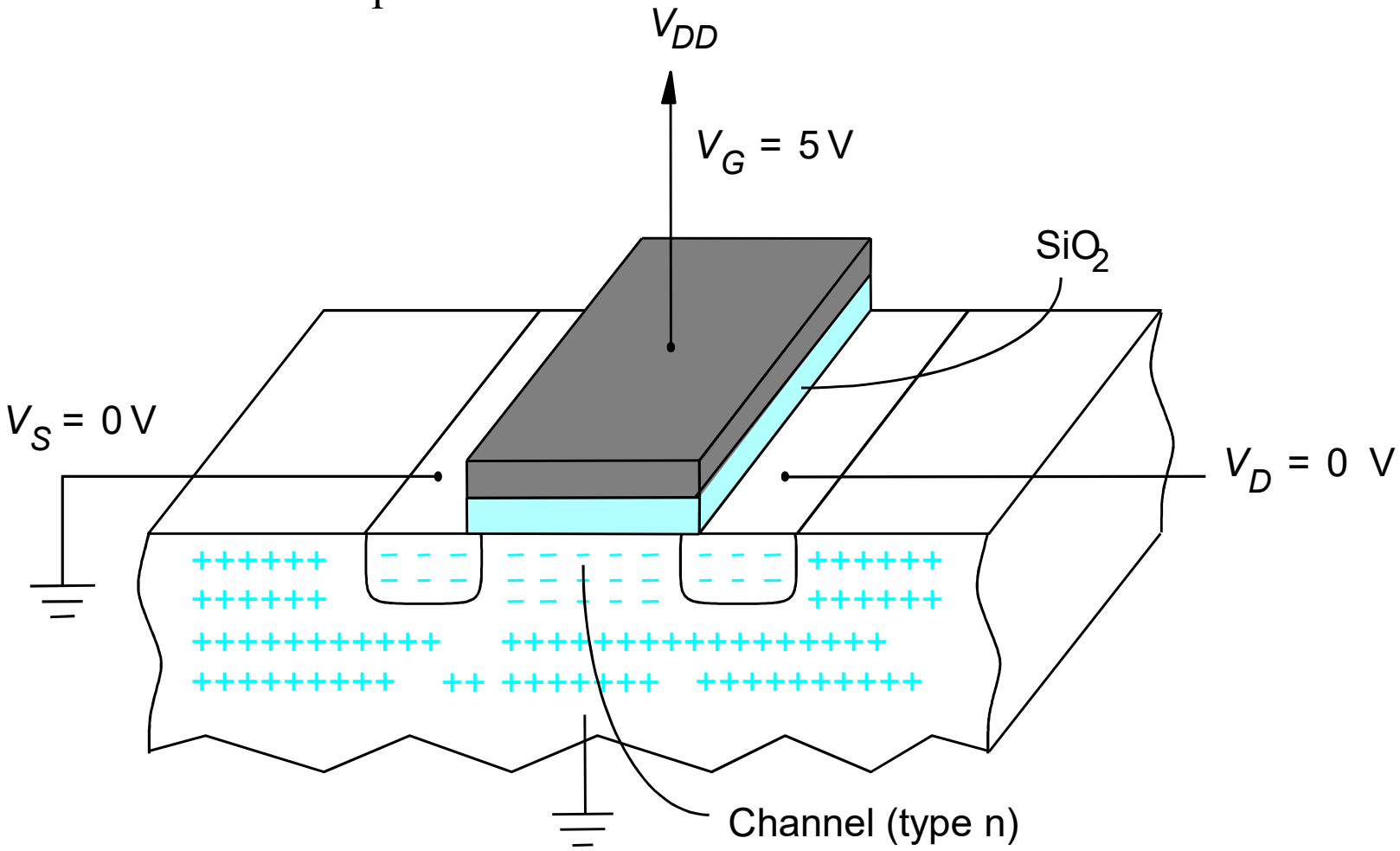
Se V_G é alto, há formação de canal entre fonte e dreno → transistor conduz → transistor fechado (turned on)

Comportamento de um transistor MOS - NMOS



(a) Quando V_{GS} = 0 V, o transistor está off

Comportamento de um transistor MOS - NMOS

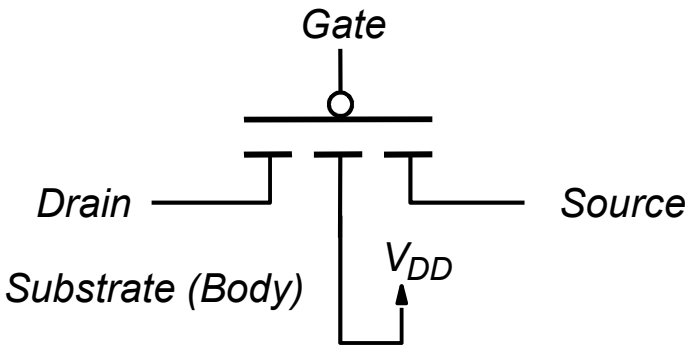


(b) Quando V_{GS} = 5 V, o transistor está on

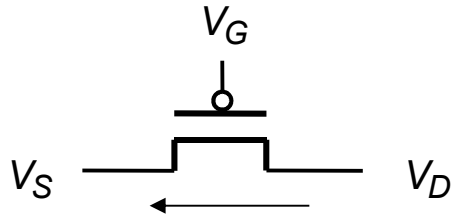
$V_{GS} > V_T \rightarrow$ há a formação do canal

Transistor PMOS como uma chave

(a) Uma chave com comportamento oposto ao do slide anterior



(b) Transistor PMOS



(c) Símbolo simplificado de um transistor PMOS

PMOS – MOS tipo P (canal P – Substrato N)

Gate - Porta

Source – Fonte

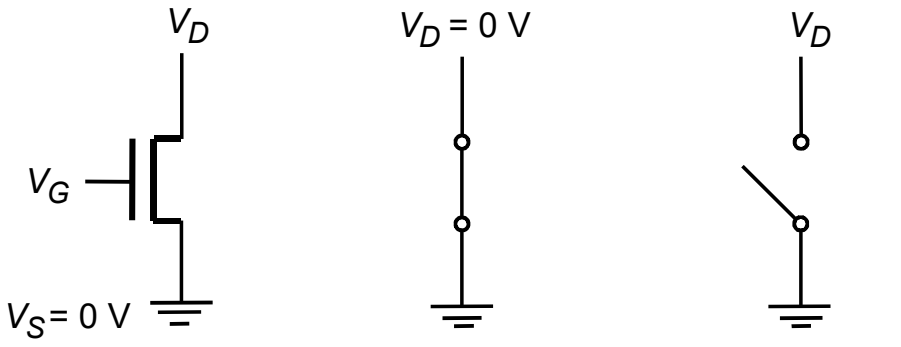
Drain - Dreno

Susbstrate (body) – substrato

Se V_G é baixo, há formação de canal entre fonte e dreno → transistor não conduz → transistor fechado (turned on)

Se V_G é alto, não há formação de canal entre fonte e dreno → transistor não conduz → transistor aberto (turned off)

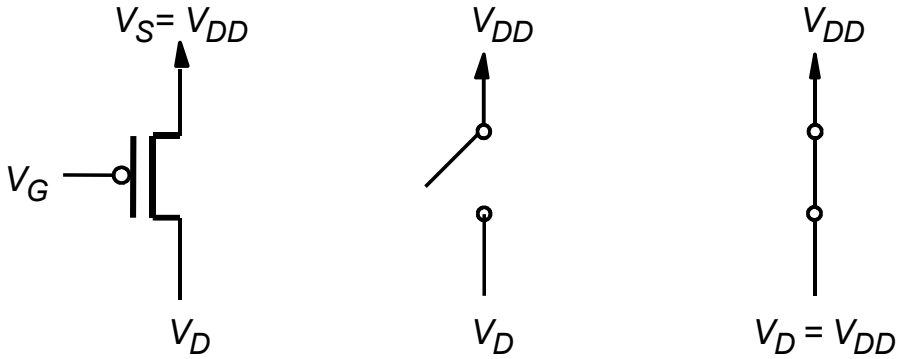
Transistores NMOS e PMOS em circuitos lógicos



Chave fechada quando $V_G = V_{DD}$

Chave aberta quando V_G = 0 V

(a) Transistor NMOS

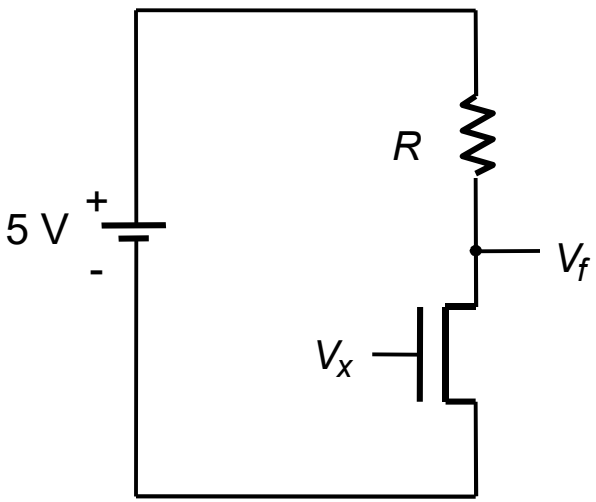


Chave Aberta quando $V_G = V_{DD}$

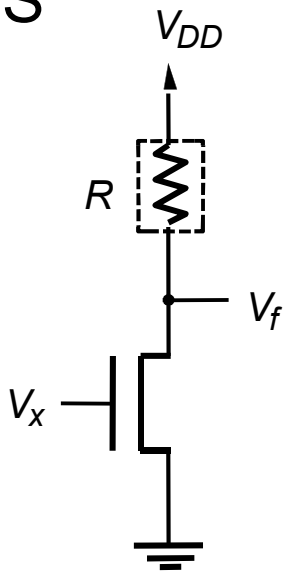
Chave fechada quando V_G = 0 V

(b) Transistor PMOS

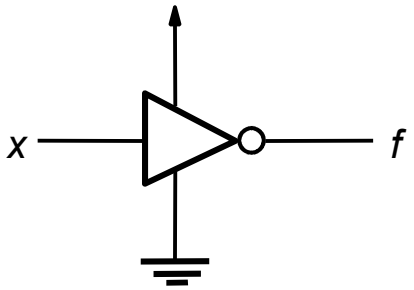
Uma Porta Inversora – NOT - construída com tecnologia NMOS

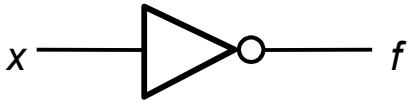


(a) Diagrama do Circuito



(b) Diagrama simplificado



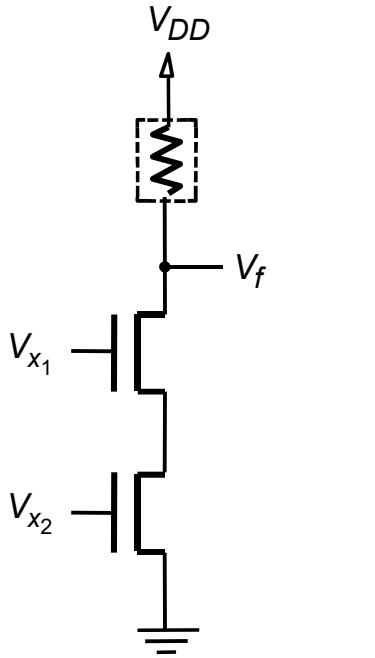


(c) Símbolos Gráficos

Vf = 0,2 V quando Vx = 5 V

O resistor é um limitador de corrente (na prática, outro transistor)

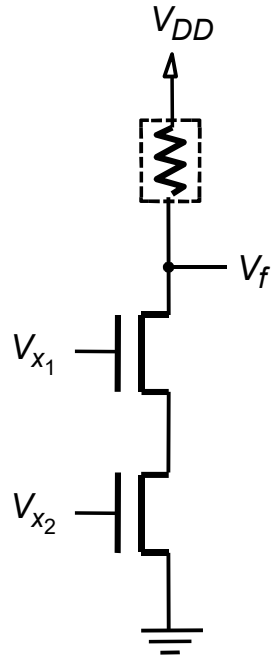
Porta com tecnologia NMOS



(a) Circuito

(b) Tabela Verdade

Porta NAND com tecnologia NMOS



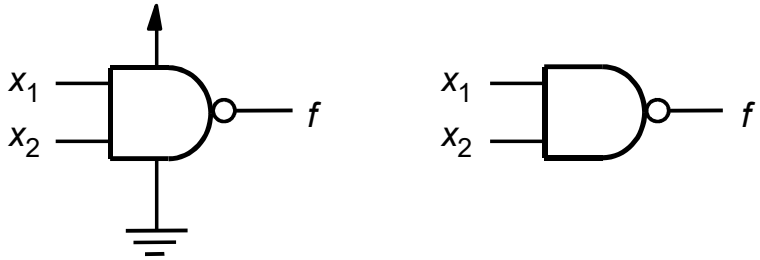
(a) Circuito

x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

(b) Tabela Verdade

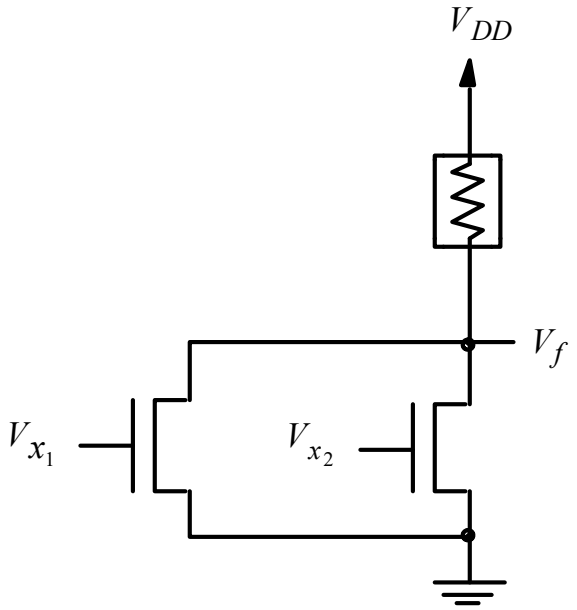
Vx1	Vx2	Vf
L	L	H
L	H	H
H	L	H
H	H	L

NAND



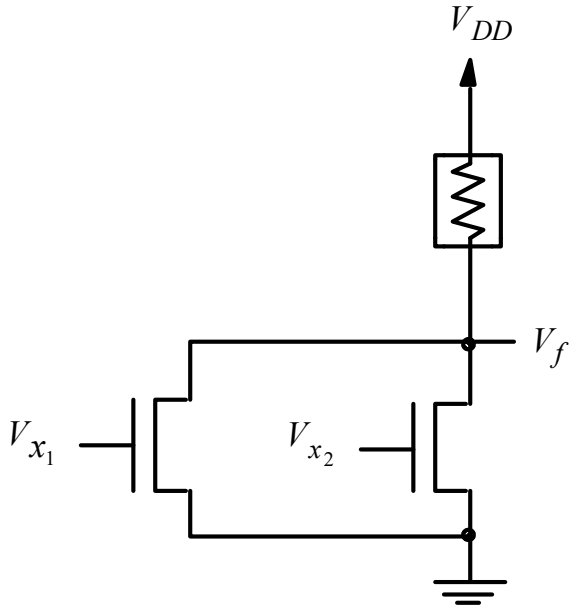
(c) Símbolo Gráfico

Porta com tecnologia NMOS



(a) Circuito

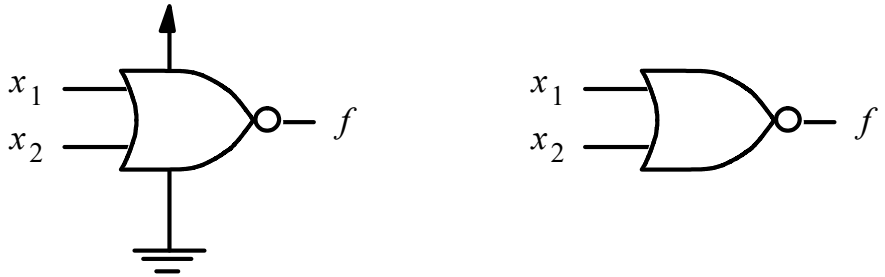
Porta NOR com tecnologia NMOS



x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

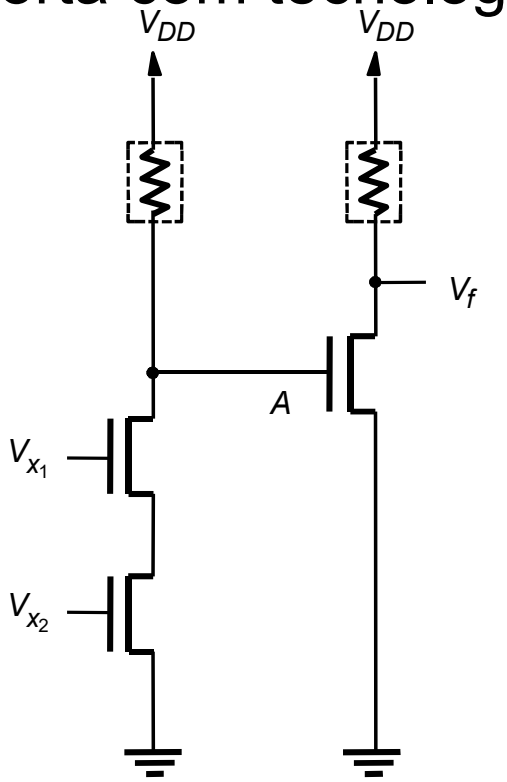
Vx1	Vx2	Vf
L	L	H
L	H	L
H	L	L
H	H	L

(a) Circuito (b) Tabela verdade



(c) Símbolo gráfico s

Porta com tecnologia NMOS



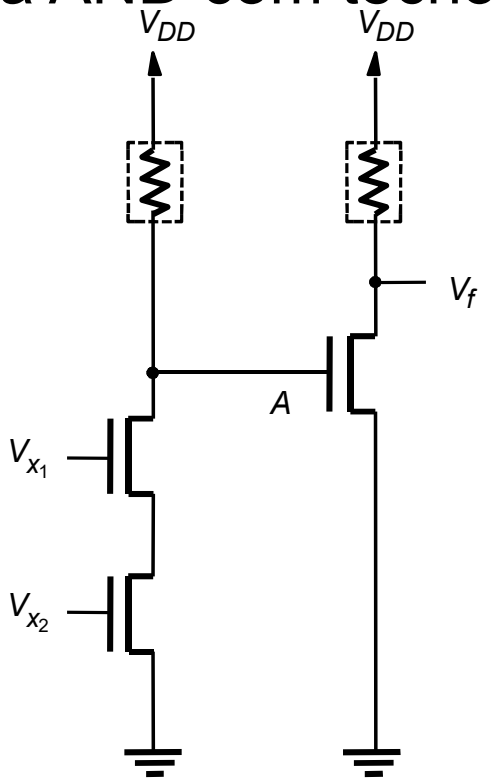
(a) Circuito

x1	x2	f
0	0	0
0	1	0
1	0	0
1	1	1

(b) Tabela Verdade

Vx1	Vx2	Vf
L	L	L
L	H	L
H	L	L
H	H	H

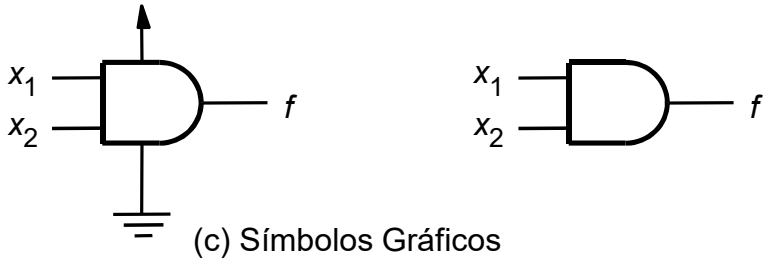
Porta AND com tecnologia NMOS



(a) Circuito

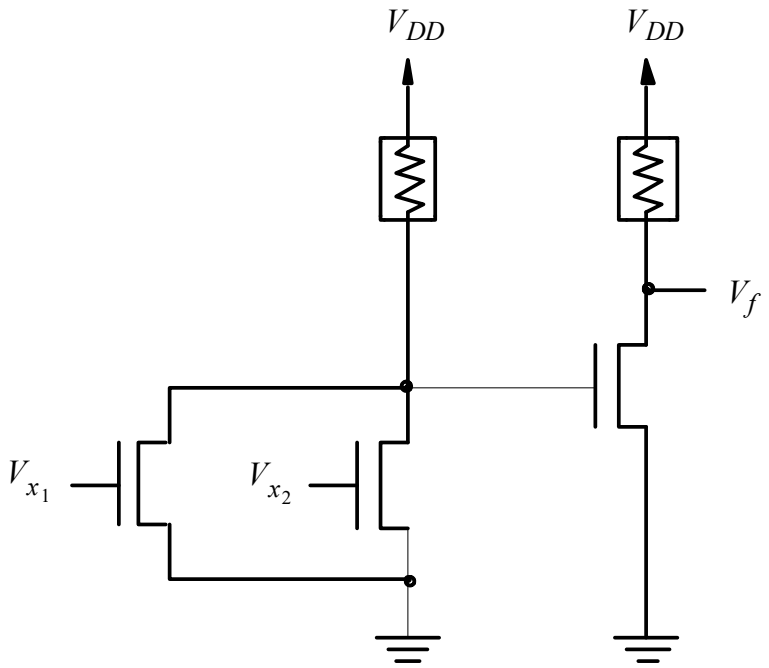
x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

(b) Tabela Verdade



(c) Símbolos Gráficos

Porta com tecnologia NMOS



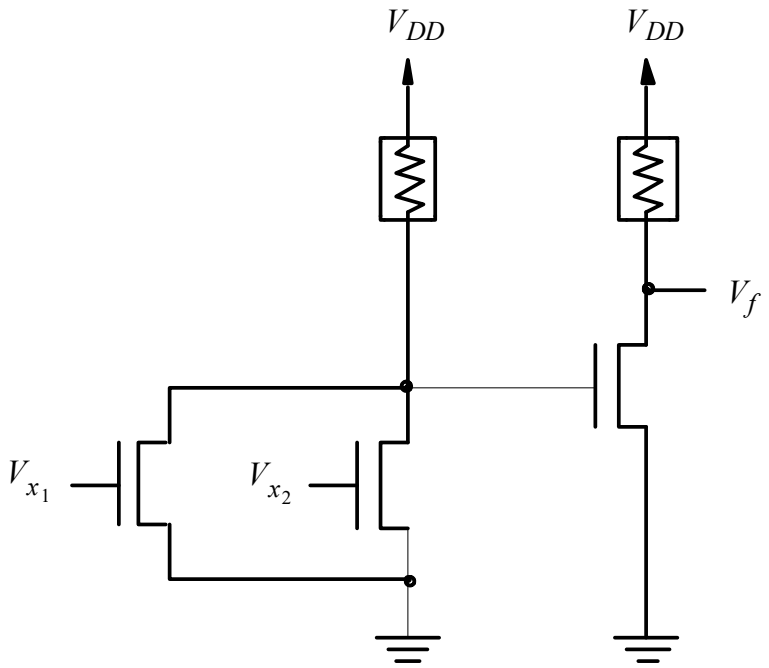
(a) Circuito

x1	x2	f
0	0	
0	1	
1	0	
1	1	

(b) Tabela Verdade

Vx1	Vx2	Vf
L	L	L
L	H	H
H	L	H
H	H	H

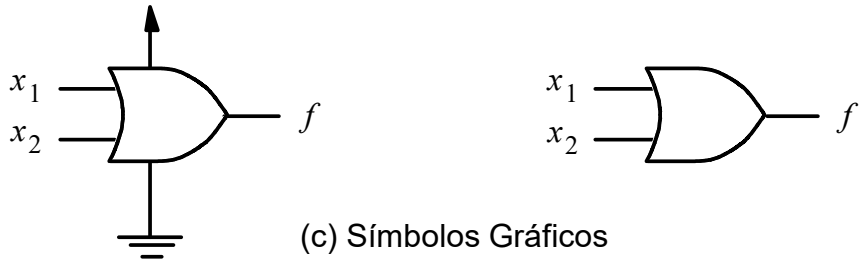
Porta OR com tecnologia NMOS



(a) Circuito

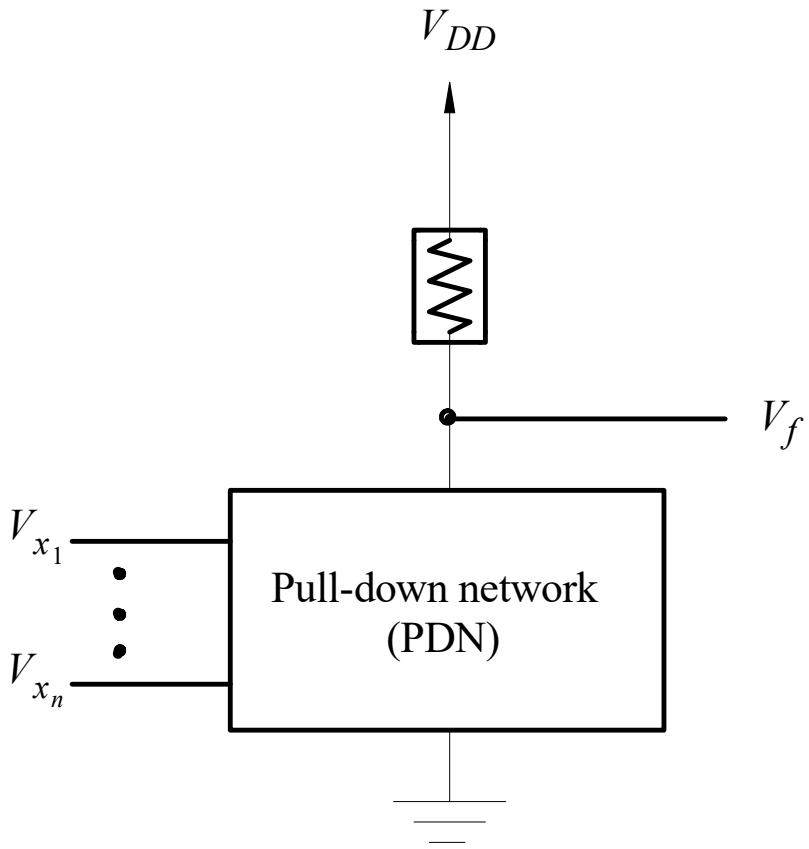
x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

(b) Tabela Verdade

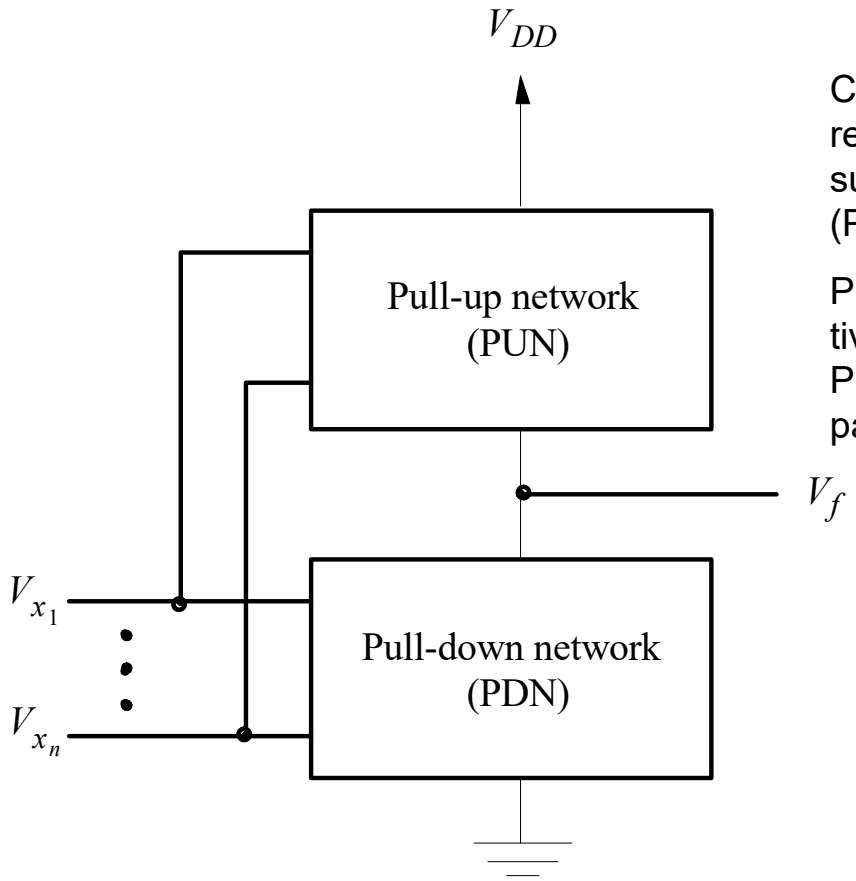


(c) Símbolos Gráficos

Estrutura de uma Porta NMOS



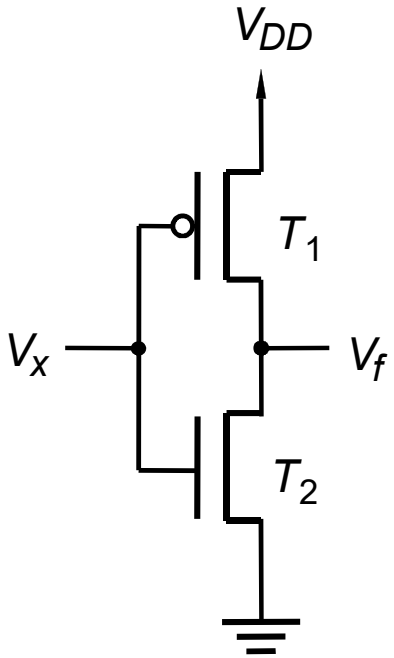
Estrutura de uma Porta CMOS



CMOS – Complementary MOS – resistor referente à porta NOMS é substituído por uma rede Pull-up (PUN)

PDN e PUN são duais, se o PDN tiver transistores NMOS em série, PUN terá transistores PMOS em paralelo, e vice-versa.

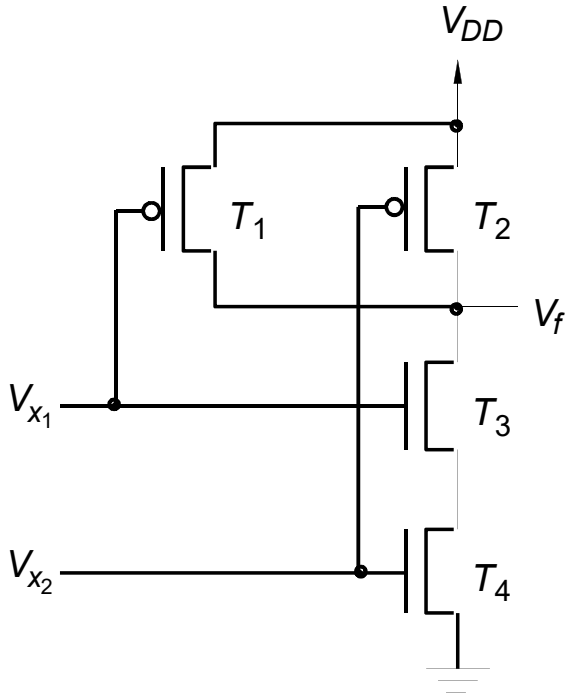
Estrutura de uma Porta NOT CMOS



x	T_1	T_2	f
0	on	off	1
1	off	on	0

(a) Circuito (b) Tabela verdade e estados dos transistores

Estrutura de uma Porta CMOS



(a) Circuit

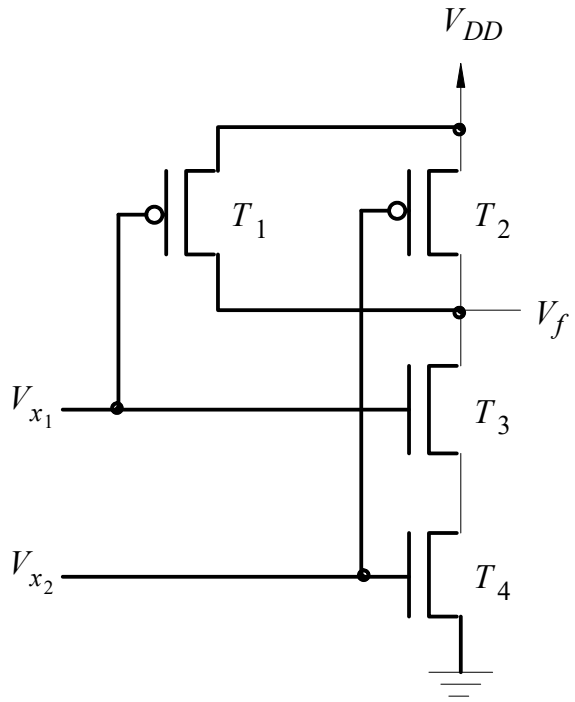
x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(b) Truth table and transistor states

Para f = 1 → $f = \overline{x1.x2} = \overline{x1} + \overline{x2}$ → PUN = 2 transistores PMOS em paralelo

Para f = 0 → $\overline{f} = x1.x2$ → PDN = 2 transistores NMOS em série

Estrutura de uma Porta NAND CMOS



(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(b) Truth table and transistor states

Para f = 1 → $f = \overline{x1x2} = \overline{x1} + \overline{x2}$ → PUN = 2 transistores PMOS em paralelo

Para f = 0 → $\overline{f} = x1x2$ → PDN = 2 transistores NMOS em série

Exercício
Dê o circuito CMOS para $f = \overline{(x1+x2)}$
PUN

PDN

Exercício

Dê o circuito CMOS para $f = \overline{(x1+x2)}$

PUN

= x1' . x2' → PUN 2 transistores PMOS em série

PDN

f' = (x1 + x2)'' = x1 + x2 → PDN 2 transistores NMOS em paralelo

$f = \overline{x1 + x2}$

PUN → $f = 1$

$f = \overline{x1 + x2} =$

$f = x1' \cdot x2'$

Será formado por 2 transistores PMOS estarão em série

PDN dual do PUN → será formado por 2 transistores NMOS em paralelo

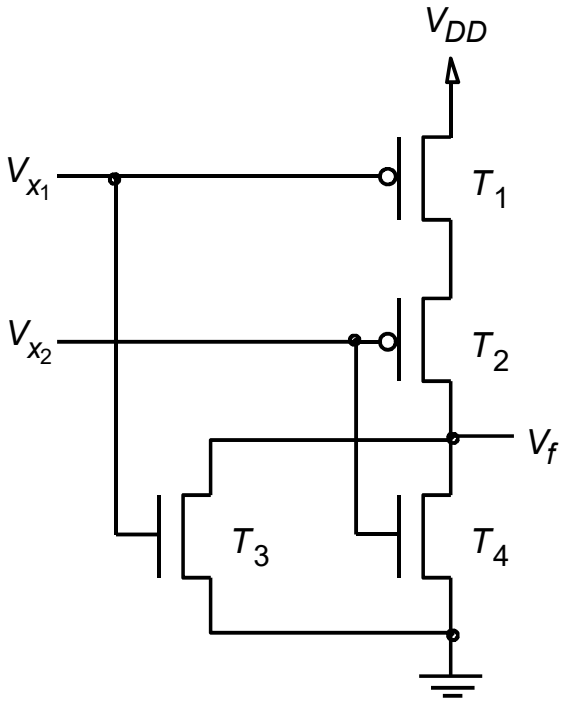
PDN → $f = 0$

$f = \overline{x1 + x2} = x1 + x2$

Será formado por dois transistores NMOS em paralelo

PUN dual do PDN → será formado por 2 transistores PMOS em série

Estrutura de uma Porta CMOS



(a) Circuit

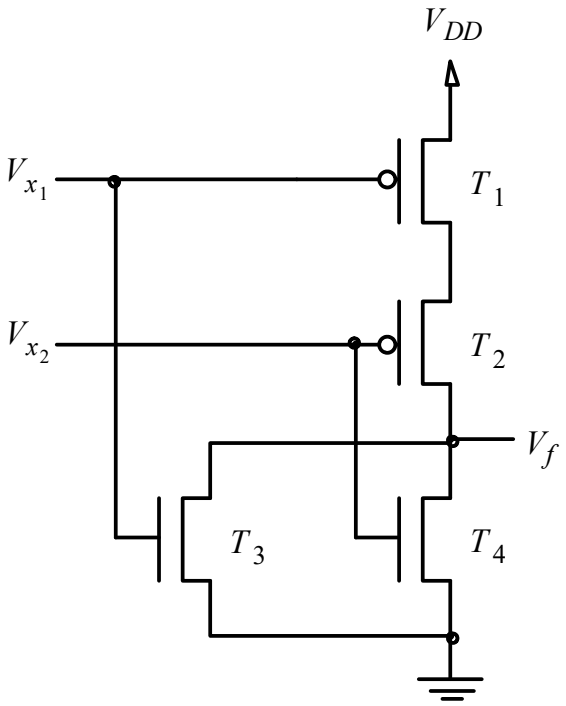
x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	
0	1	on	off	off	on	
1	0	off	on	on	off	
1	1	off	off	on	on	

(b) Truth table and transistor states

Para f = 1 → $f = \overline{x1 + x2} = \overline{x1} \cdot \overline{x2}$ → PUN = 2 transistores PMOS em série

Para f = 0 → $\overline{f} = x1 + x2$ → PDN = 2 transistores NMOS em paralelo

Estrutura de uma Porta NOR CMOS



(a) Circuit

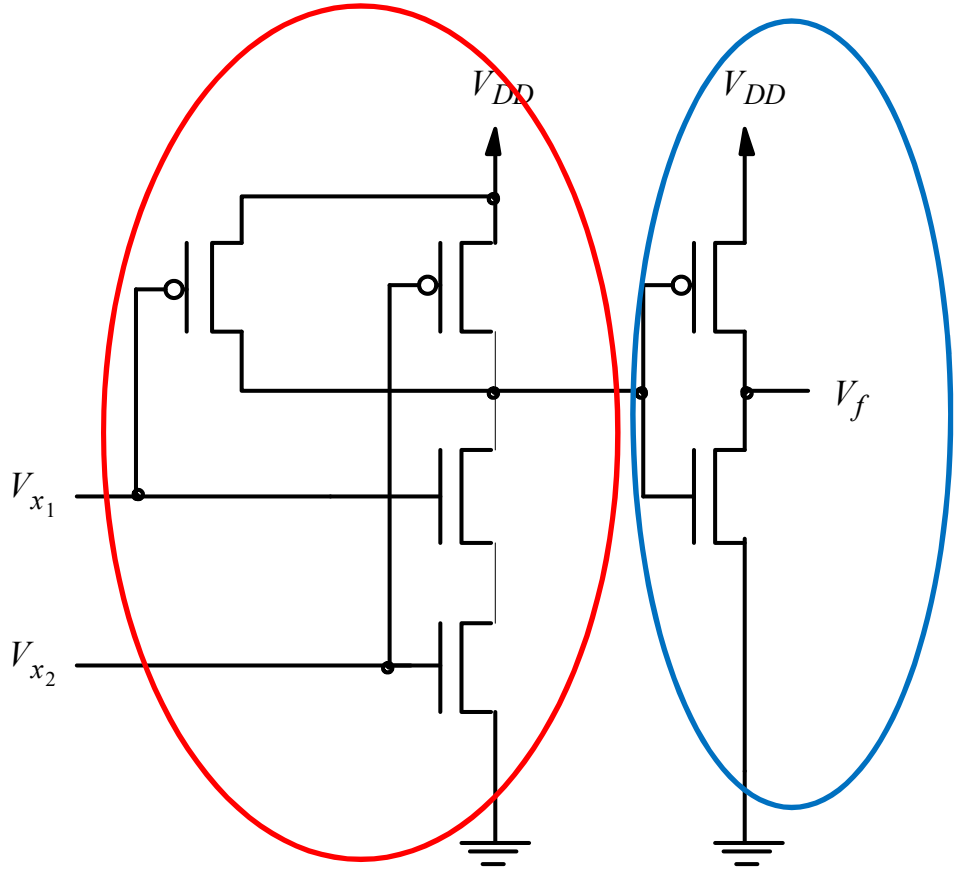
x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

(b) Truth table and transistor states

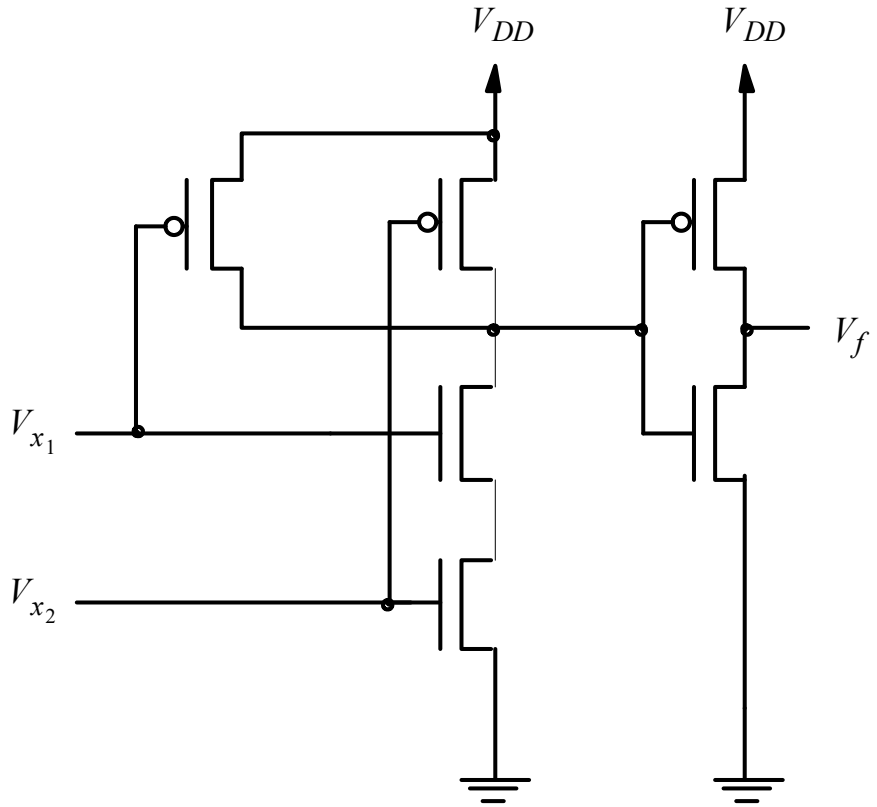
Para f = 1 → $f = \overline{x1 + x2} = \overline{x1} \cdot \overline{x2}$ → PUN = 2 transistores PMOS em série

Para f = 0 → $\overline{f} = x1 + x2$ → PDN = 2 transistores NMOS em paralelo

Estrutura de uma Porta CMOS



Estrutura de uma Porta AND CMOS



NAND + NOT

Estrutura de uma Porta CMOS

Exercício 1

Considere a função: $f = \overline{x1} + \overline{x2}\ \overline{x3}$

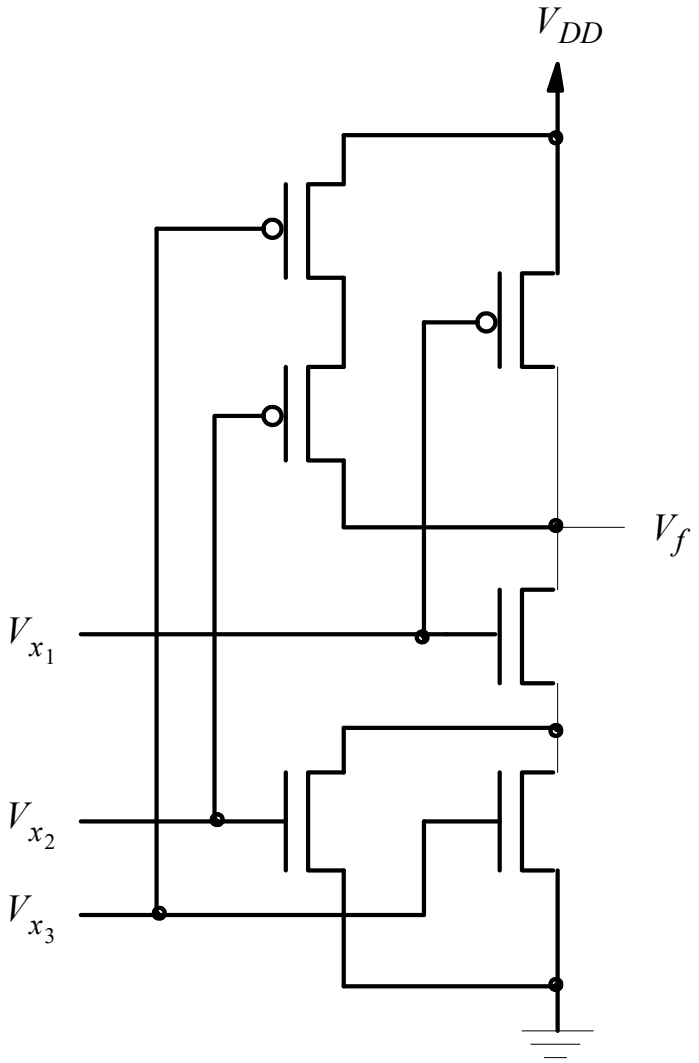
Ache o circuito CMOS equivalente com o menor número de transistores possíveis

Exercício 2

Considere a função: $f = \overline{x1} + (\overline{x2} + \overline{x3})\ \overline{x4}$

Ache o circuito CMOS equivalente com o menor número de transistores possíveis

Estrutura de uma Porta CMOS – Exercício 1



PUN

f = x1' + x2' x3'

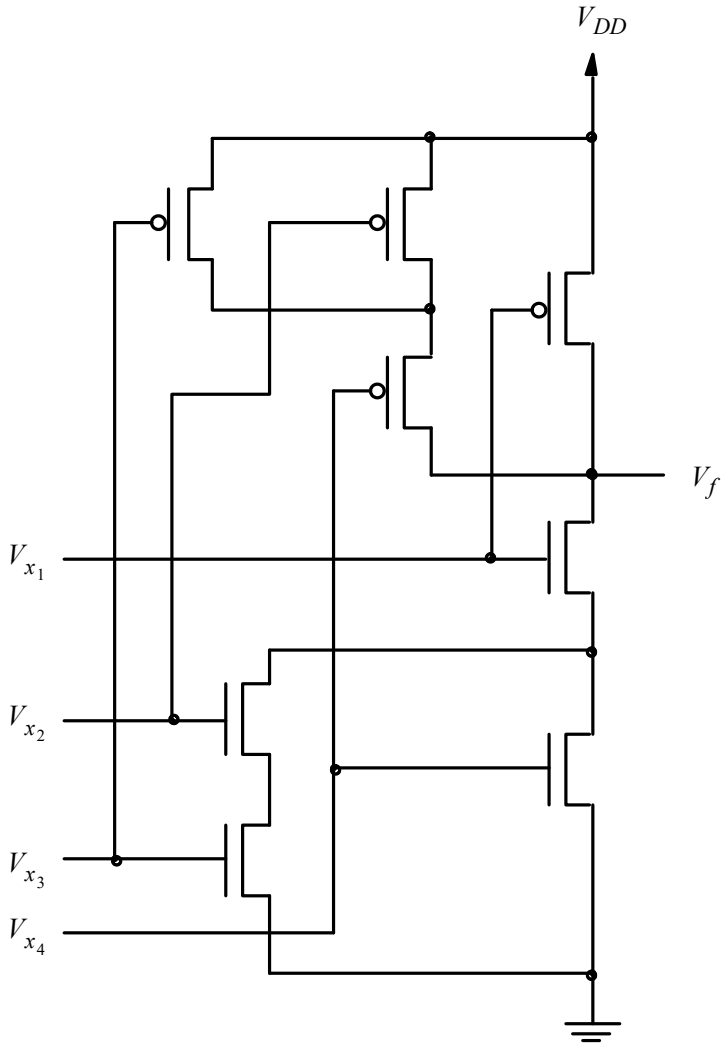
PDN

$\overline{f} = \overline{\overline{x1} + \overline{x2}\ \overline{x3}} = x1\ (x2 + x3)$

$f' = \overline{x1' + x2' x3'} = x1'' \cdot \overline{x2'x3'} =$

$= x1 \cdot (x2'' + x3'') = x1 \cdot (x2 + x3)$

Estrutura de uma Porta CMOS – Exercício 2



PUN

f = x'1 + (x'2 + x'3) x'4

PDN

f = x'1 + (x'2 + x'3) . x'4

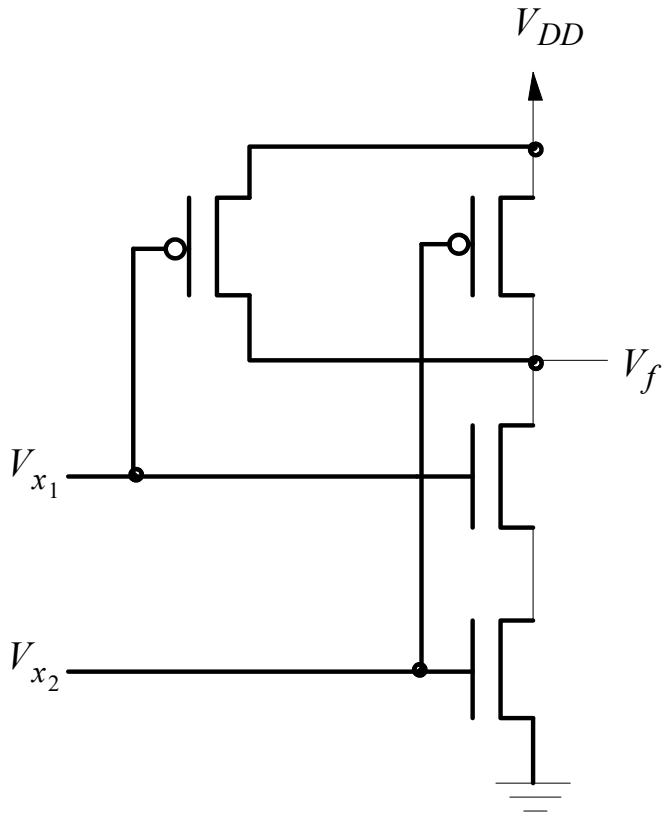
f' = (x'1 + (x'2 + x'3) x'4)' =

f' = x''1 . (x'2 + x'3) x'4)' =

= x1 . ((x'2+x'3)' + x''4) =

= x1 . ((x2 . x3) + x4)

Níveis de Tensão em uma Porta Lógica



(a) Circuit

V_{x_1}	V_{x_2}	V_f
L	L	H
L	H	H
H	L	H
H	H	L

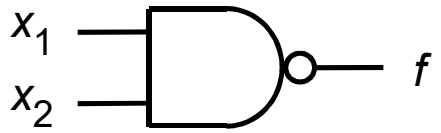
(b) Voltage levels

Interpretação dos Níveis de Tensão – Lógica Positiva e Negativa

V_{x_1}	V_{x_2}	V_f
L	L	H
L	H	H
H	L	H
H	H	L

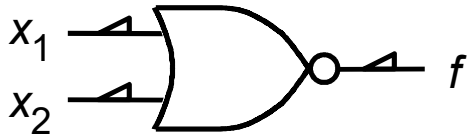
(a) Níveis de Tensão

x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0



(b) Tabela Verdade – Lógica Positiva e Símbolo

x_1	x_2	f
1	1	0
1	0	0
0	1	0
0	0	1



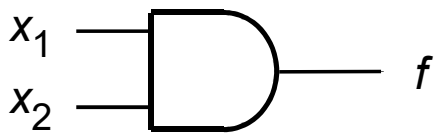
(c) Tabela Verdade – Lógica Negativa e Símbolo

Interpretação dos Níveis de Tensão – Lógica Positiva e Negativa

V_{x_1}	V_{x_2}	V_f
L	L	L
L	H	L
H	L	L
H	H	H

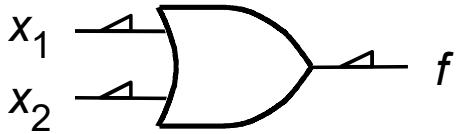
(a) Níveis de Tensão

x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1



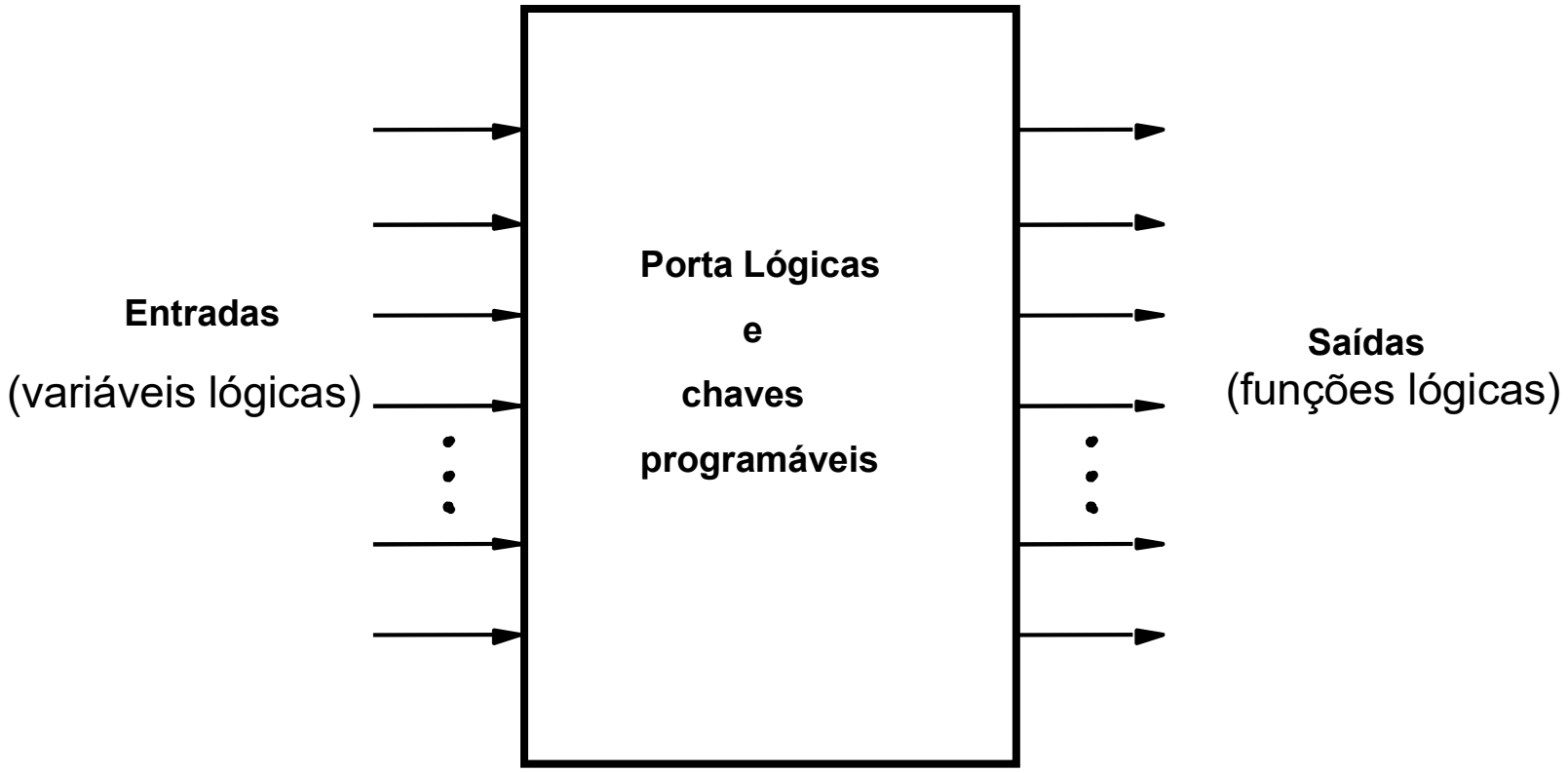
(b) Lógica Positiva

x_1	x_2	f
1	1	1
1	0	1
0	1	1
0	0	0

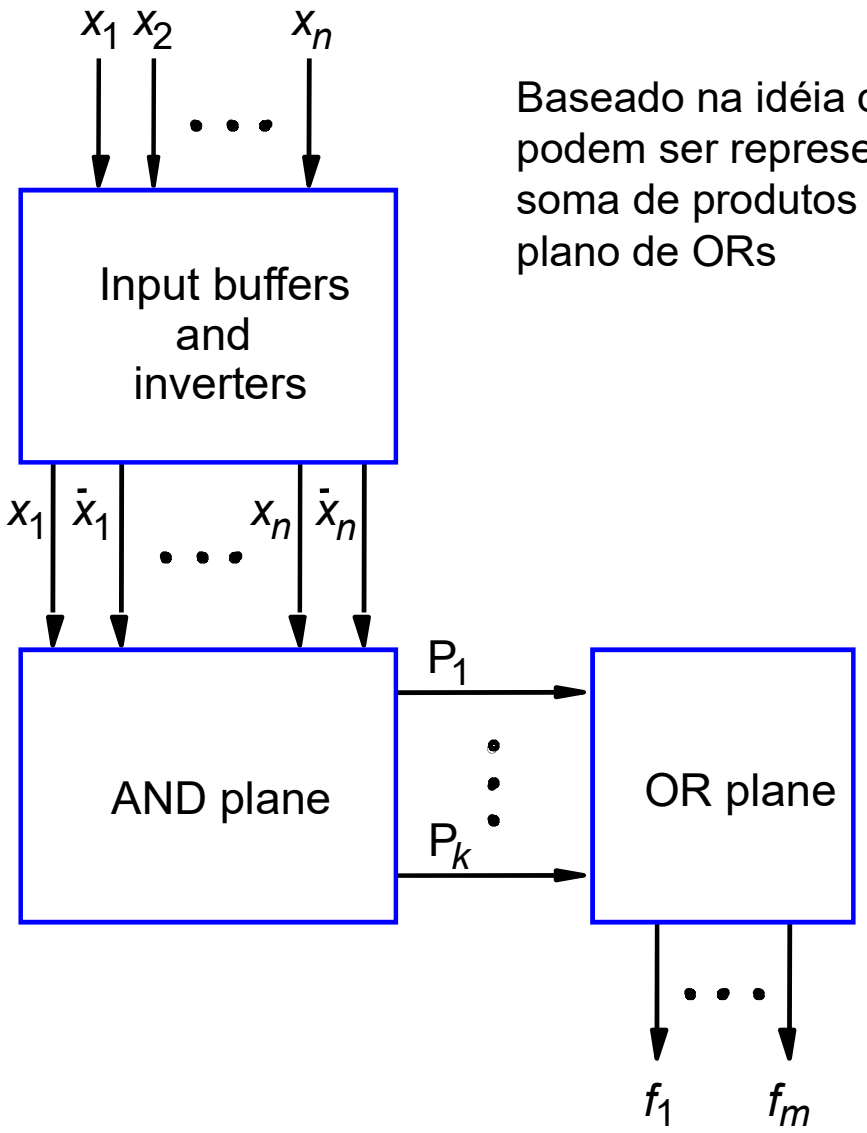


(c) Lógica Negativa

Dispositivos Lógicos Programáveis como uma Caixa Preta

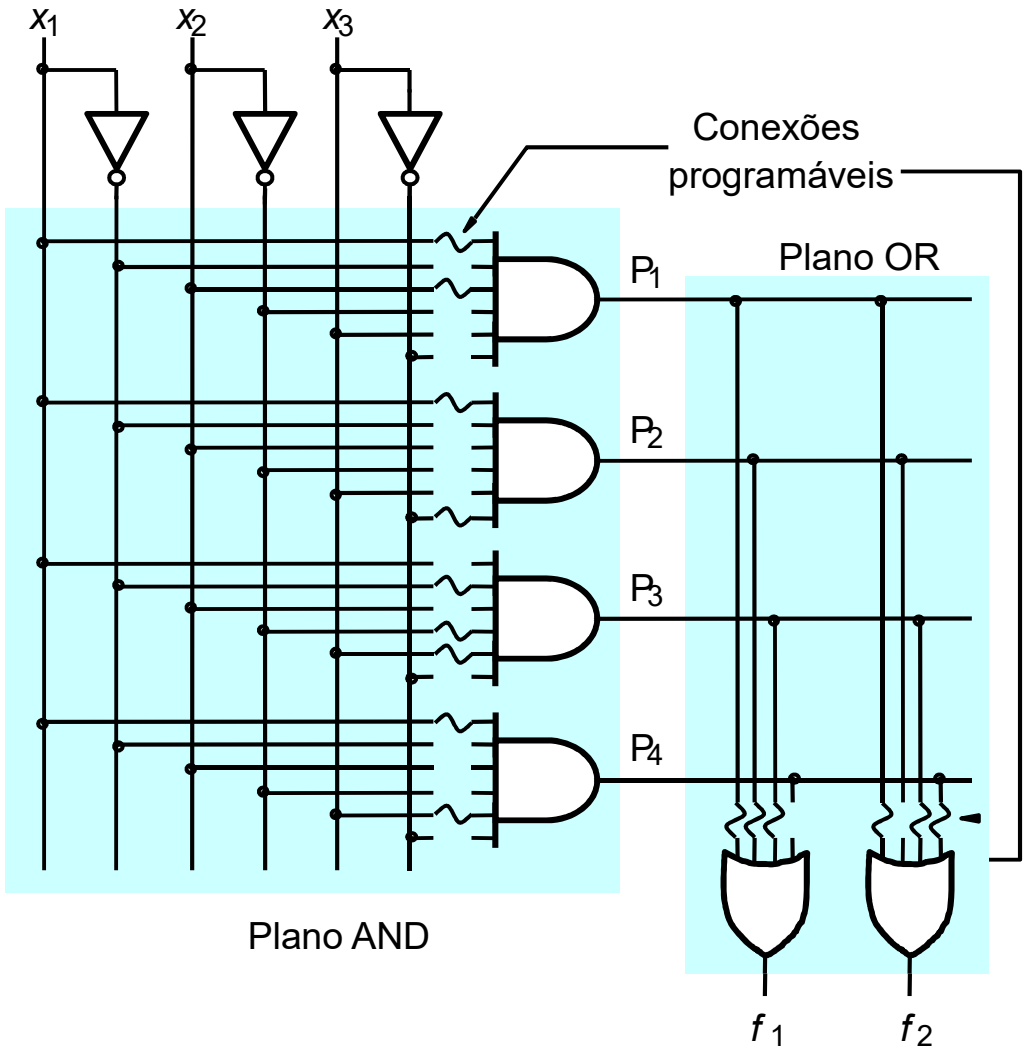


Estrutura geral de uma PLA – Programmable Logic Array



Baseado na idéia que as funções lógicas podem ser representadas como uma soma de produtos → plano de ANDs e plano de ORs

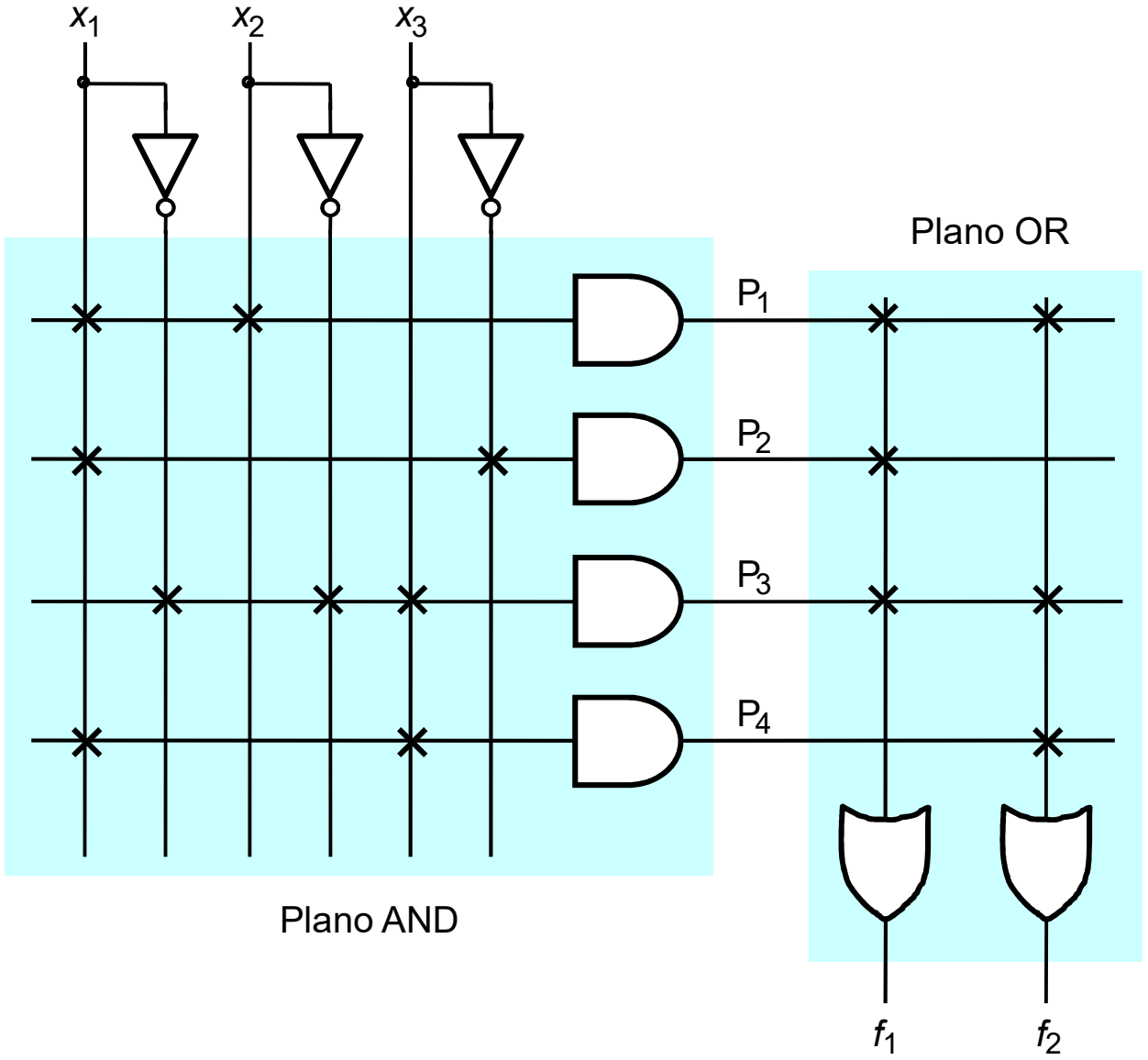
Diagrama, em nível de portas lógicas, de uma PLA



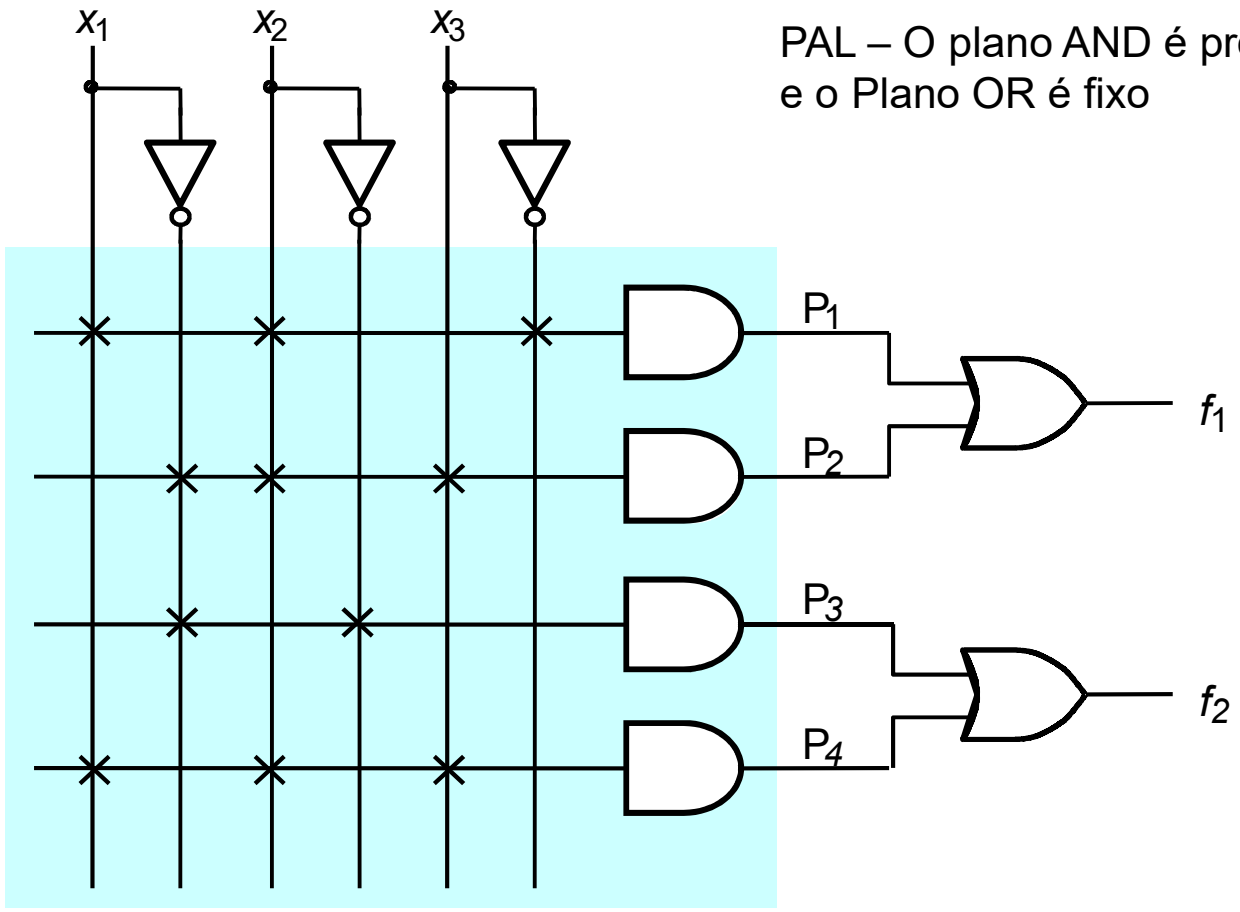
P1 = x1 . x2
P2 = x1 . x'3
P3 = x'1 . x'2 . x3
P4 = x1 . x3
f1 = P1 + P2 + P3
f2 = P1 + P3 + P4

Exercício – Dizer quais são as respectivas funções f1 e f2.

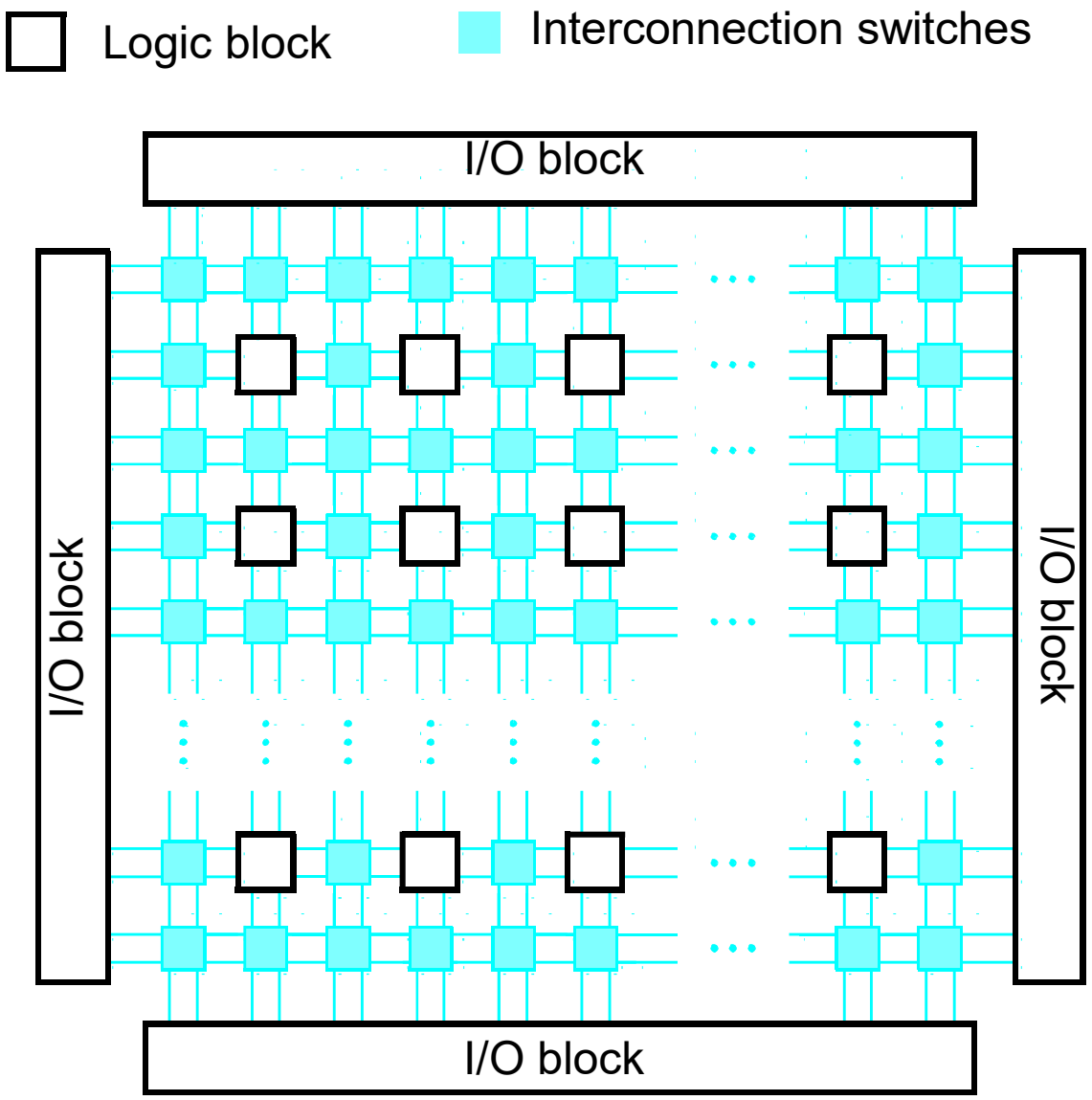
Desenho esquemático de uma PLA



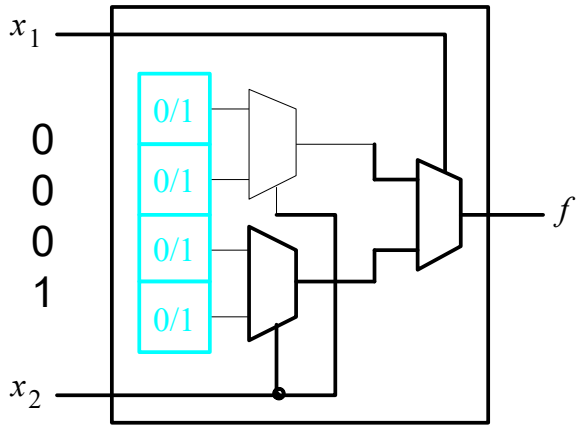
Exemplo de uma PAL – Programmable Array Logic



Estrutura de uma FPGA – Field Programmable Gate Array



FPGA - lookup table (LUT) de duas entradas



(a) Circuit for a two-input LUT

AND
f = x1 . x2

x1	x2	f
0	0	0
0	1	0
1	0	0
1	1	1

LUT → contém células que armazenam, São usadas para implementar uma função lógica

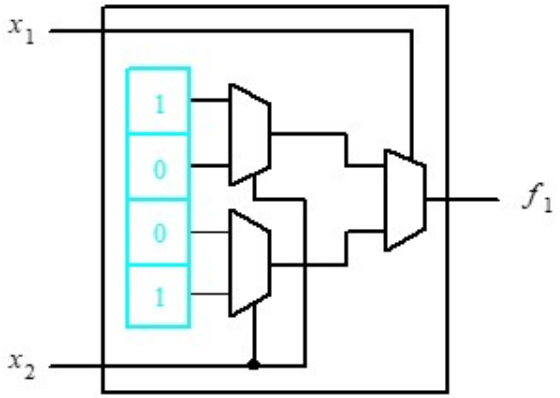
MUX 2:1

f (S, x1, x2) → Se S = 0 → f = x1, c.c. f = x2

F = S’ x1 + S x2

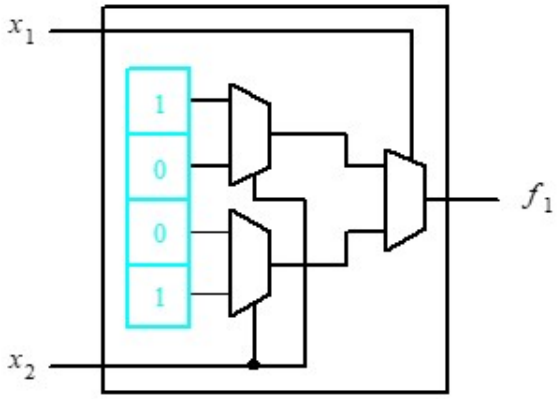
FPGA - lookup table (LUT) de duas entradas

Que função é esta ?
O que seria armazenado na LUT para executar esta função?



FPGA - lookup table (LUT) de duas entradas

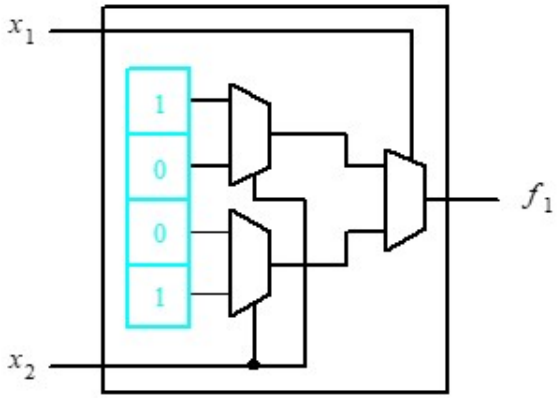
Que função é esta ?
O que seria armazenado na LUT para executar esta função?



x1	x2	f1
0	0	1
0	1	0
1	0	0
1	1	1

FPGA - lookup table (LUT) de duas entradas

Que função é esta ?

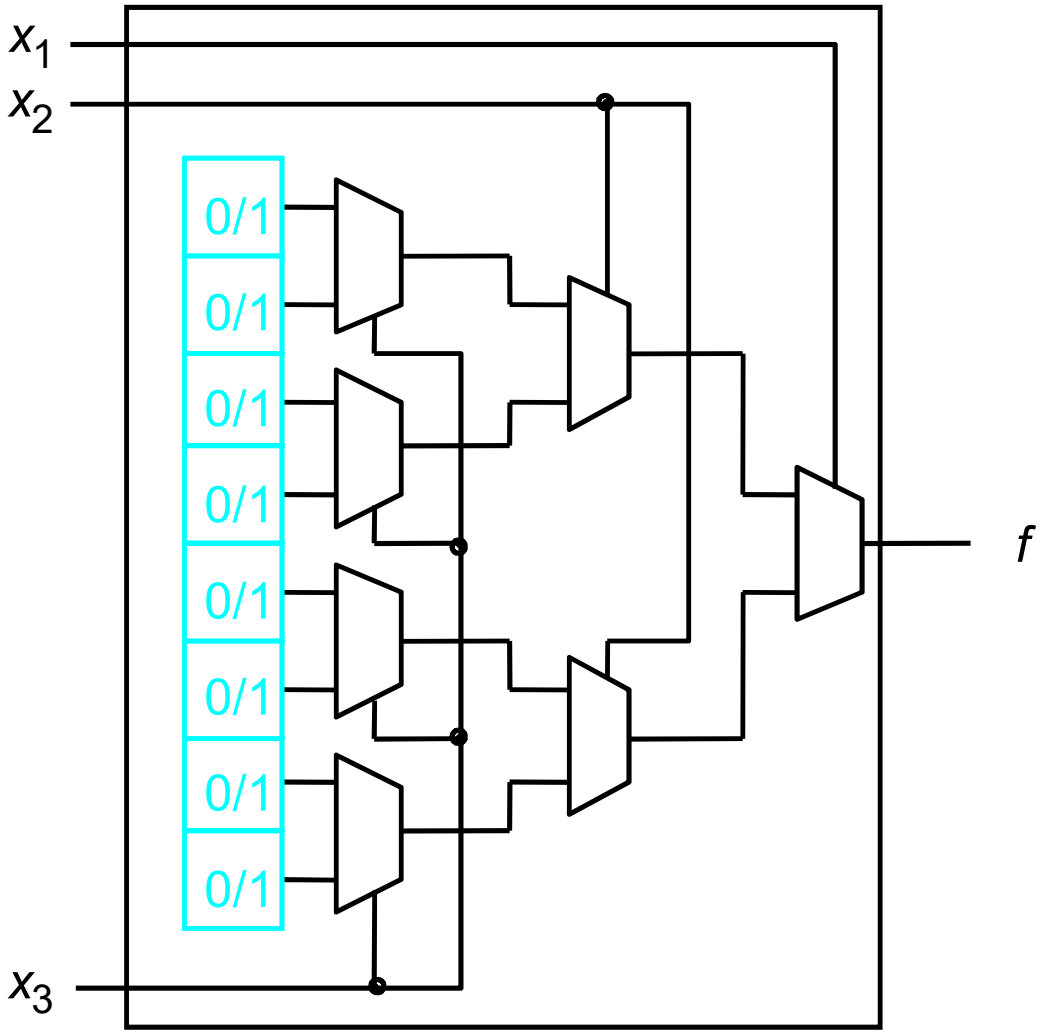


x1	x2	f1
0	0	1
0	1	0
1	0	0
1	1	1

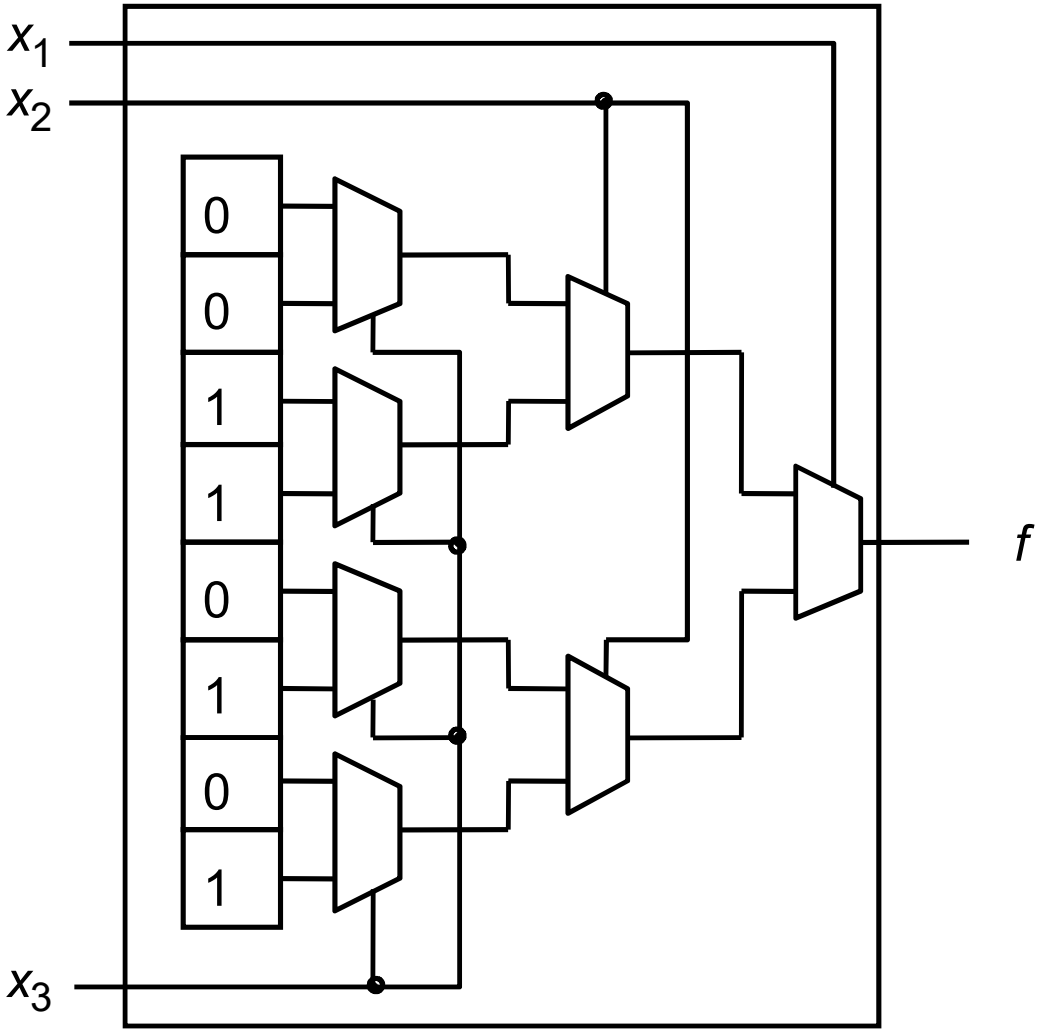
f1 = x1’ x2’ + x1 x2

XNOR

FPGA - lookup table (LUT) de três entradas



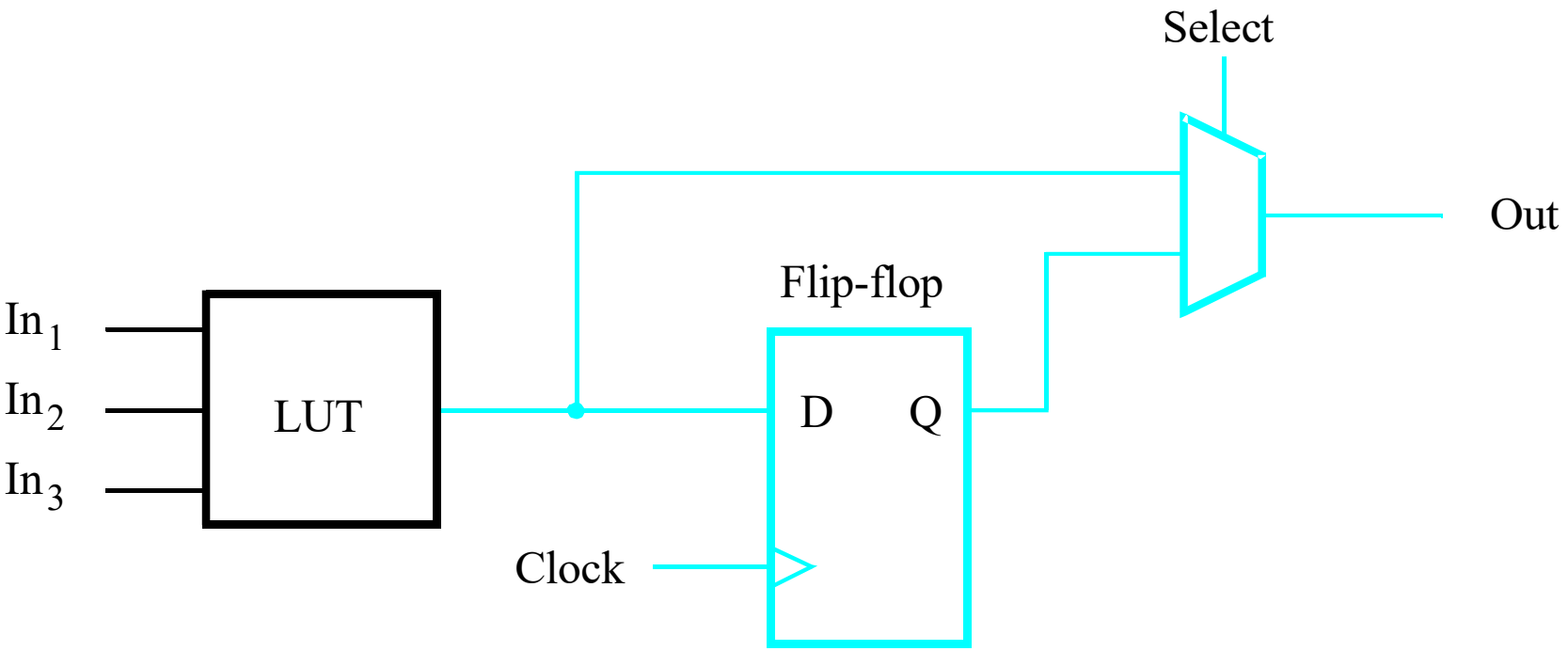
FPGA - lookup table (LUT) de três entradas



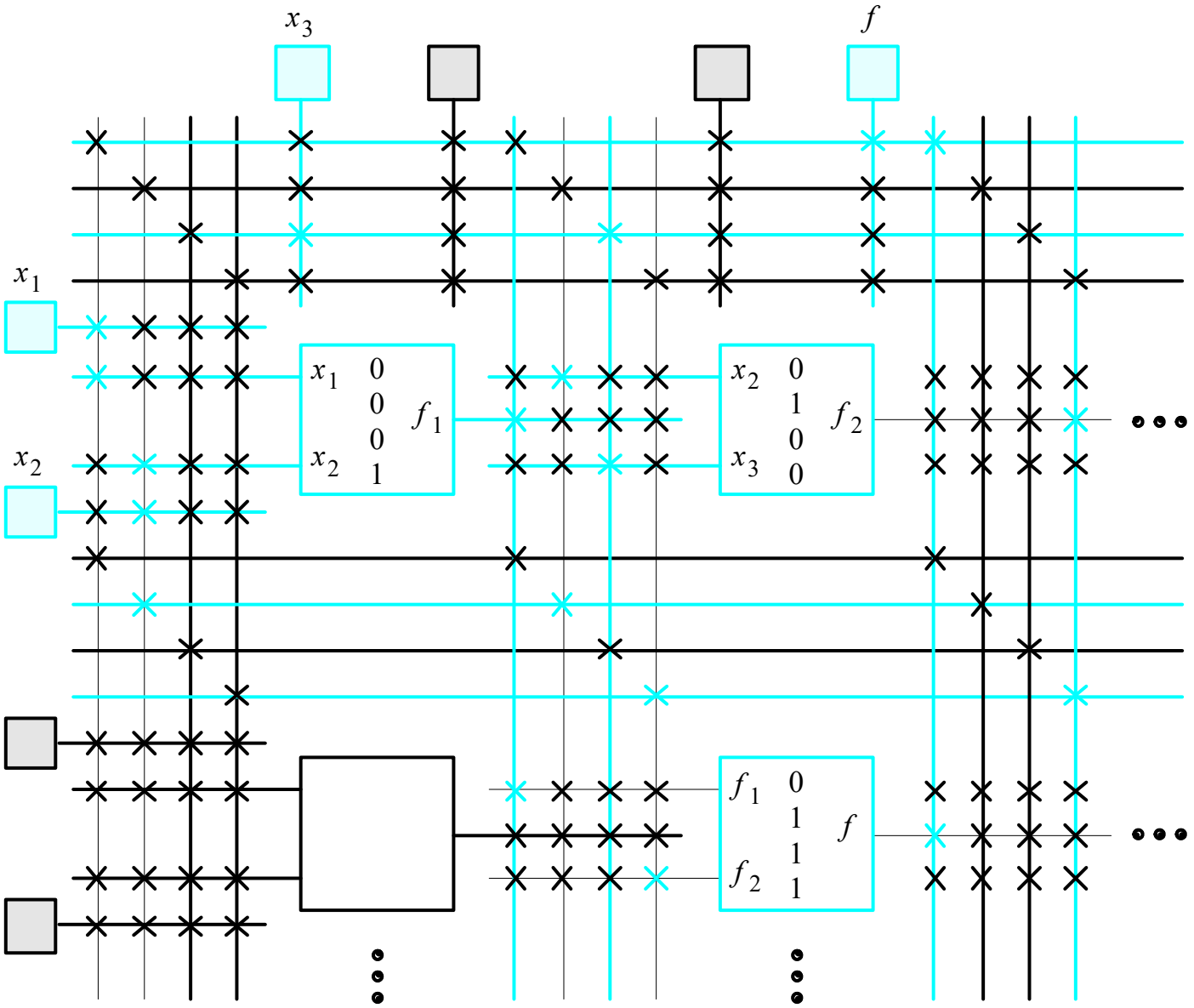
x1	x2	x3	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

f = x1’x2x3’+x1’x2x3+x1x2’x3
= x1’x2 + x1x2’x3

FPGA - lookup table (LUT) + Flip Flop



FPGA Programada



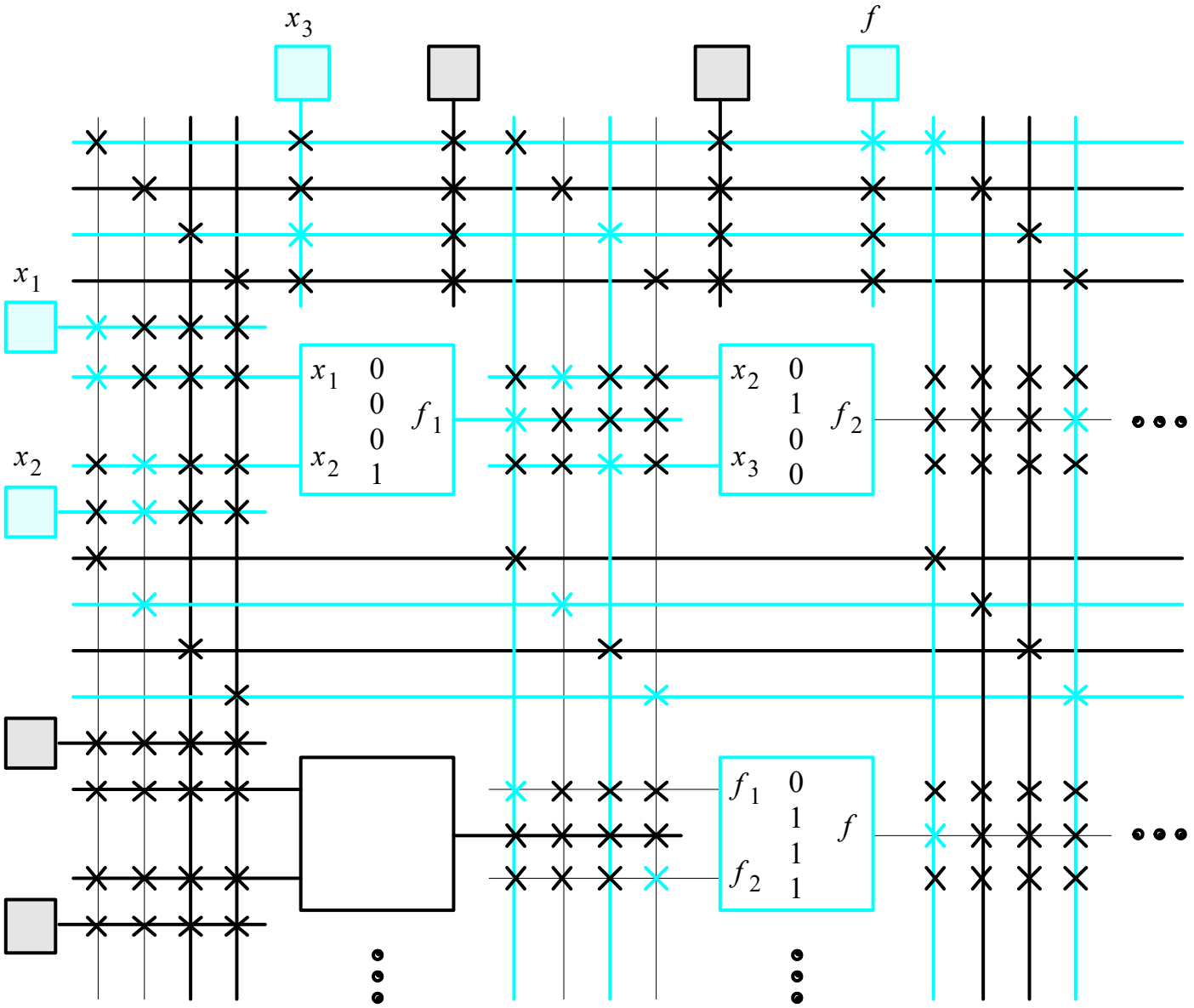
Exercício: Dê as funções f, f1 e f2

f1 =

f2 =

f =

FPGA Programada



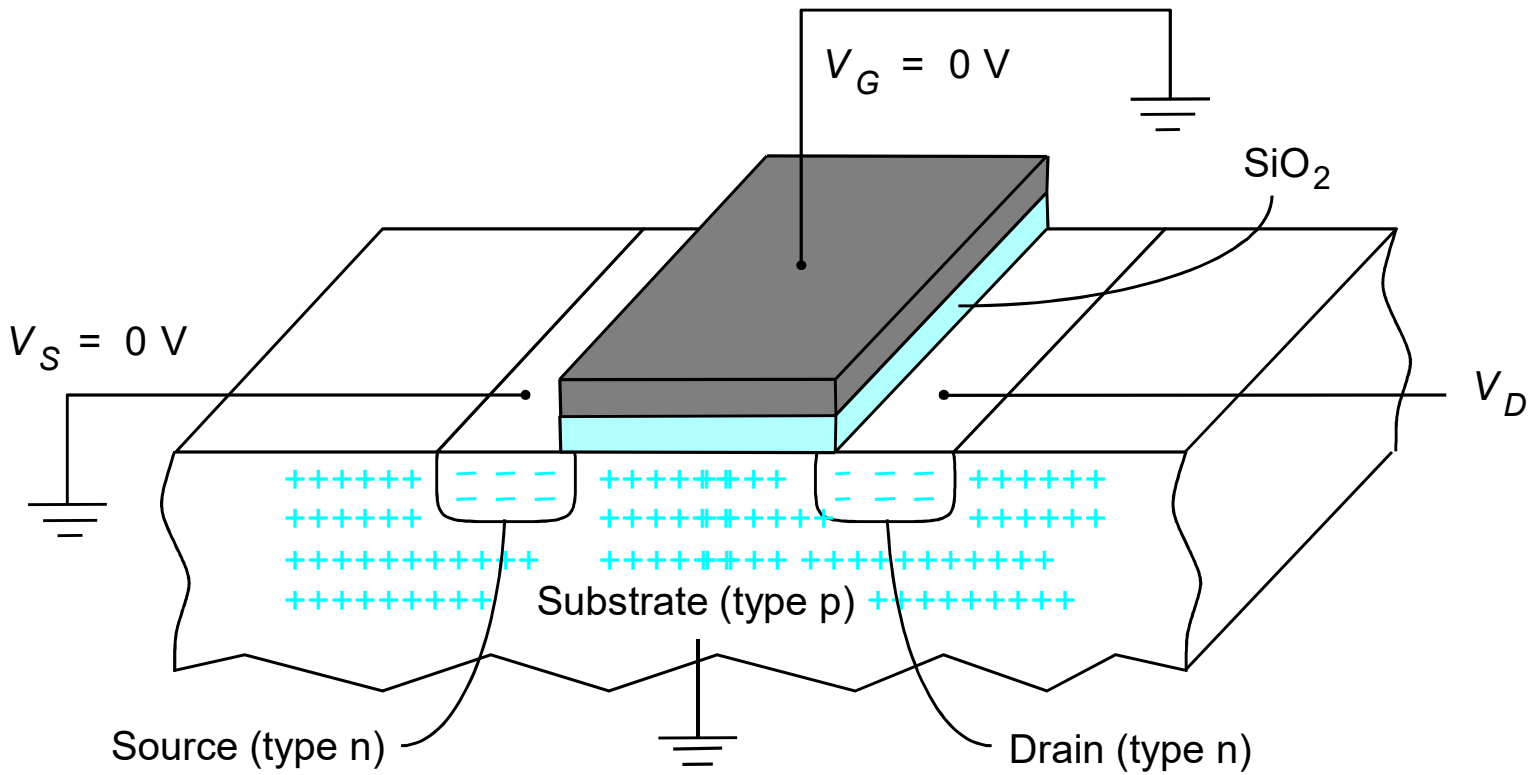
Exercício: Dê as funções f, f1 e f2

f1 = x1 . x2

f2 = x2' .x3

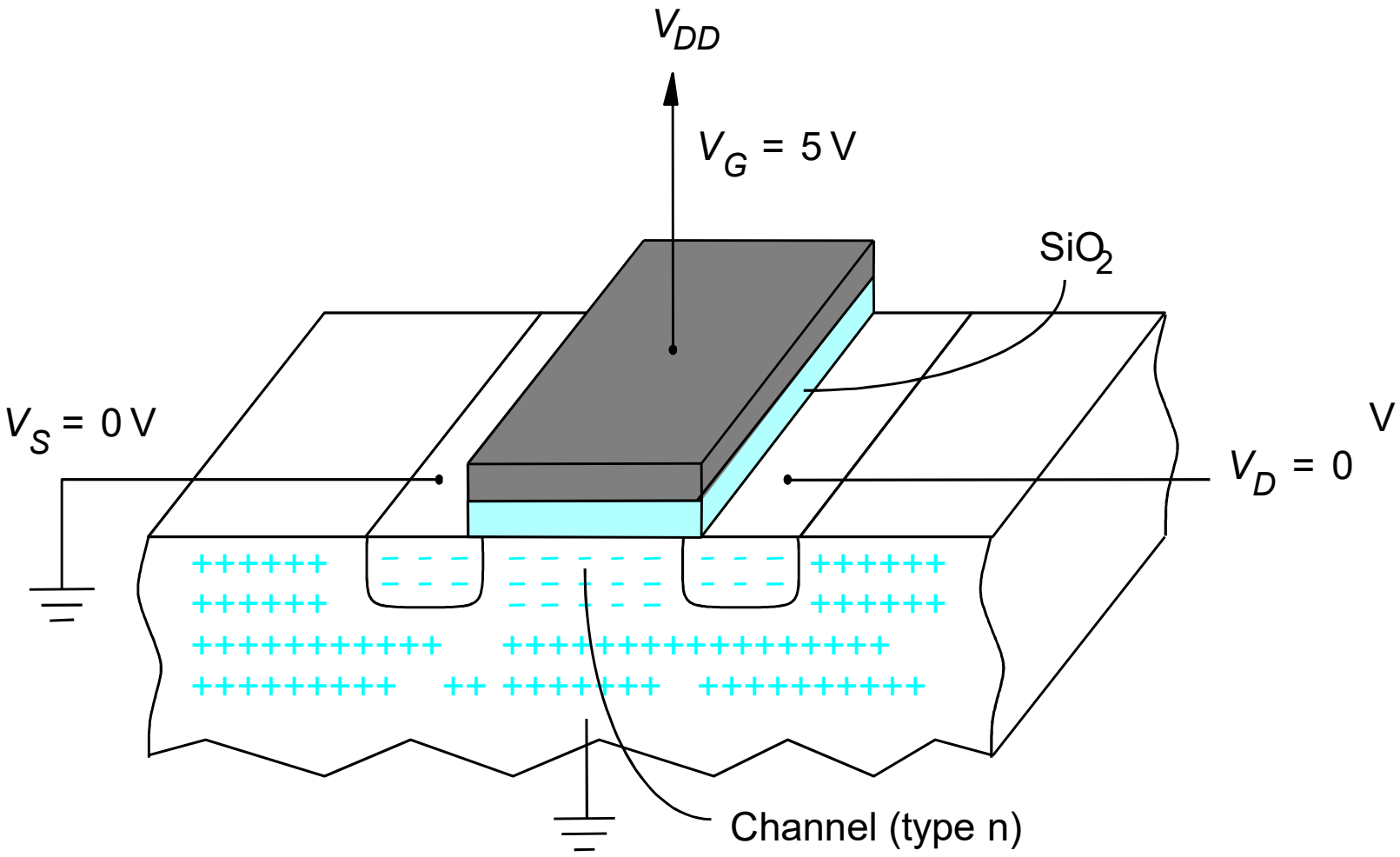
f = (x1x2+x2'x3)

Comportamento de um transistor MOS - NMOS



(a) Quando V_{GS} = 0 V, o transistor está off

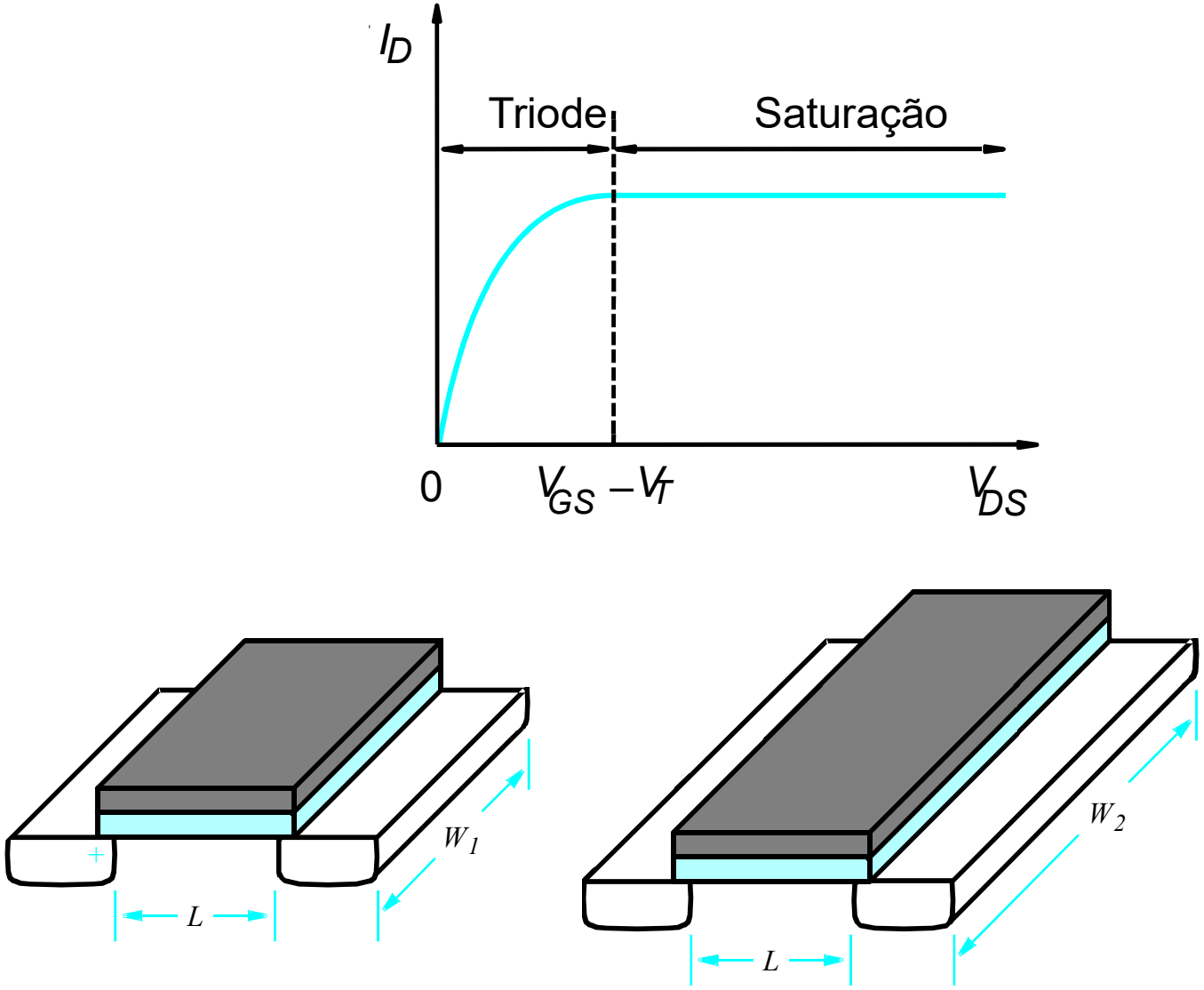
Comportamento de um transistor MOS - NMOS



(b) Quando V_{GS} = 5 V, o transistor está on

$V_{GS} > V_T \rightarrow$ há a formação do canal

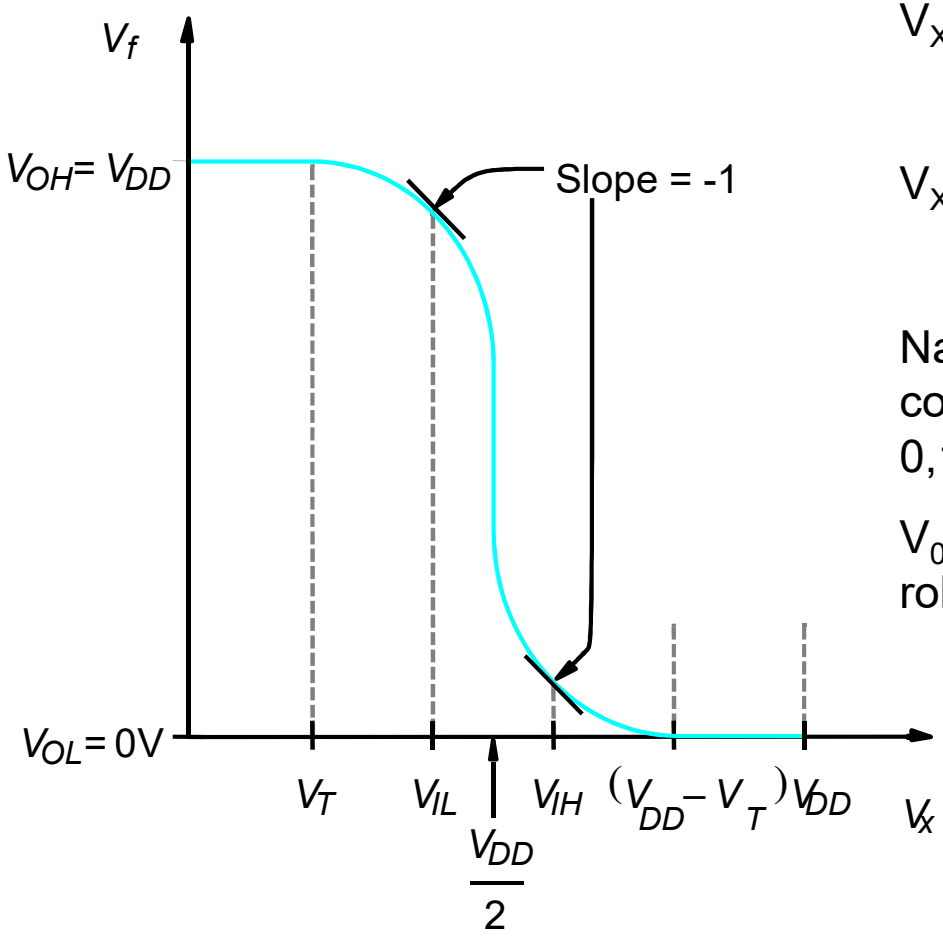
Relação tensão-corrente em um transistor NMOS



(a) Small transistor

(b) Larger transistor

Curva de transferência de um inversor CMOS



$V_X = 0$ → NMOS off

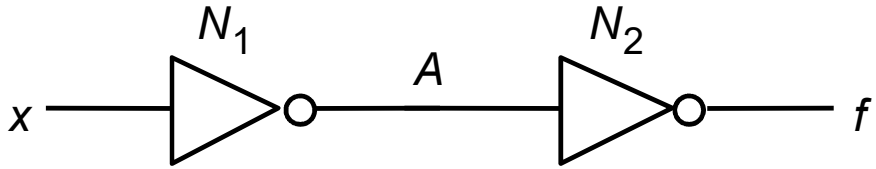
$V_X = V_{DD}$ → PMOS off

} Sem fluxo de corrente

Na realidade existe uma pequena corrente → leakage current → V_{0L} = 0,1 mV

V_{0L}, V_{1L}, V_{0H} e V_{1H} → quantifica a robustez de uma família lógica

Margem de Ruído



Dois inversores em cascata

Ruído → perturbações randômicas que podem alterar um sinal.

Por exemplo, a saída de N1 pode ser alterada por uma perturbação externa (ruído).

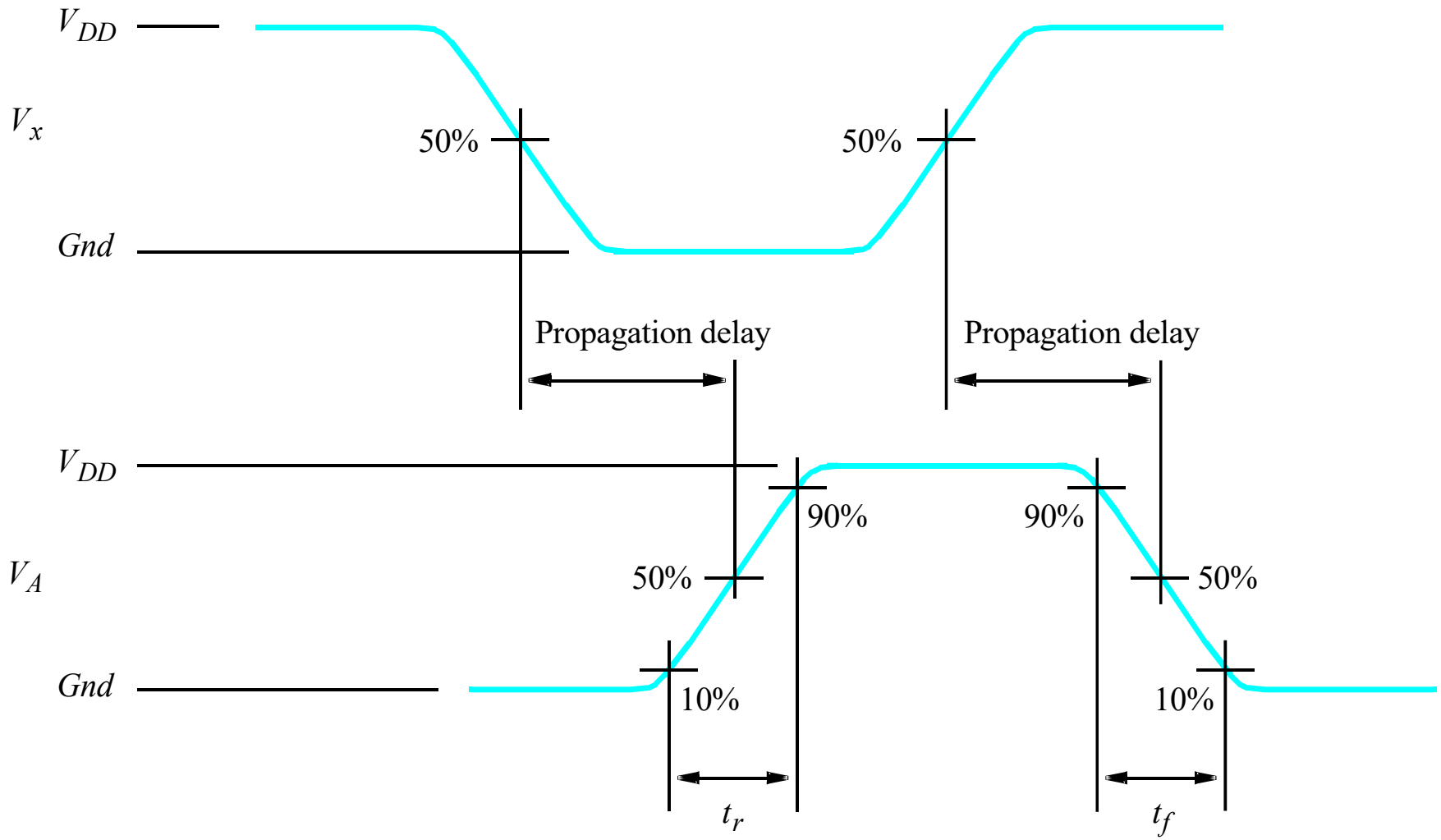
Se este ruído alterar V_{1L} de N1, este nível deve se manter abaixo de V_{1L}, para ser interpretado corretamente por N2.

A capacidade para tolerar ruídos sem afetar a operação correta → margem de ruído

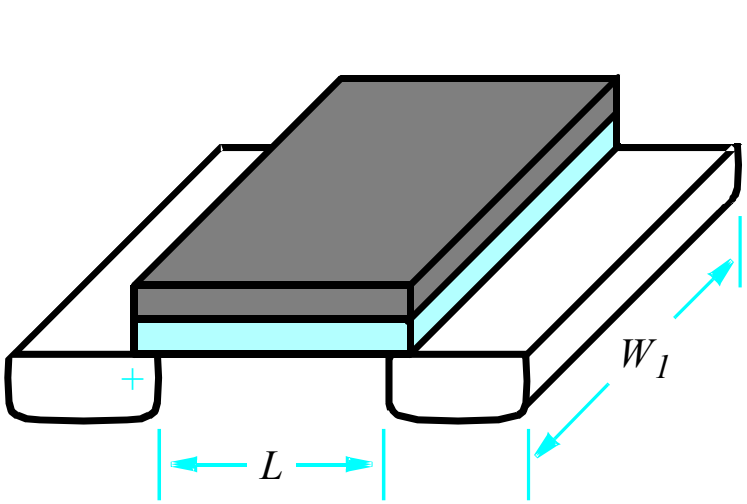
$$NM_L = V_{1L} - V_{0L}$$

$$NM_H = V_{0H} - V_{1H}$$

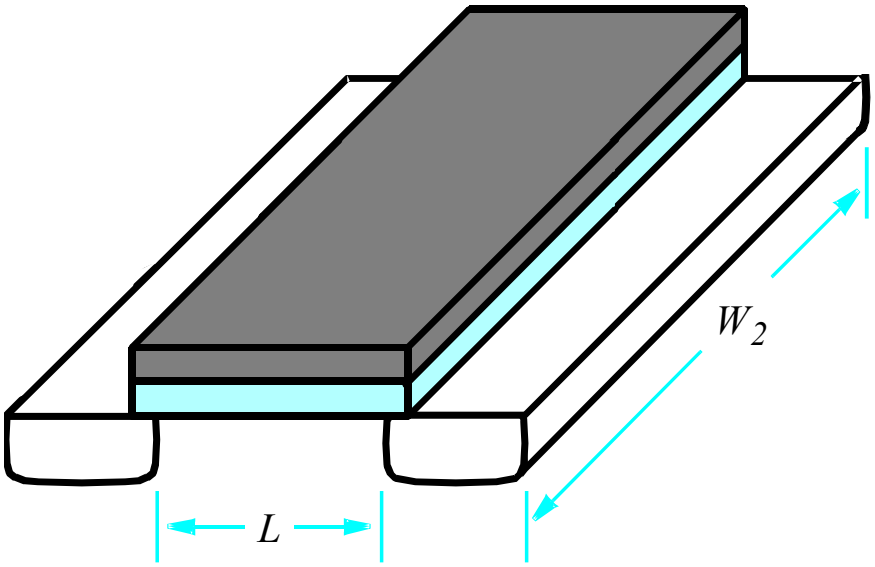
Figure 3.48 Voltage waveforms for logic gates



Dimensões de transistores

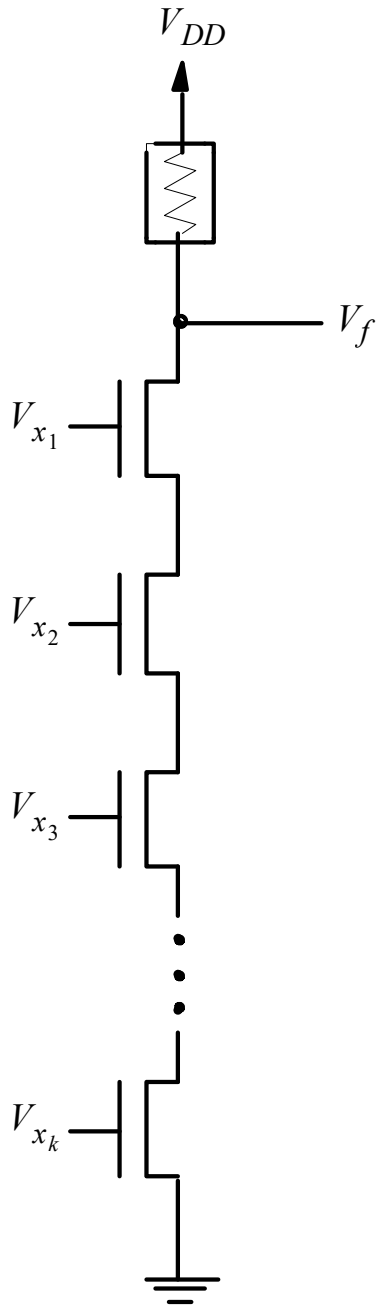


(a) Small transistor

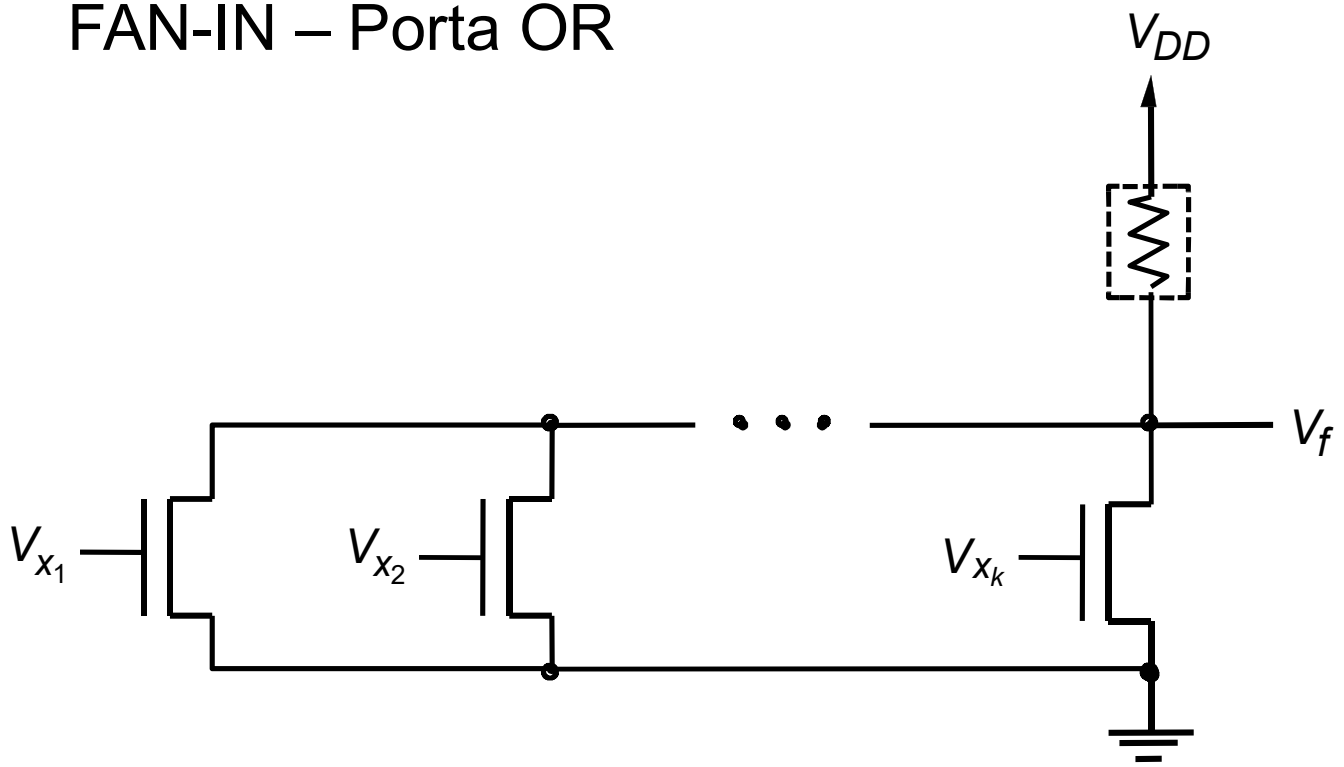


(b) Larger transistor

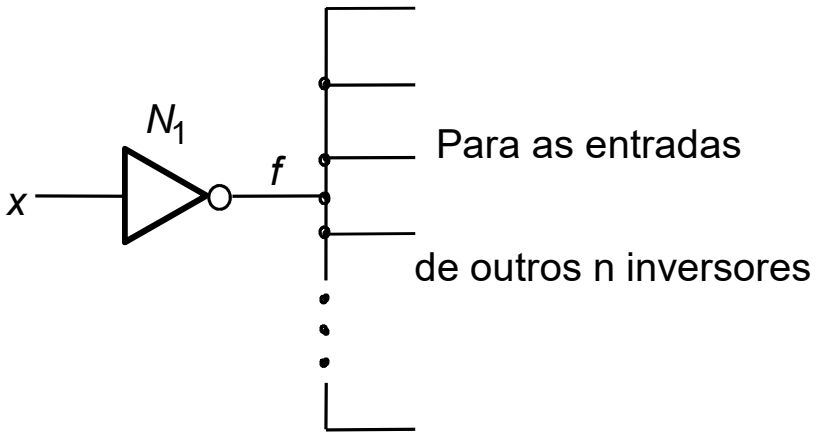
FAN-IN – Porta AND



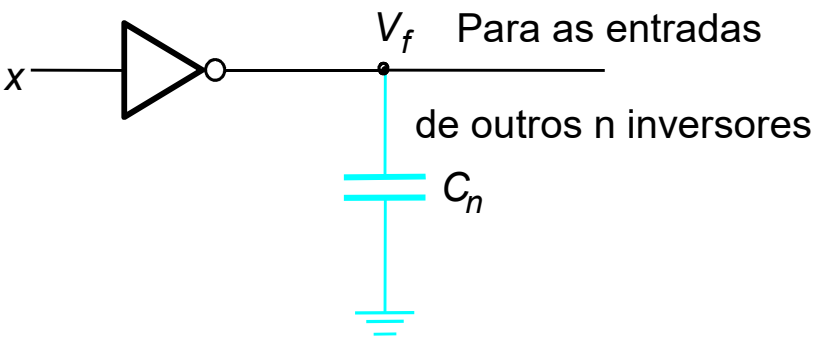
FAN-IN – Porta OR



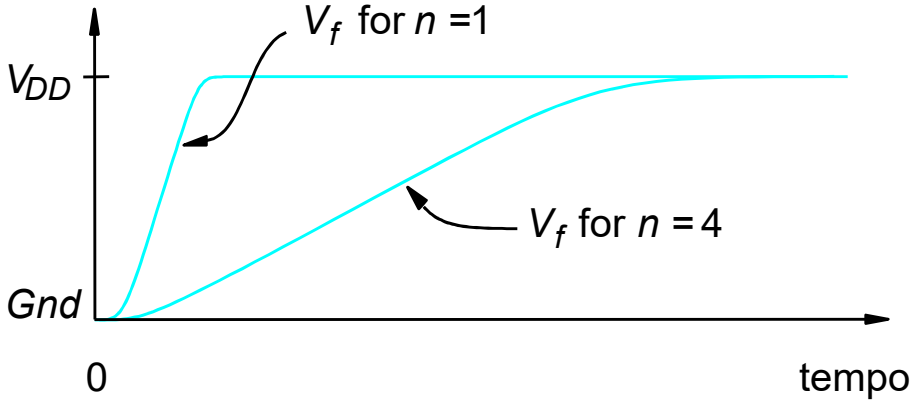
O efeito do fan-out na propagação de atrasos



(a) Inversor que drives outros n inversores

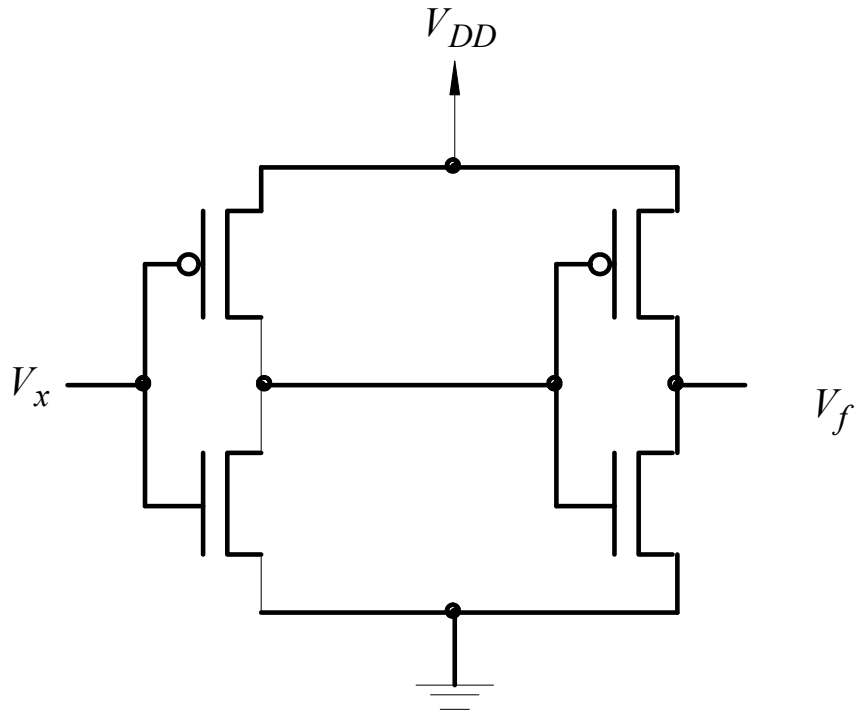


(b) Circuito equivalente

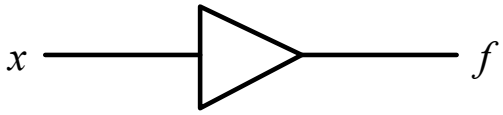


(c) Propagação parar diferentes valores de n

Buffer não inversor

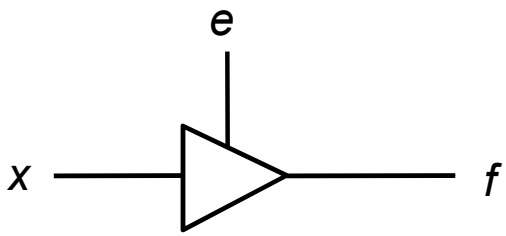


(a) circuito CMOS

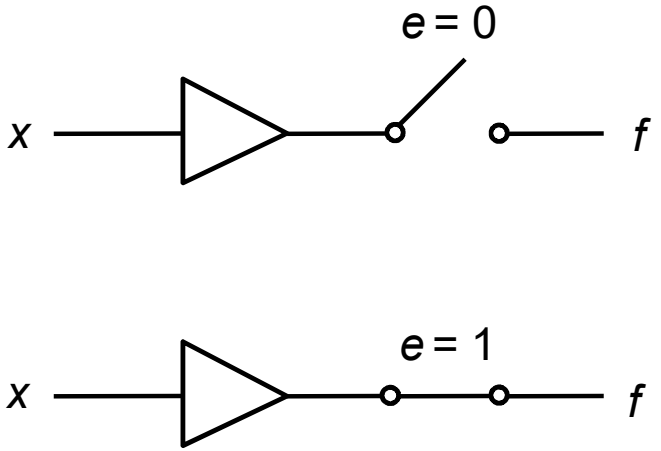


(b) símbolo gráfico

Buffer tri-state



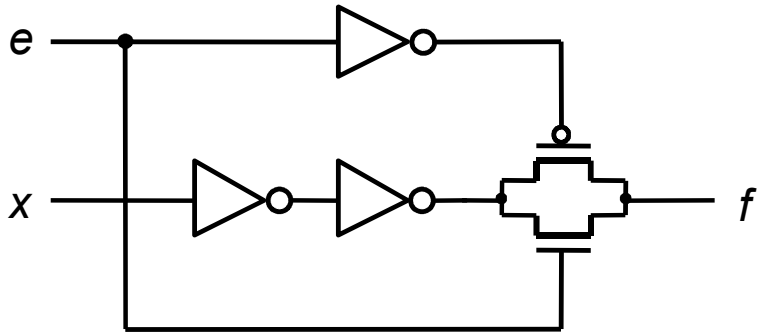
(a) Buffer tri-state



(b) Circuito equivalente

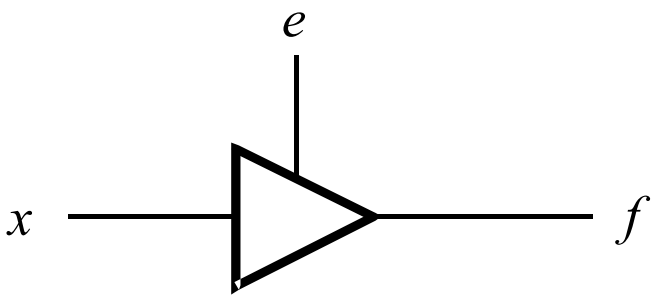
e	x	f
0	0	Z
0	1	Z
1	0	0
1	1	1

(c) Tabela Verdade

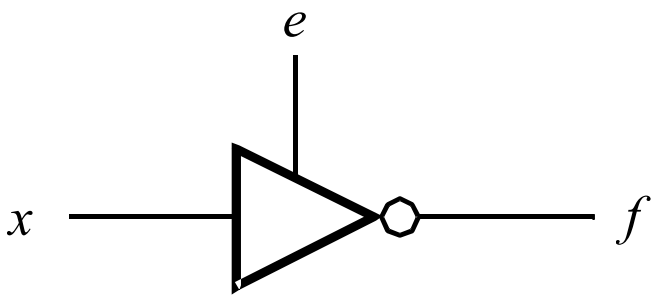


(d) Implementação

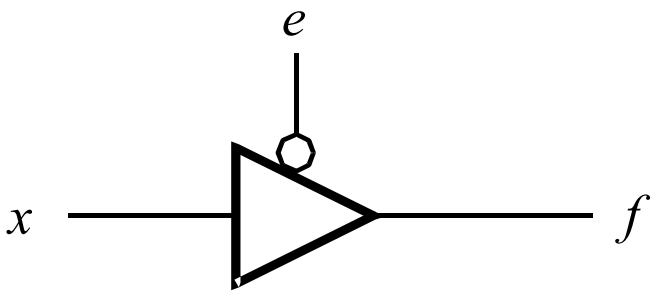
Buffers tri-state



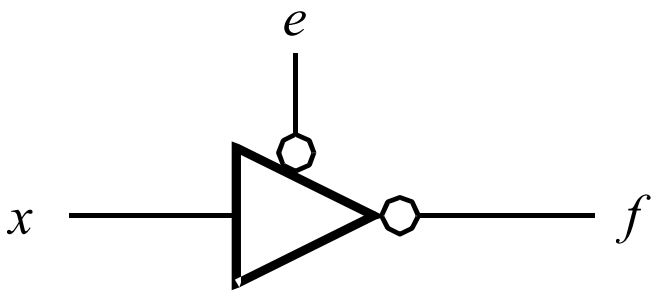
(a)



(b)

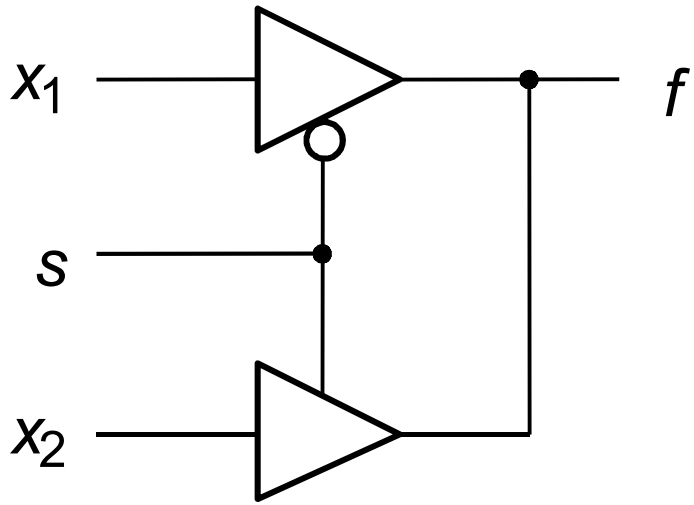


(c)



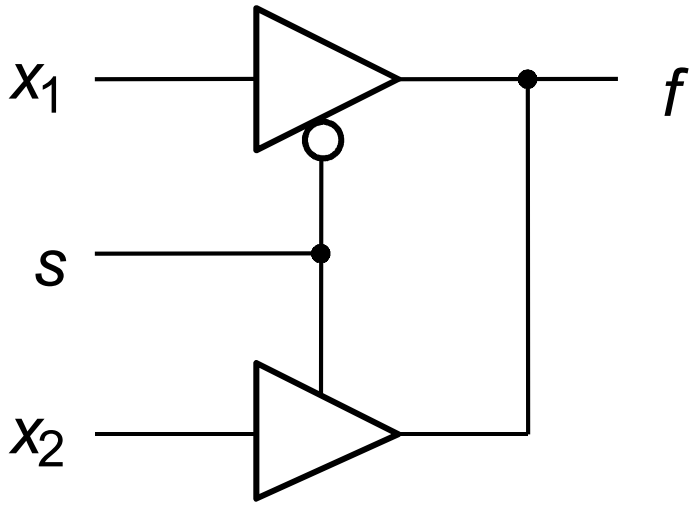
(d)

Uma utilização de buffers tri-state



Que circuito é este??

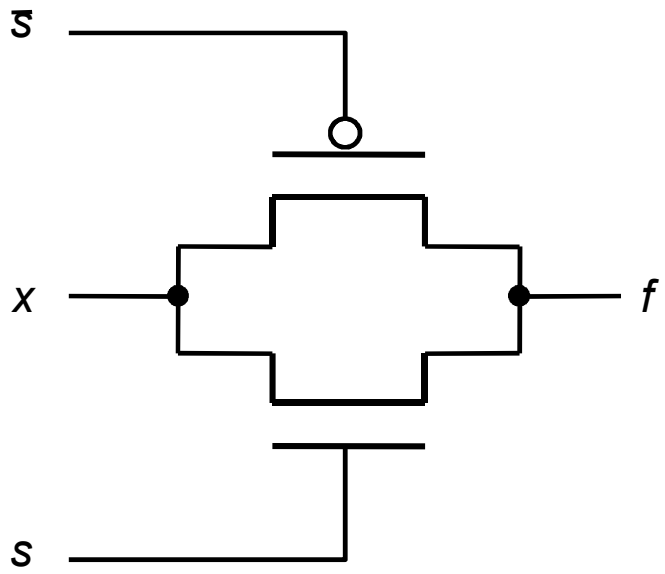
Uma utilização de buffers tri-state – MUX 2:1



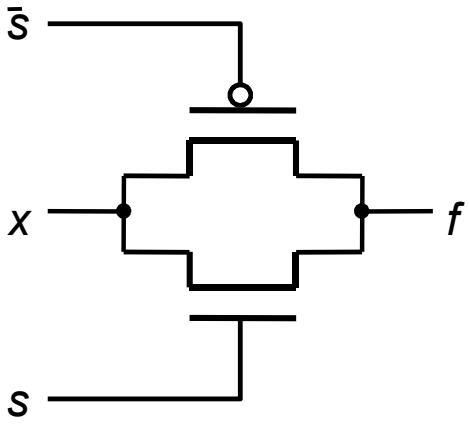
S	X1	X2	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

S	f
0	X1
1	X2

Qual é o comportamento deste circuito ???



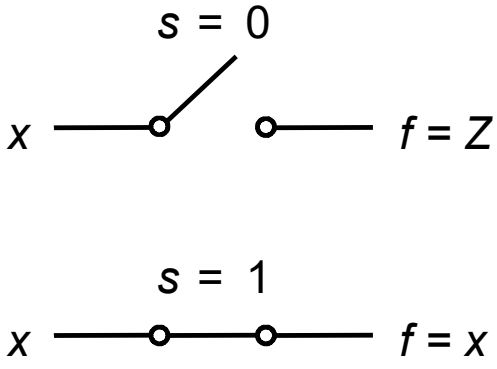
Transmission Gate – Chave CMOS



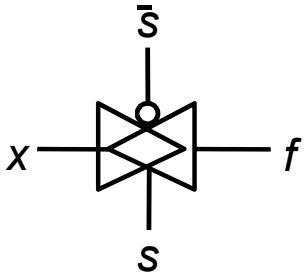
(a) Circuito

s	f
0	Z
1	x

(b) Tabela Verdade



(c) Circuito equivalente

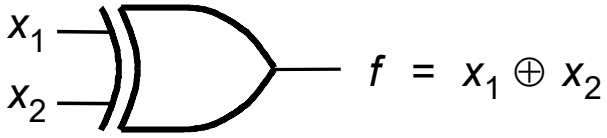


(d) Símbolo Gráfico

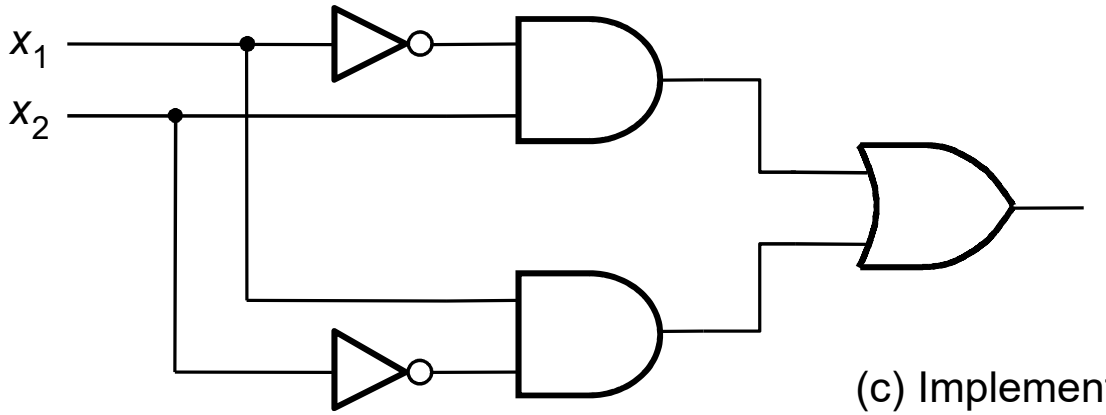
OU-Exclusivo – XOR

x_1	x_2	$f = x_1 \oplus x_2$
0	0	0
0	1	1
1	0	1
1	1	0

(a) Tabela Verdade



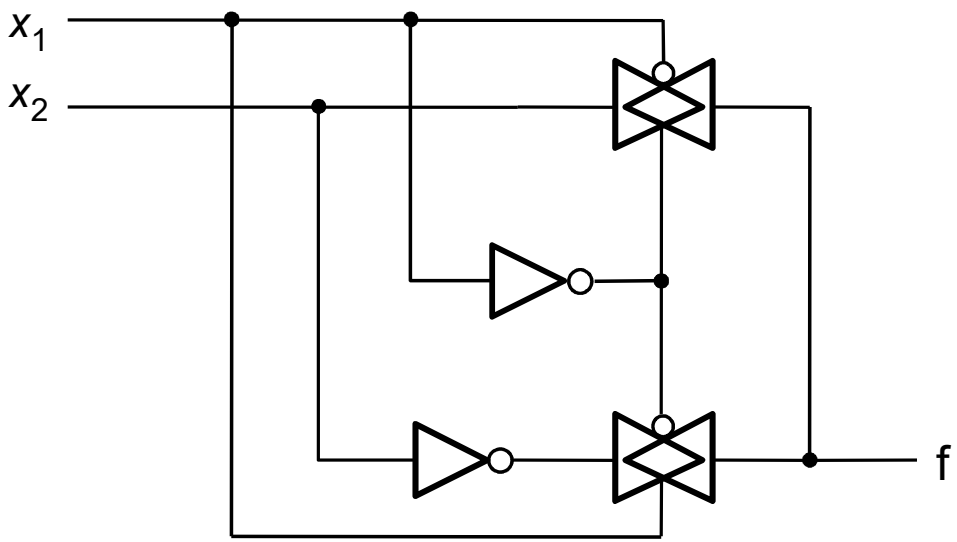
(b) Símbolo Gráfico



(c) Implementação usando SOP

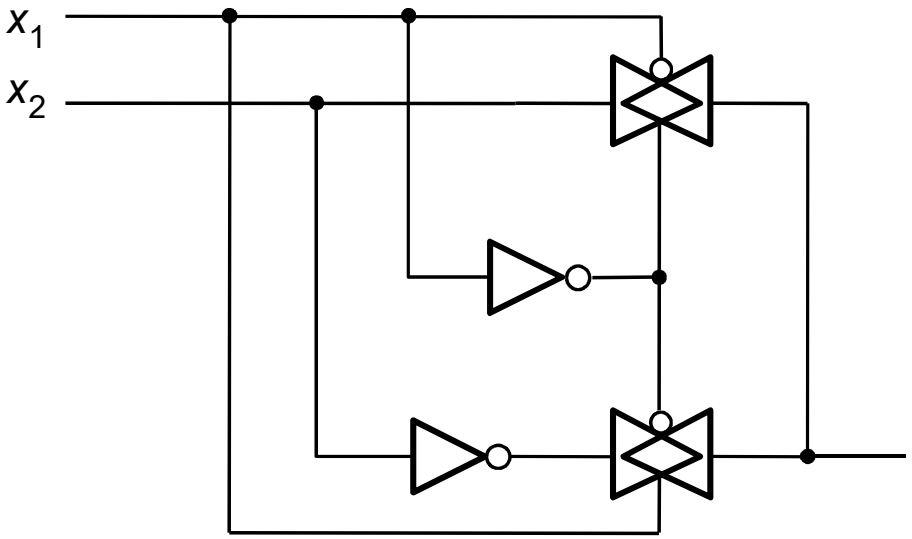
f = x1'x2 + x1x2'

Que circuito é este ???



Circuito CMOS

XOR com transmission gates

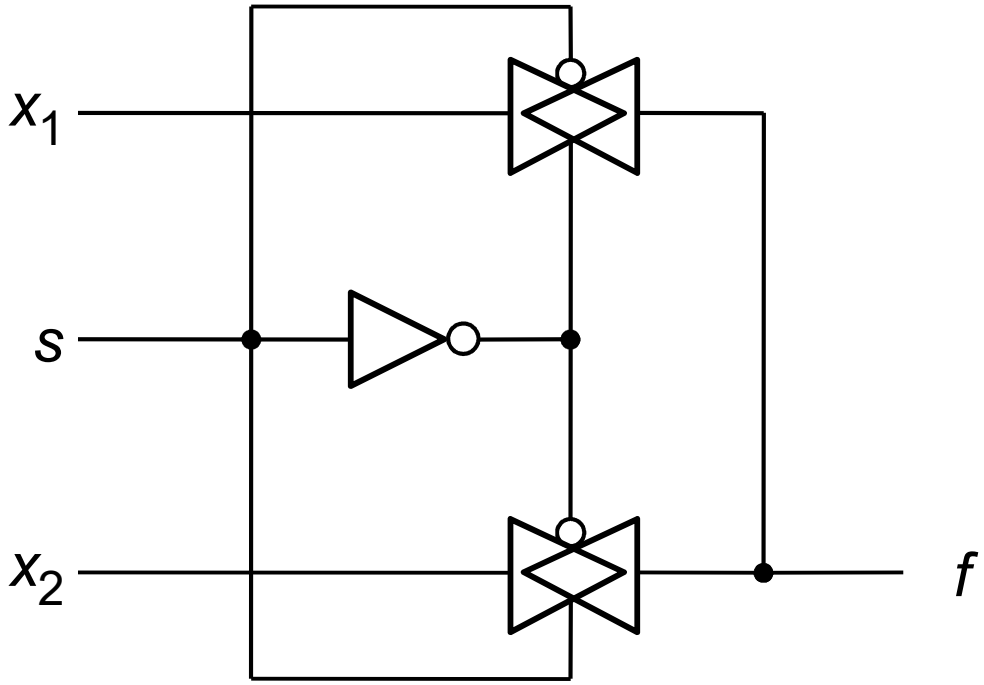


X1	f
0	X2
1	X2'

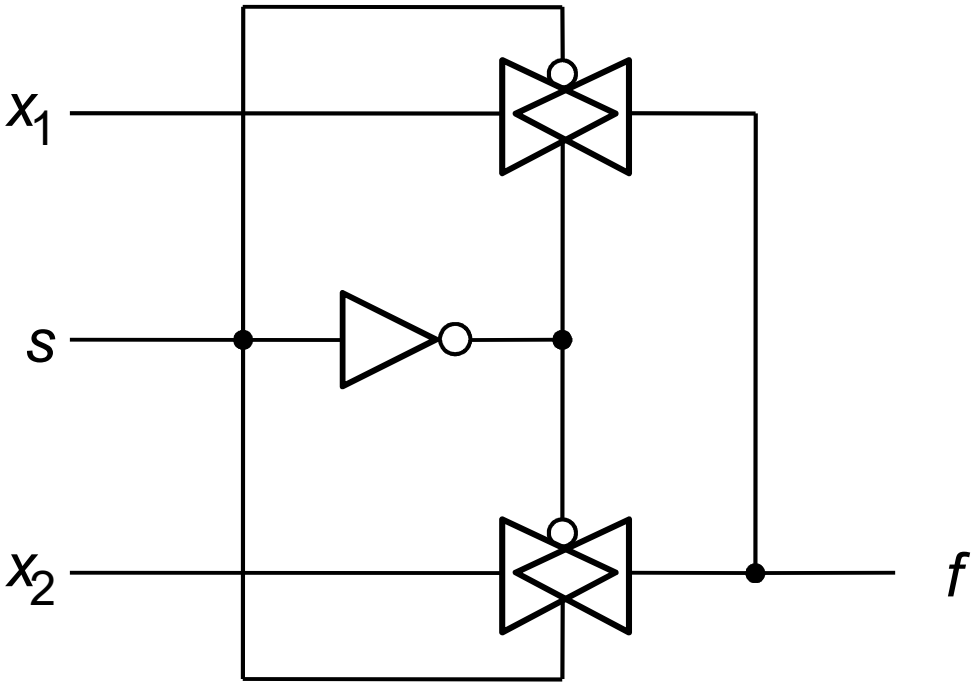
$f = x_1 \oplus x_2$

x1	x2	f
0	0	0
0	1	1
1	0	1
1	1	0

Que circuito é este ???



MUX 2:1 com transmission gate



S	X1	X2	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

S	f
0	X1
1	X2

EXERCÍCIO

Derivar o circuito CMOS da função f = xy + xz, com o menor número de transistores possível.

f = x.(y + z)

EXERCÍCIO

Derivar o circuito CMOS da função f = xy + xz, com o menor número de transistores possível.

1- Uma solução é fazer a' = x, b' = y e um c' = z → f = a'b' + a' c' = a' (b' + c')

2 – Outra solução

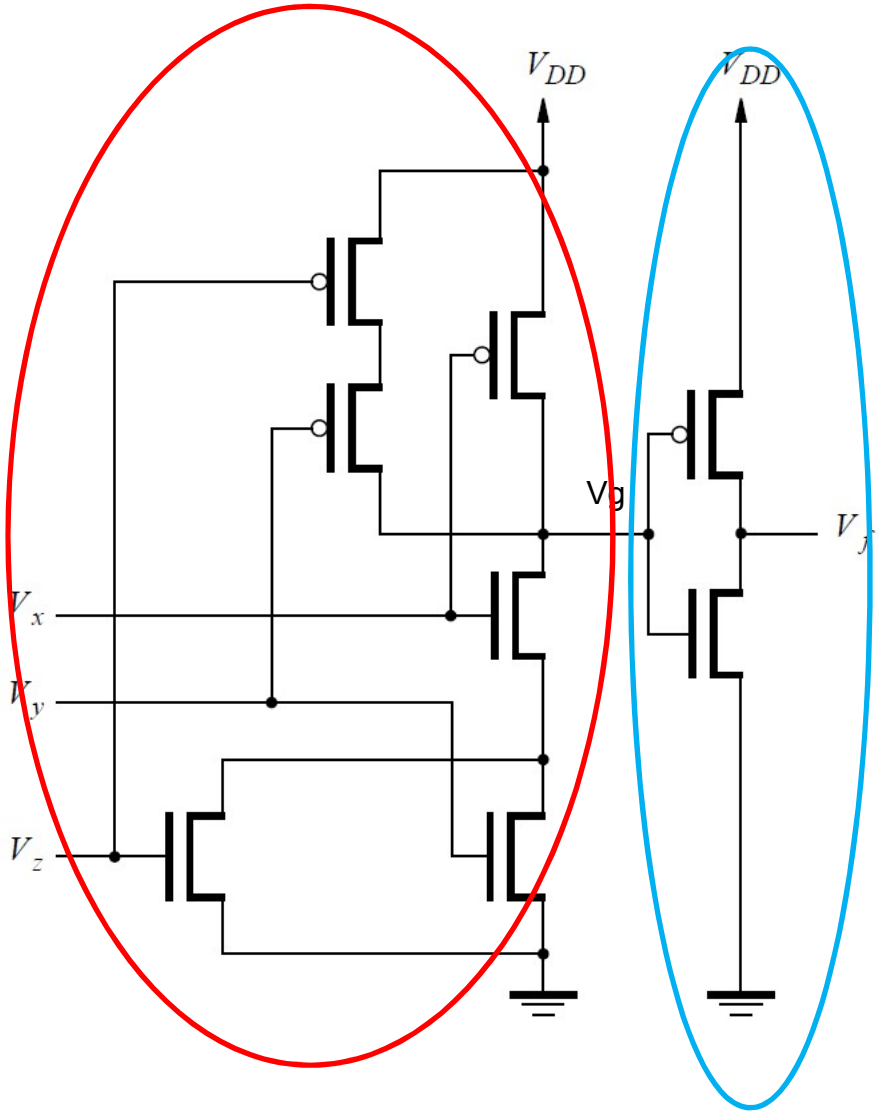
f = x (y+z)

f' = x' + $\overline{(y+z)}$

f' = x' + y'z' → se g = f' → g = x' + y'z'

f = g'

OBS – f = xy + xz ➔ f' = (xy + xz)' = (xy)' . (xz)' = (x' + y') . (x' + z') = x' + y'.z'


V_{DD}
V_{DD}
Vg
V_f
V_x
V_y
V_z